# Design issues for IP intra-train feedback

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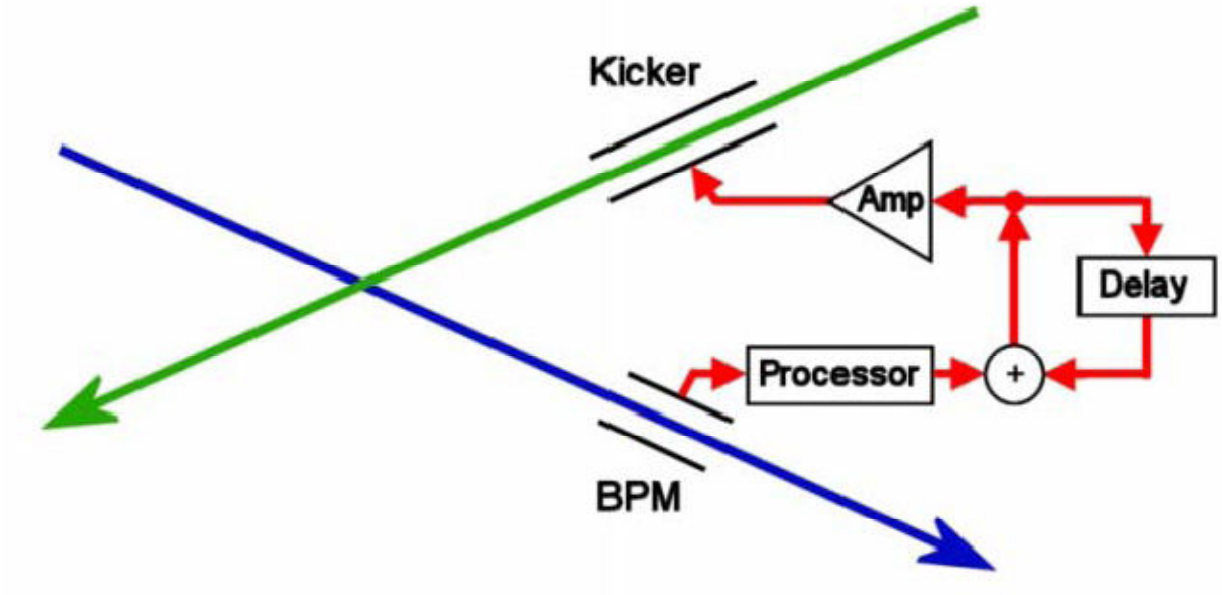
# Outline

- Reminder of IP intra-train feedback system
- General considerations
- ILC RDR layout (comment on simulations)
- Prototype hardware (FONT systems)
- Engineering integration issues
- Summary

# IP intra-train feedback system - concept

- Last line of defence against relative beam misalignment
- Measure vertical position of outgoing beam and hence beam-beam kick angle
- Use fast amplifier and kicker to correct vertical position of beam incoming to IR




**FONT – Feedback On Nanosecond Timescales**

**(Oxford, Daresbury, CERN, DESY, KEK, SLAC)**

# General considerations (1)

**1. IP position feedback:**

**hardware located near IP**

**kicker at 90 degrees w.r.t. IP**

**2. IP angle feedback:**

**hardware ideally located near IP**

**kicker in phase w.r.t. IP**

**3. Additional possibilities:**

**(bunch-by-bunch) luminosity scan system (from BEAMCAL)**

**information from alignment systems (eg. QD0 etc.)**

**‘feed-forward’ information from upstream in machine (eg. DR)**

**…**

# General considerations (2)

**Time structure of bunch train:**

**ILC (500 GeV): c. 3000 bunches w. c. 300 ns separation**
**CLIC (3 TeV): c. 300 bunches w. c. 0.5 ns separation**

**Feedback latency:**

**ILC: O(100ns) latency budget allows digital approach**
**CLIC: O(10ns) latency requires analogue approach**

**Recall speed of light: c = 30 cm / ns:**

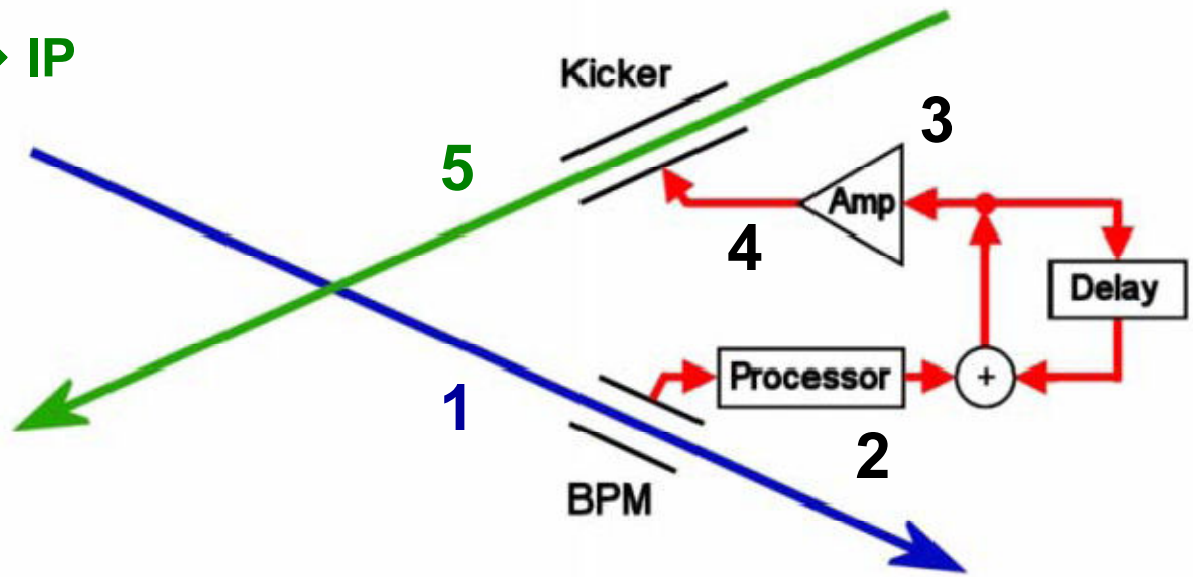
**FB hardware should be close to IP (especially for CLIC!)**

# IP position feedback latency

**Designed for (bunch-by-bunch) position correction of beams at IP**

**Latency:**

1. **Beam flight time IP → BPM**
2. **Signal processing, FB calculation**
3. **Amplifier + kicker response time**
4. **Cable delays**
5. **Beam flight time kicker → IP**

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# Latency issues

- **BPM or kicker further from IP**
  - → **longer beam flight distance**
  - → **increase latency (3ns per metre)**
- **Electronics further from beamline**
  - → **longer cable runs**
  - → **increase latency (4-5ns per metre)**
- **FB system electronics latency**

# ILC RDR Design (schematic)

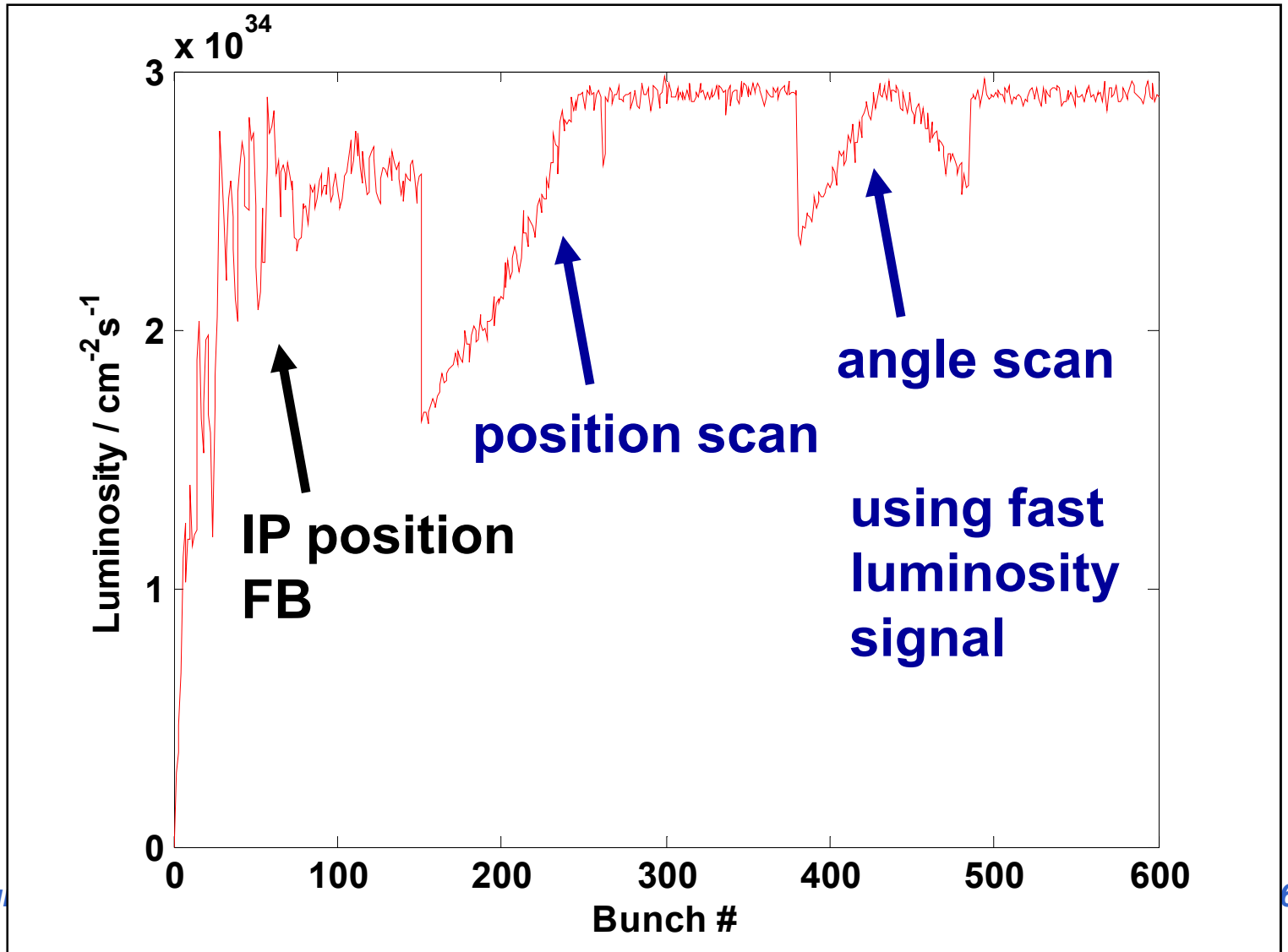
1. IP position feedback:
   provide IP beam position correction at +- 50 sigma_y level
   i.e. +- 300 nm of vertical beam motion at IP

2. IP angle feedback: hardware located few 100 metres upstream
   conceptually very similar to position FB, (arguably) less critical

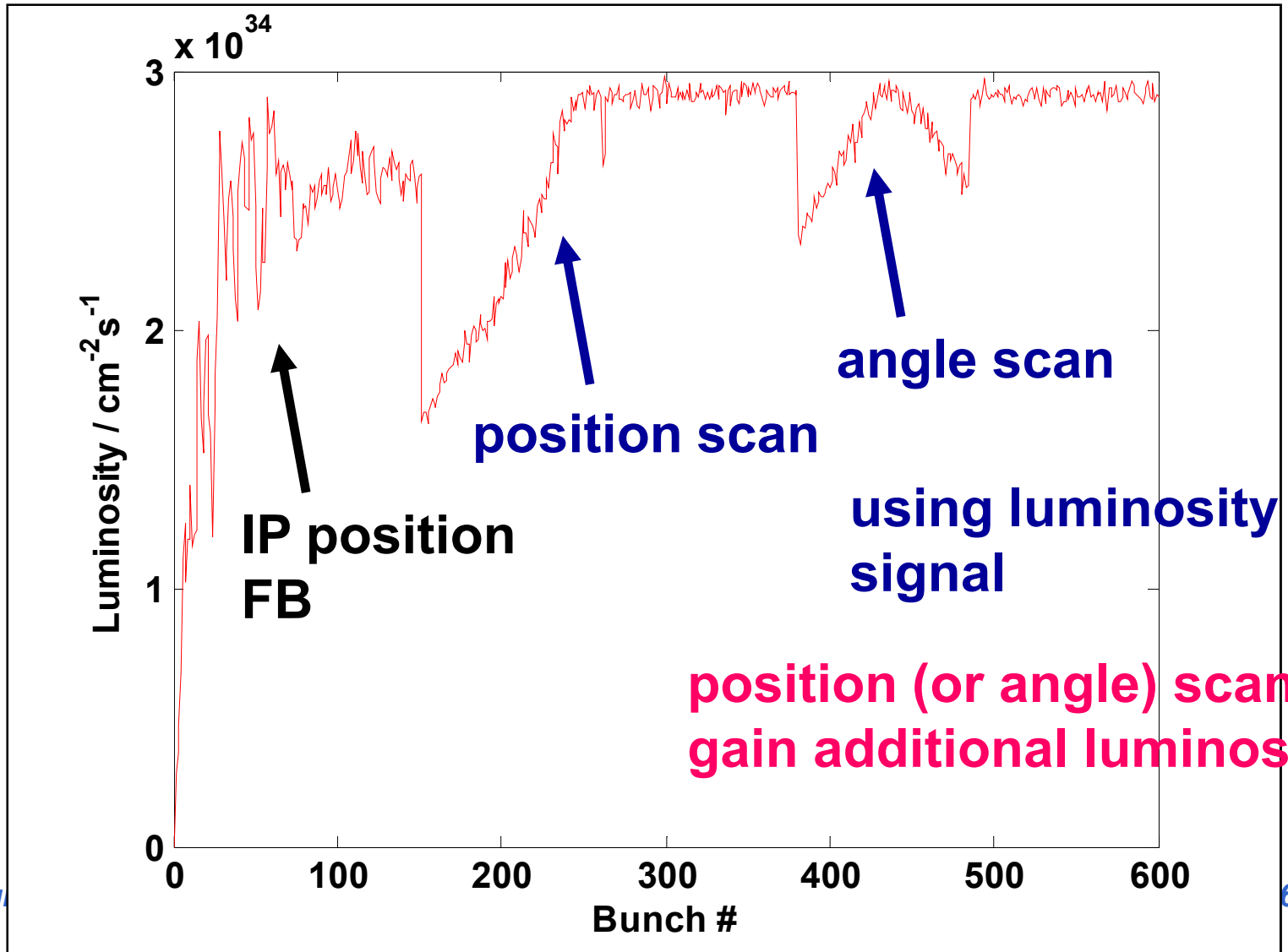
3. Bunch-by-bunch luminosity signal (from BEAMCAL)

   ‘special’ systems requiring dedicated hardware + data links

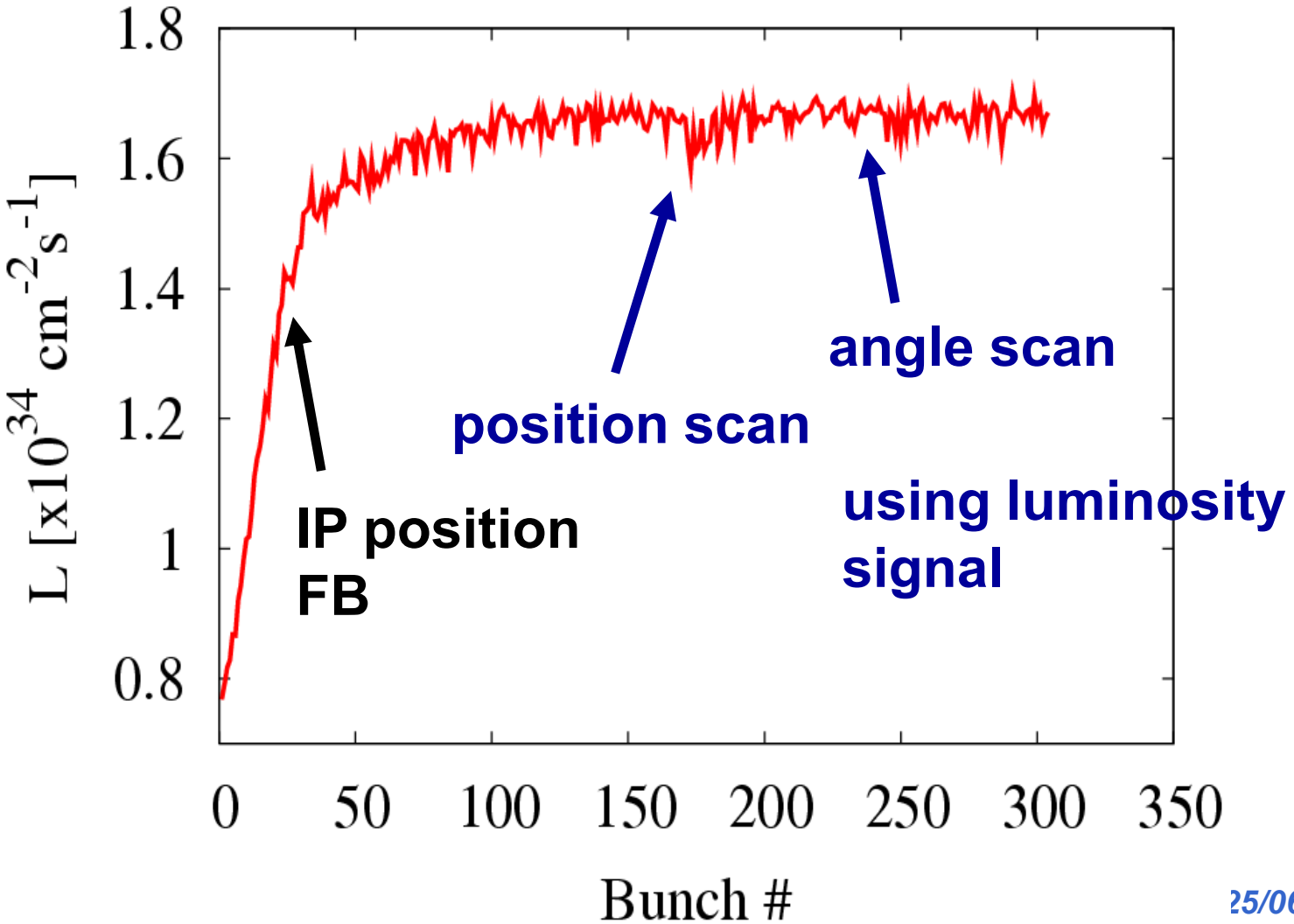
# IP intra-train FB performance (White)



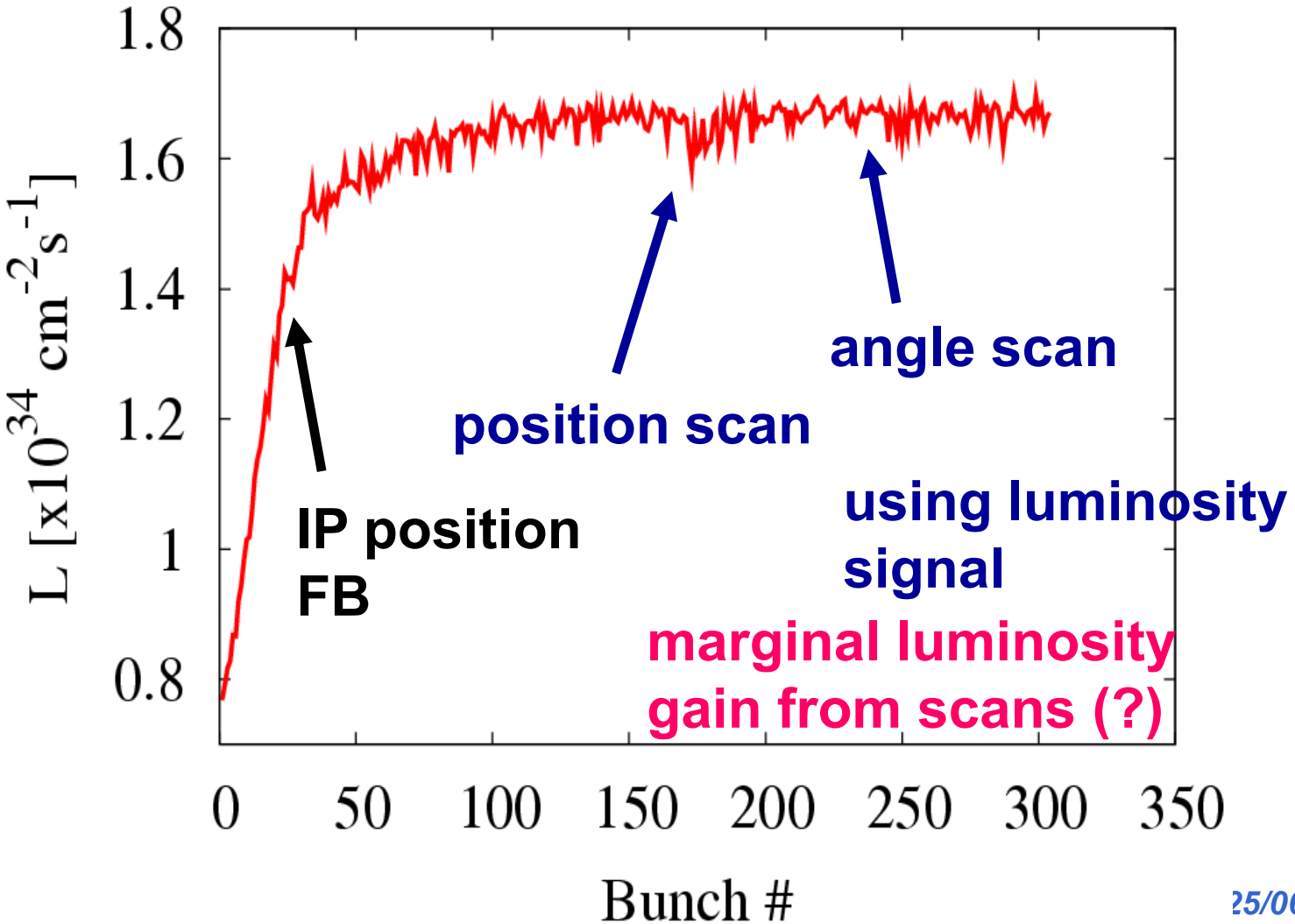
# IP intra-train FB performance (White)



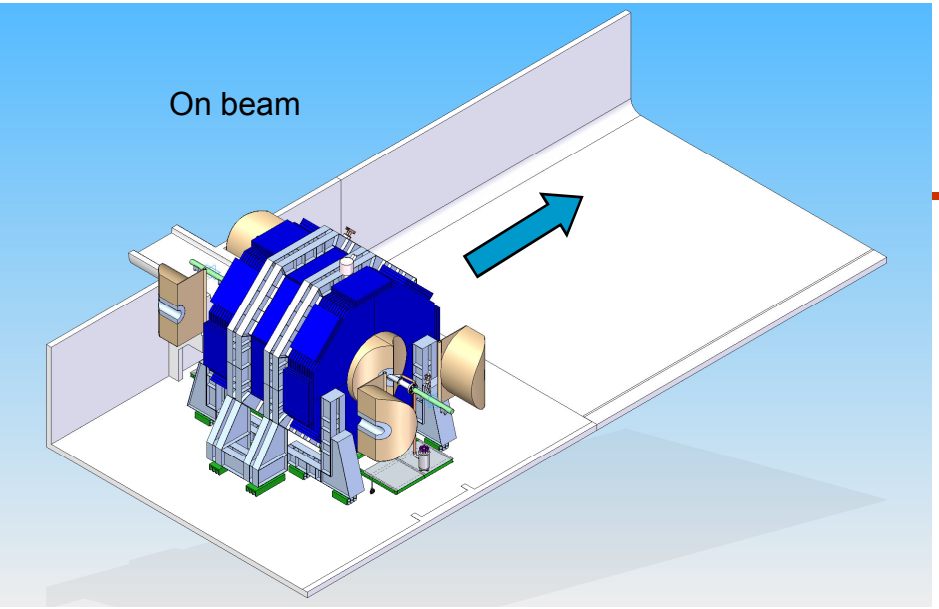
# IP intra-train FB performance (Lopez)

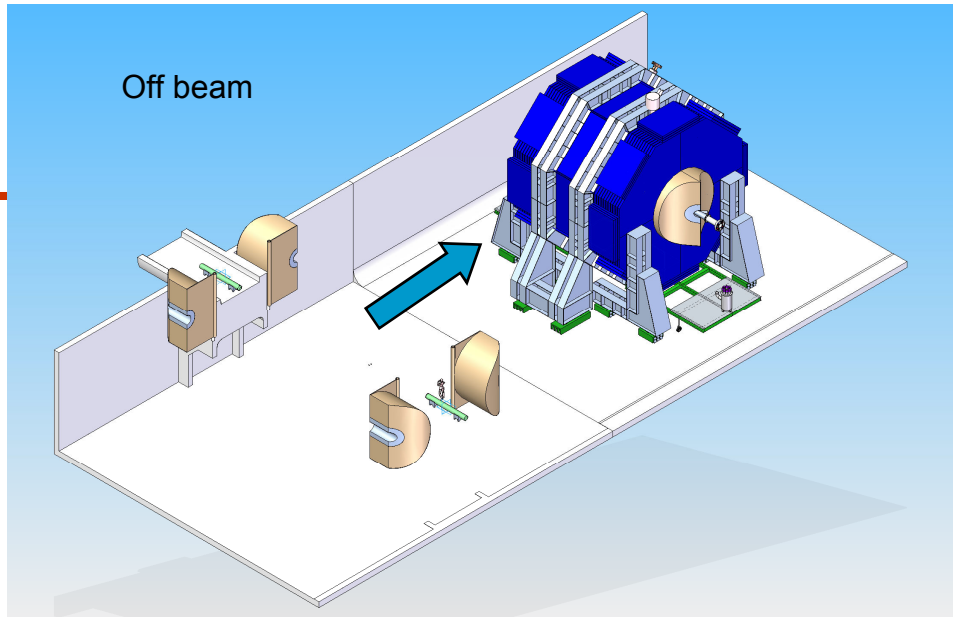


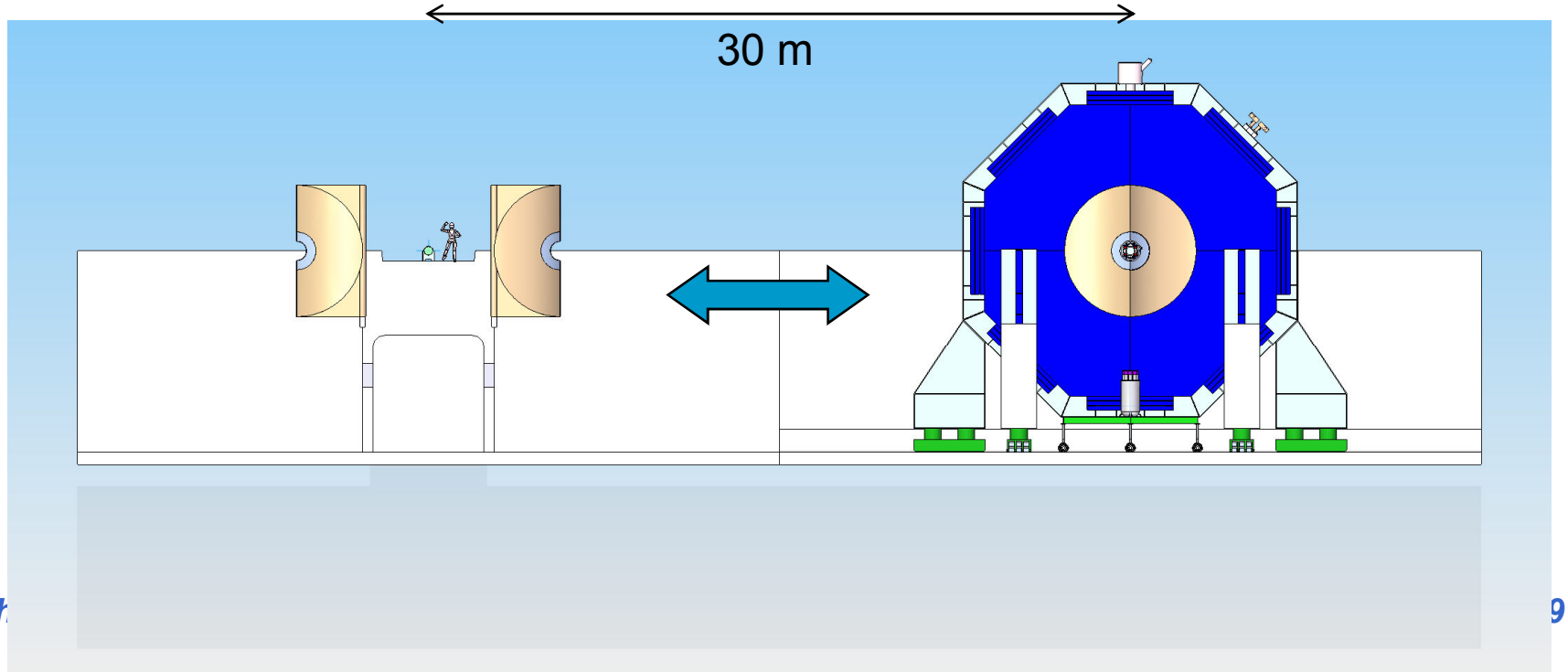
# IP intra-train FB performance (Lopez)



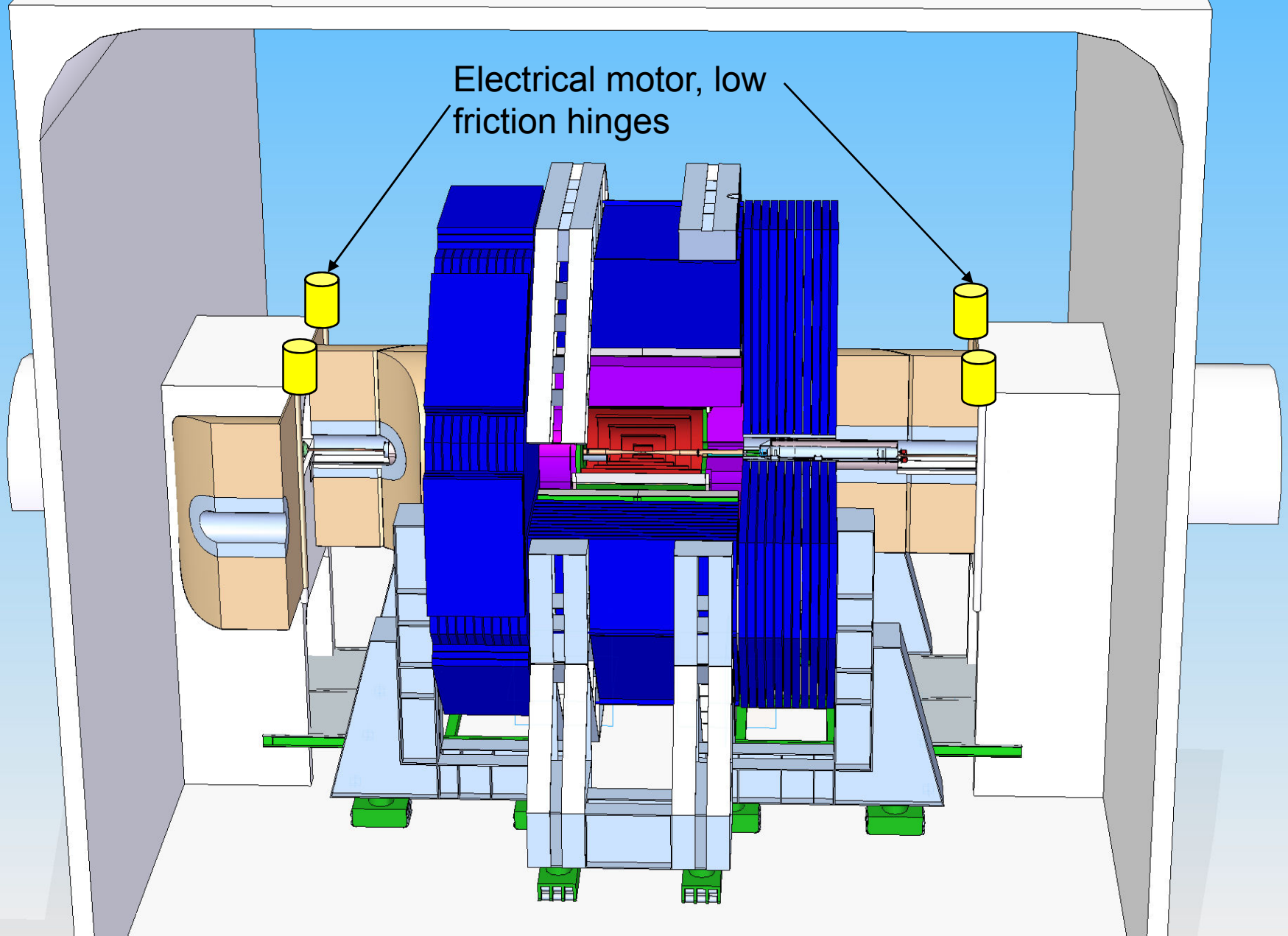
# ILC: Push-pull concept for detectors



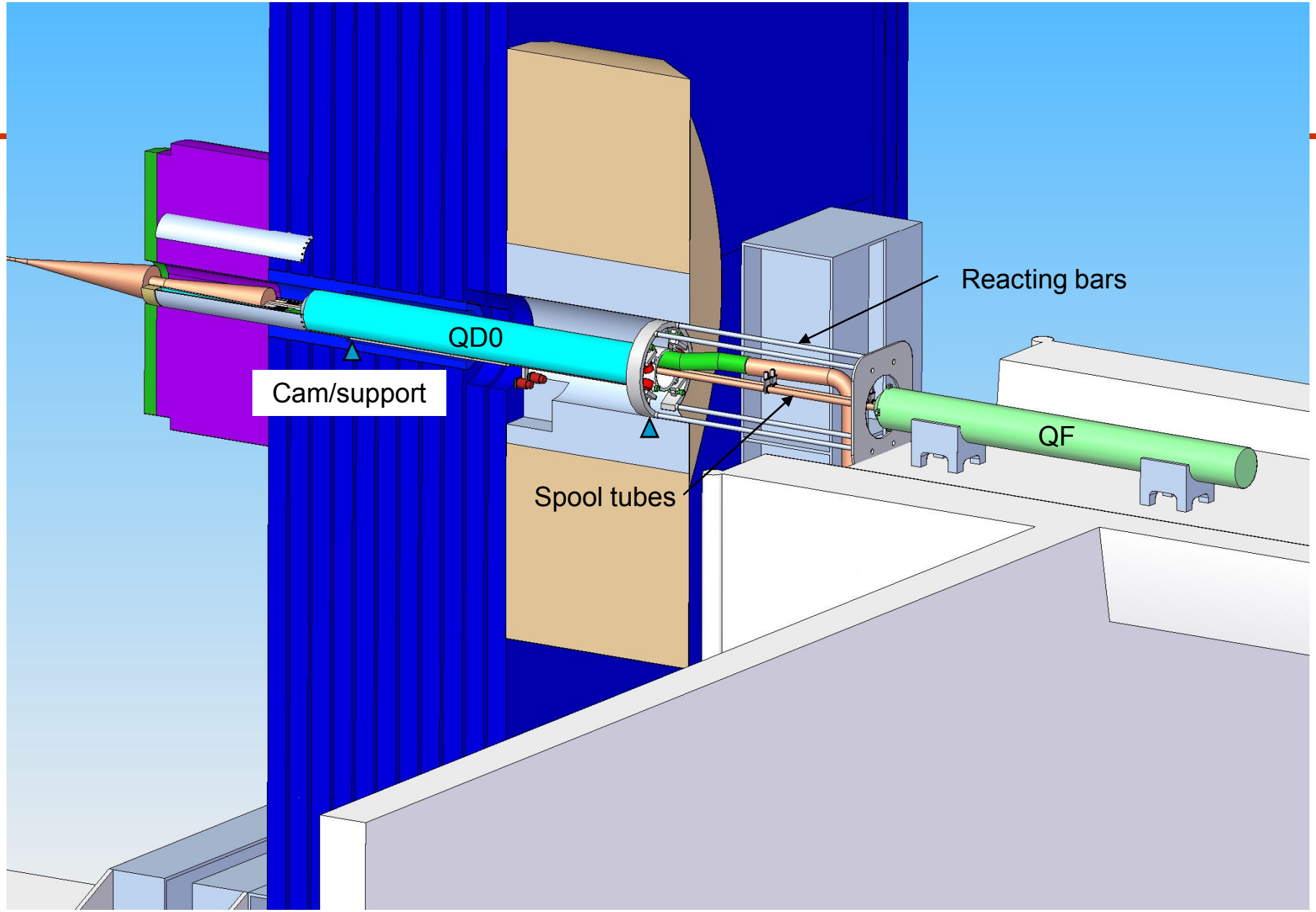



# Silicon Detector (SiD) Concept

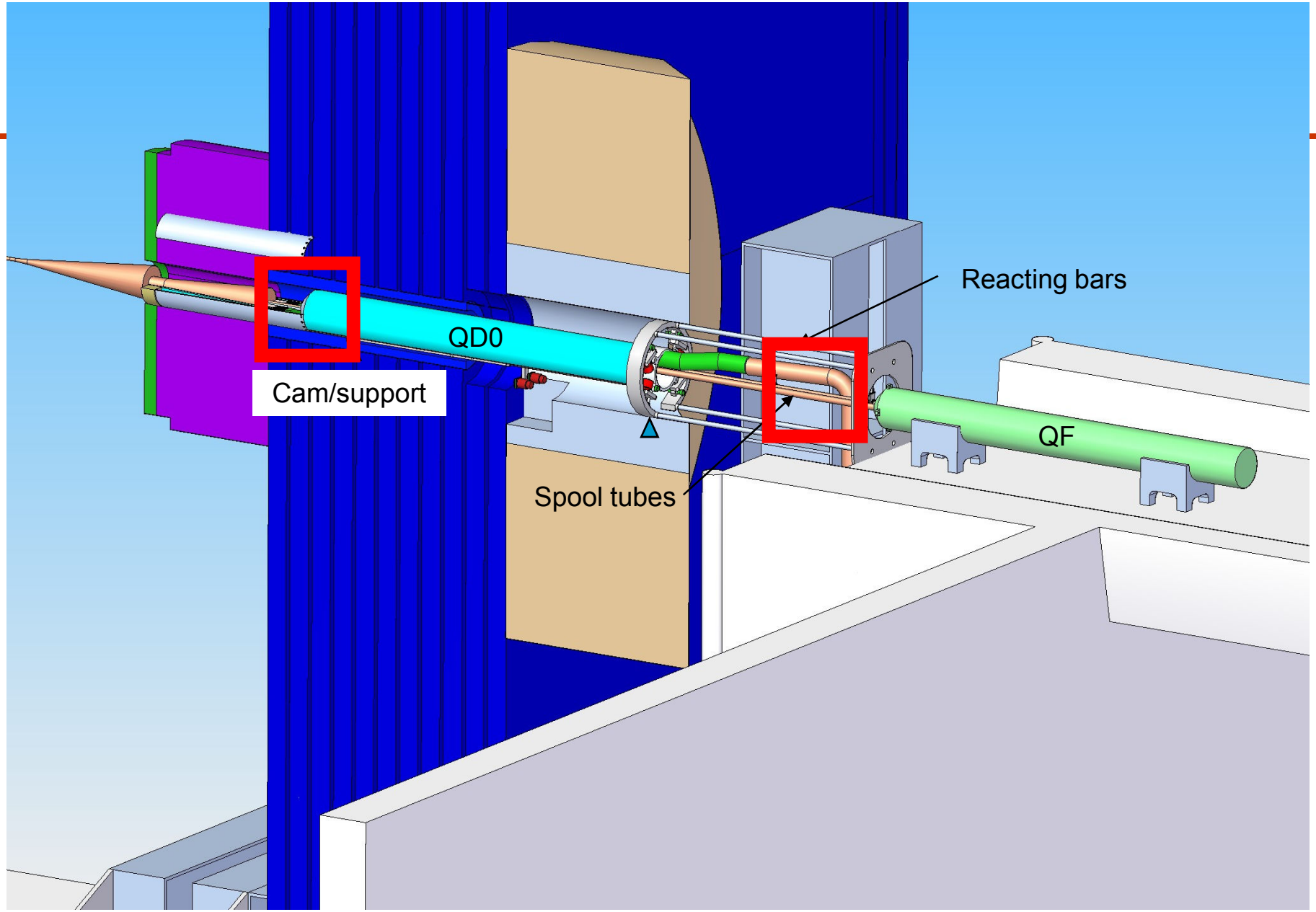


# Final Doublet Region




Opening 2 m on the beam

# Final Doublet Region




Opening 2 m on the beam

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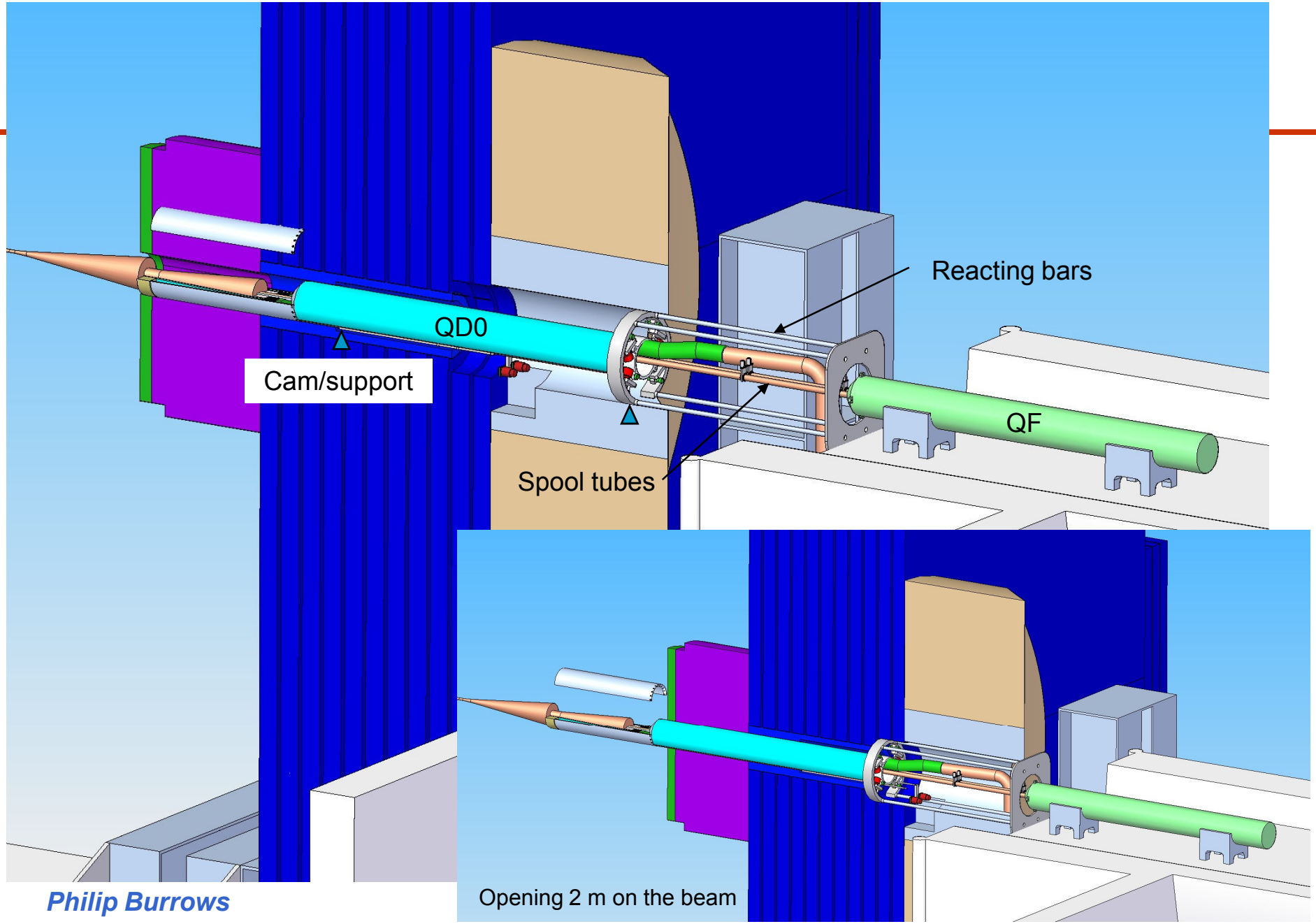


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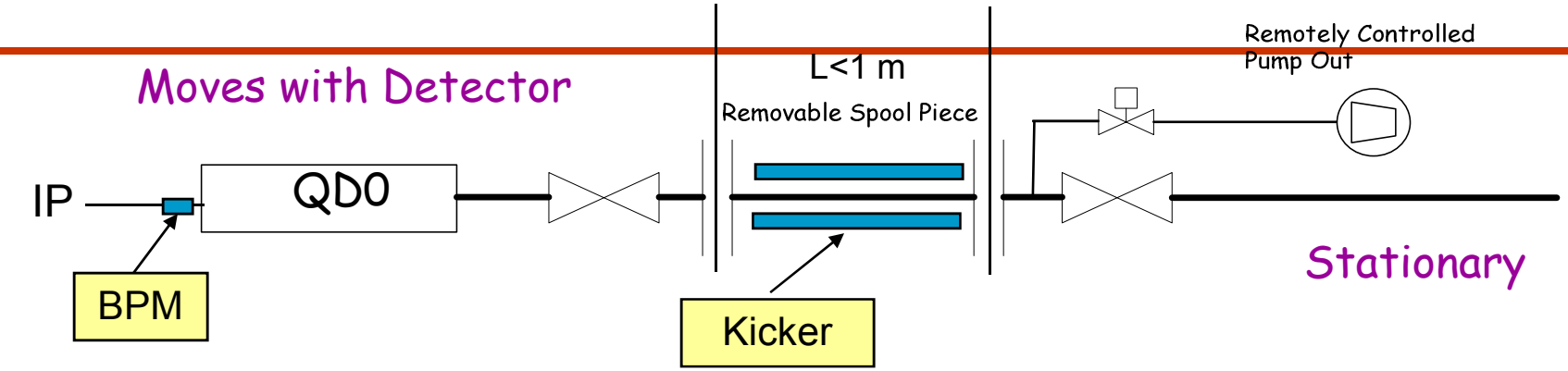
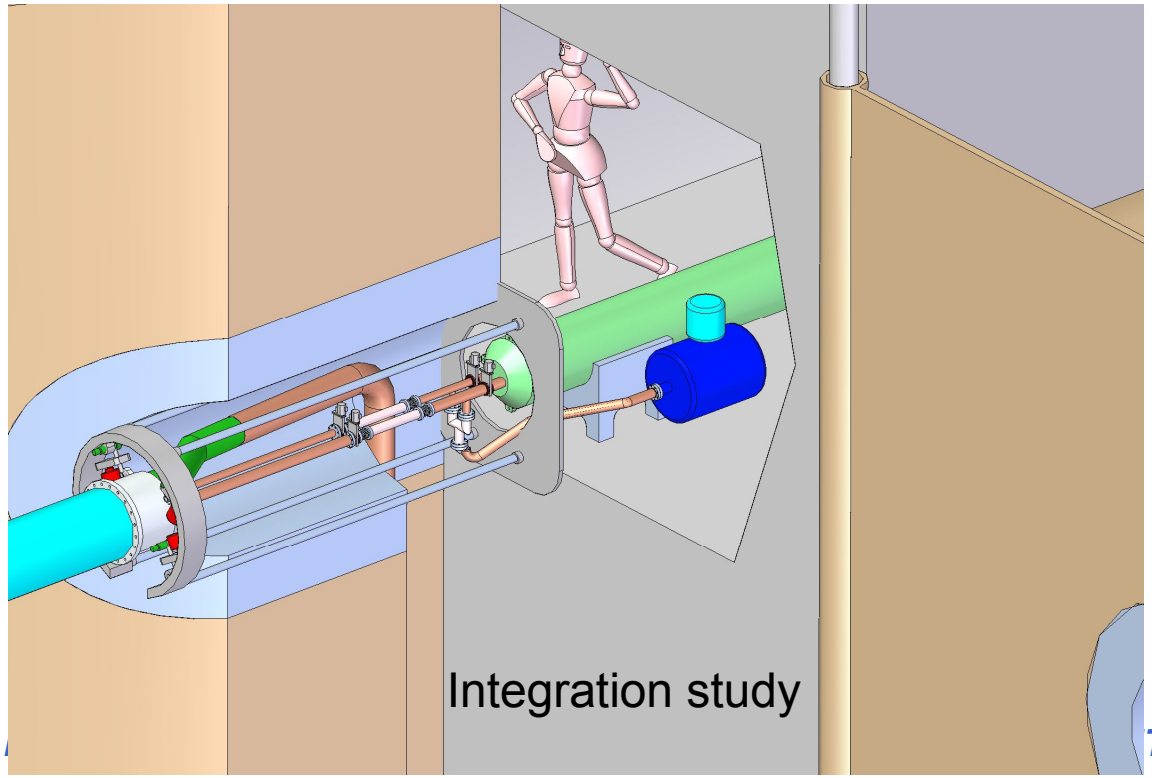
# Feedback Instrumentation & Vacuum Design




**Present vacuum requirements :**

**P < 1nT in the BDS**

**P < 100nT in the experimental region**

•We may rely on the cryopumping from QD0

•We do not need extra pumps

•We do not need periodic bake out *in situ.*

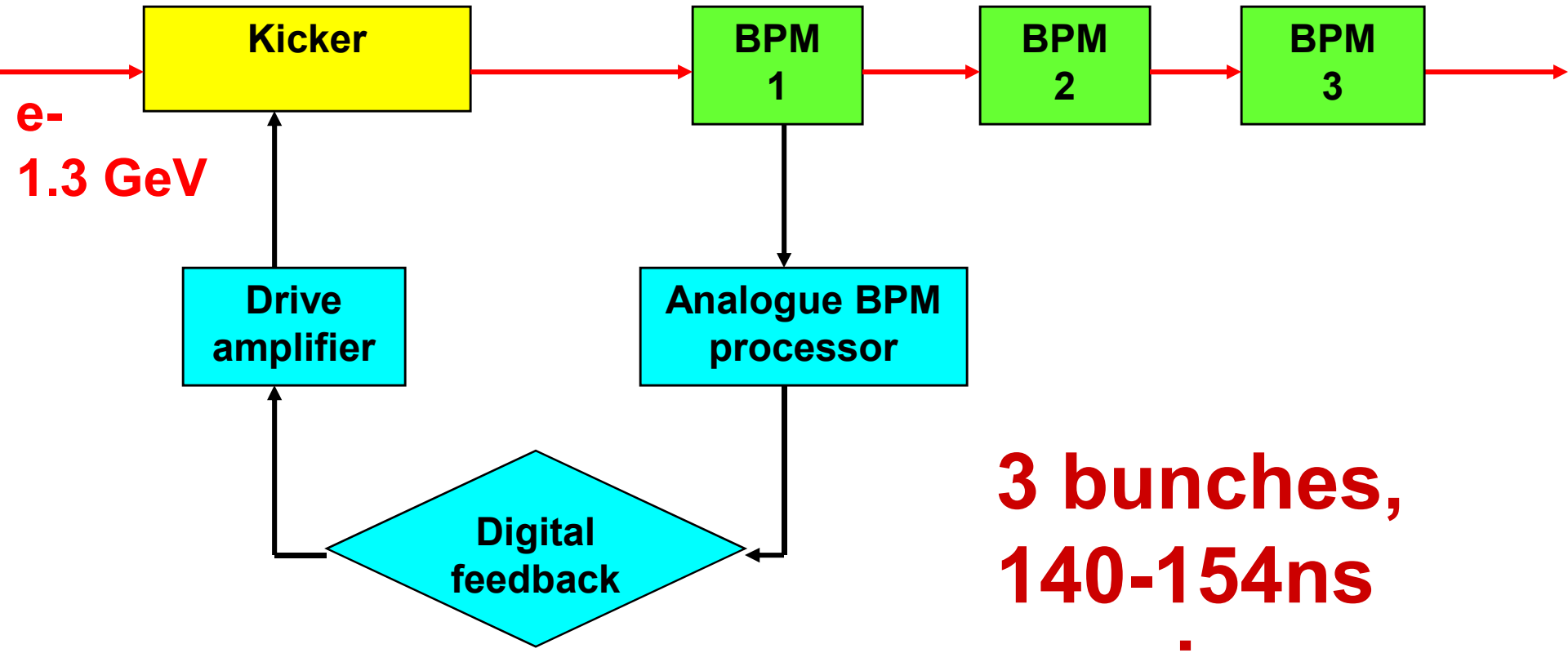
Open point :

•The beam instrumentation required

•Shut-off valves

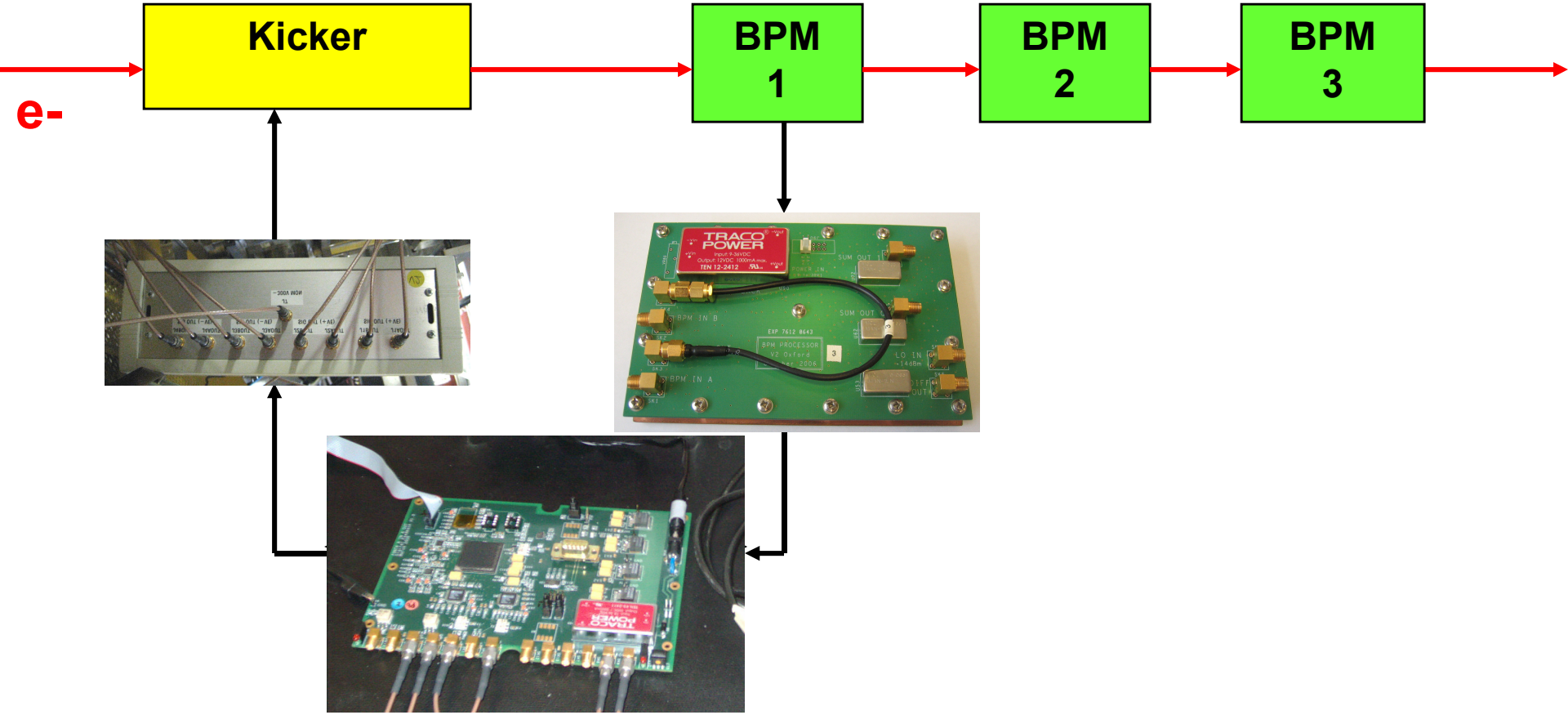
# ILC feedback prototype status

# FONT4 ILC prototype at KEK/ATF

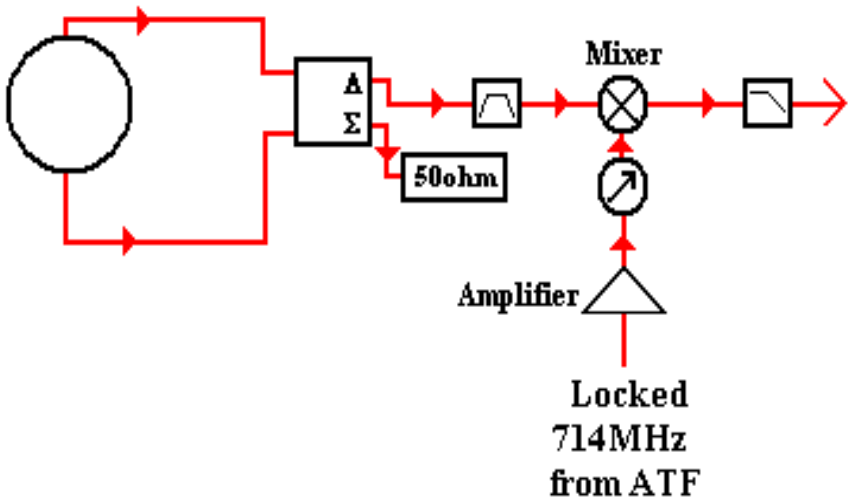


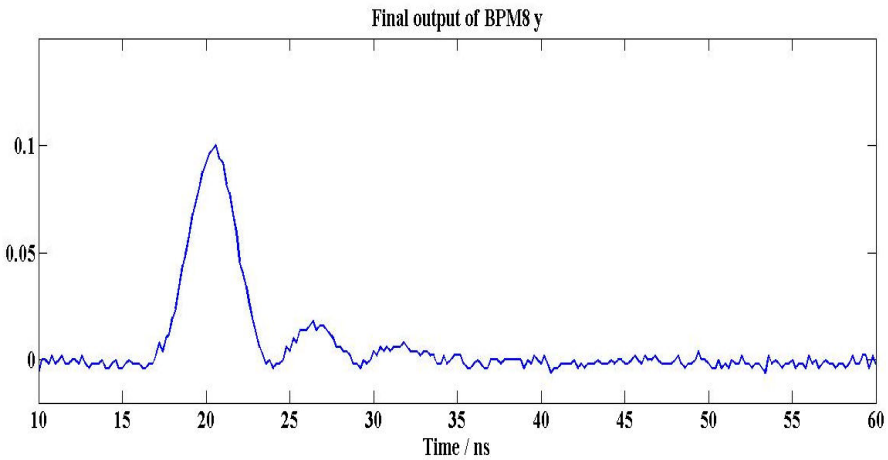

**3 bunches, 140-154ns spacing**

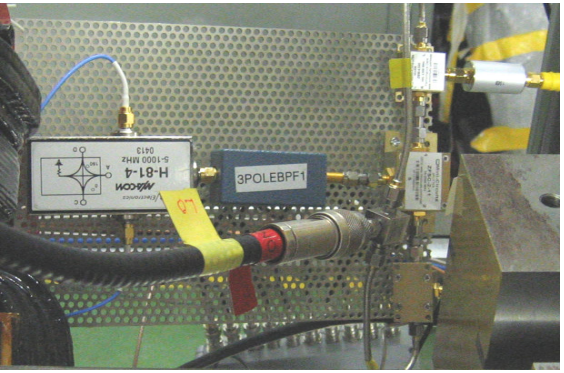
# FONT4 ILC prototype at KEK/ATF



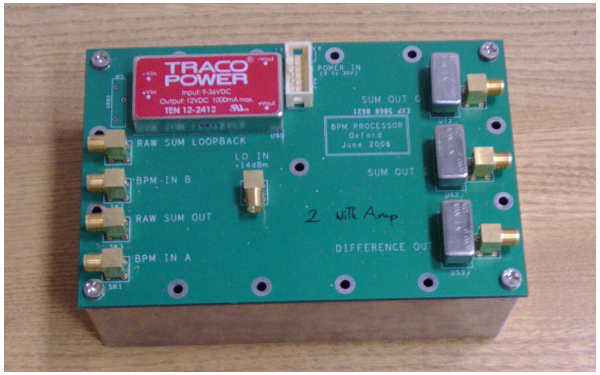
# BPM processor



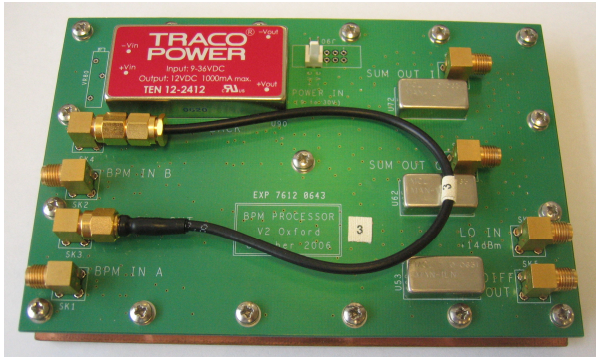




2005

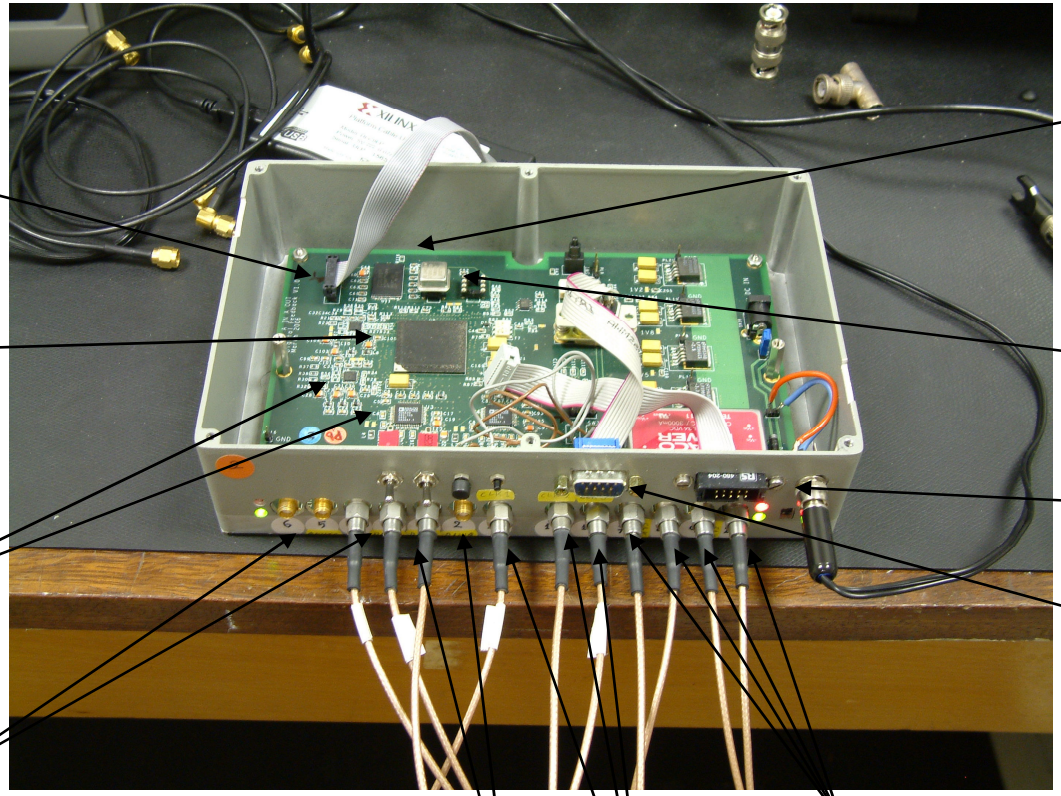



2006




2007

# Digital Feedback Board



JTAG port

PROM

Xilinx Virtex4 FPGA

40 MHz oscillator

GP I/O Header

Analog Devices ADC/DACs

RS232 comms

2 x Analog Output channels (differential)

4 x General-purpose digital outputs

2 x Analog Input channels (single-ended)

3 x external clock/trigger inputs

# Kicker driver amplifier

**Specifications:**

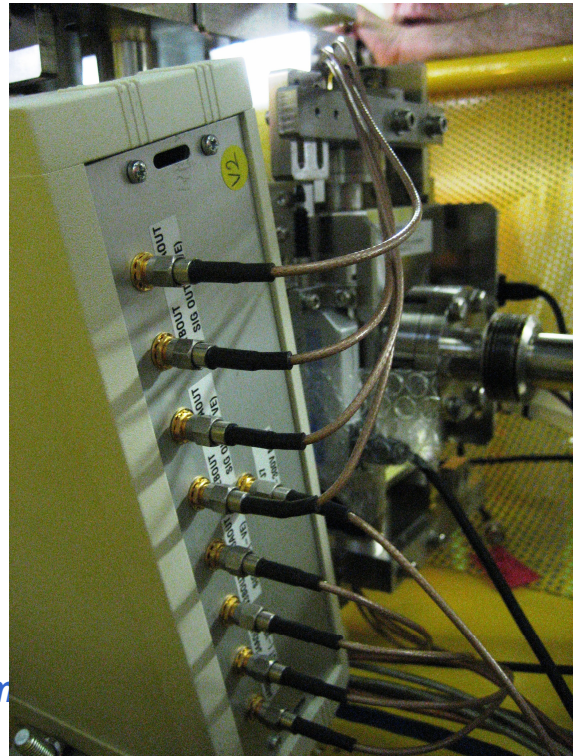
- **+- 15A (kicker terminated with 50 Ohm)**
- **+- 30A (kicker shorted at far end)**
- **35ns risetime (to 90%)**
- **pulse length 10 us (specified for 20-60 bunches)**
- **repetition rate 10 Hz**

**Outline design done in Oxford**

**Order placed with TMD Technologies Sept 06**

**Two prototype units delivered Dec 06**

**Tested numerous times with beam in 2007 and 2008**



# Latency estimate

- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 10ns

  Irreducible latency: 14ns

- BPM processor: 10ns
- ADC/DAC (3.5 89 MHz cycles) 40ns
- Signal processing (9 357 MHz cycles) 28ns
- FPGA i/o 3ns
- Amplifier 35ns
- Kicker fill time 3ns

  Electronics latency: 119ns

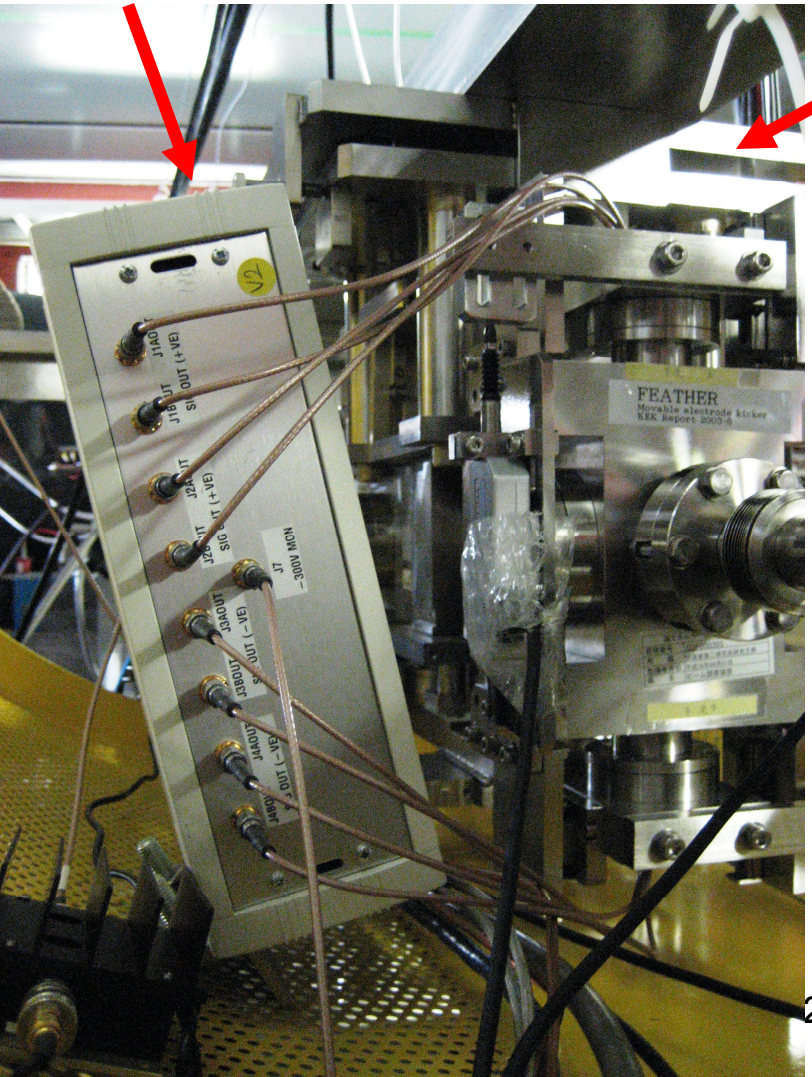
- Total latency budget: 133ns

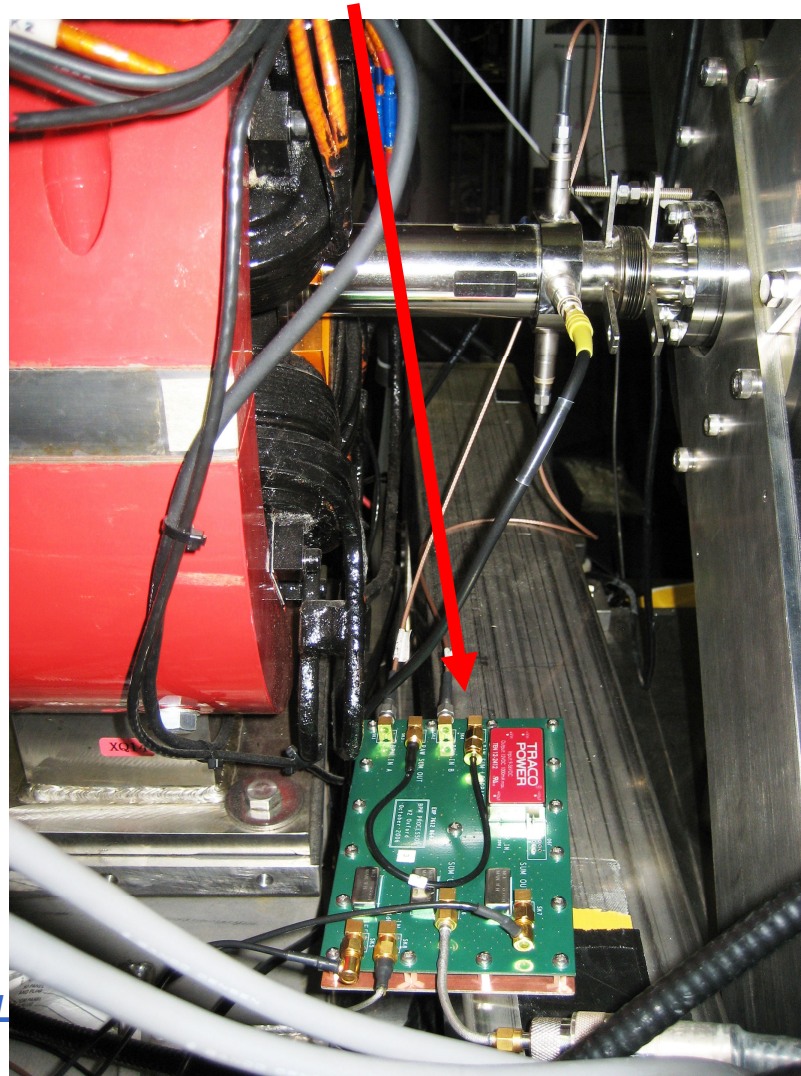
# FONT4 beamline section

Amplifier

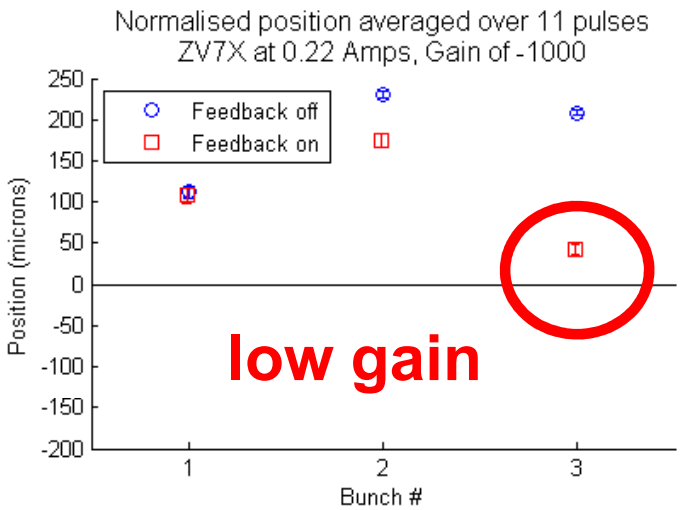
FEATHER
Kicker

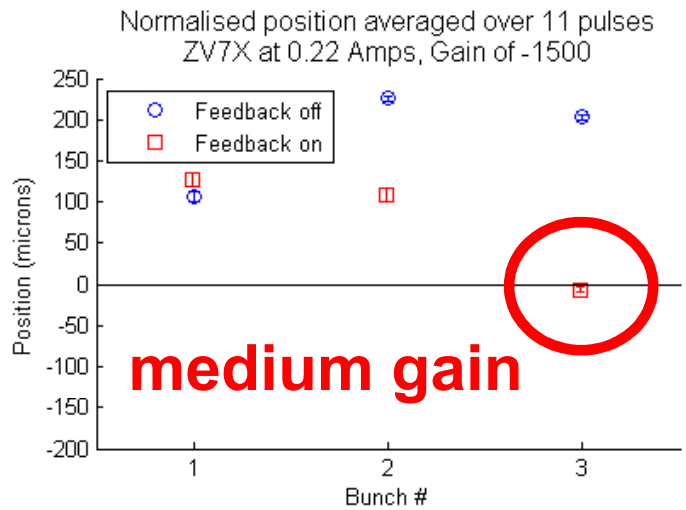
BPM processor board

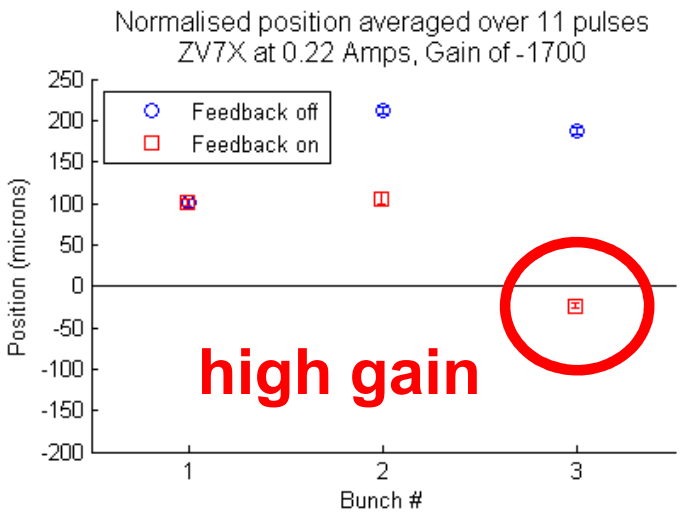


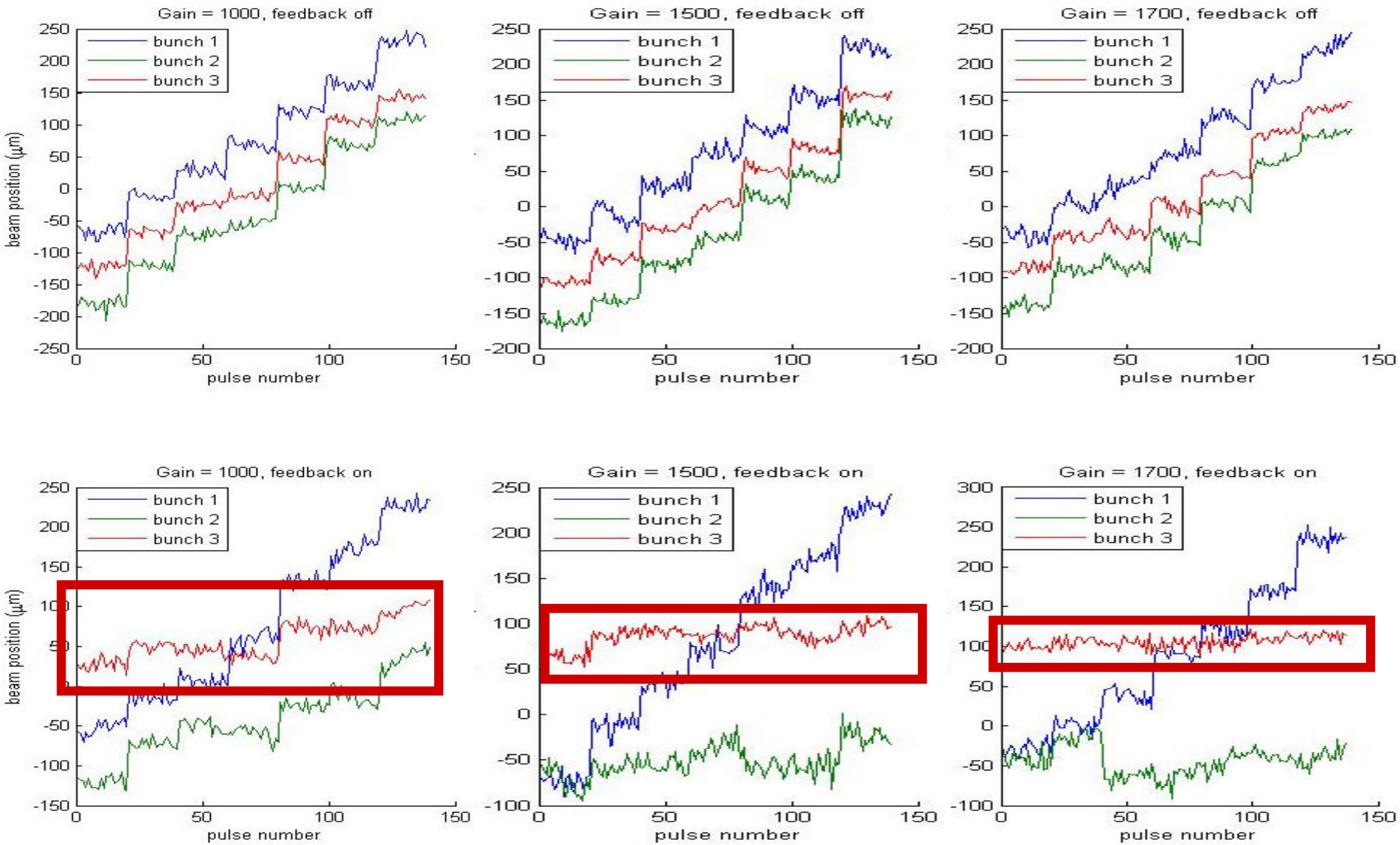
# Example (1) of Results



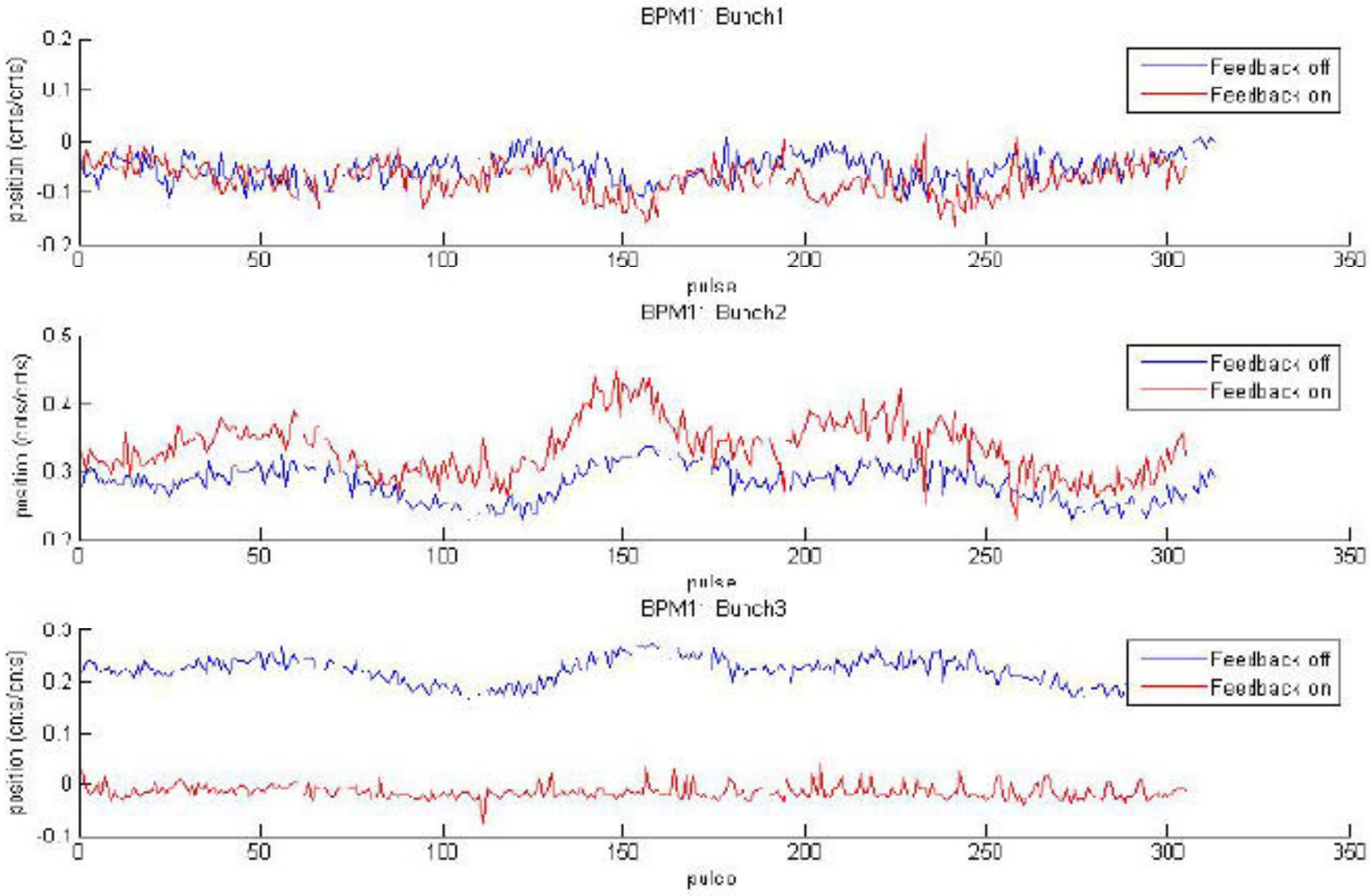



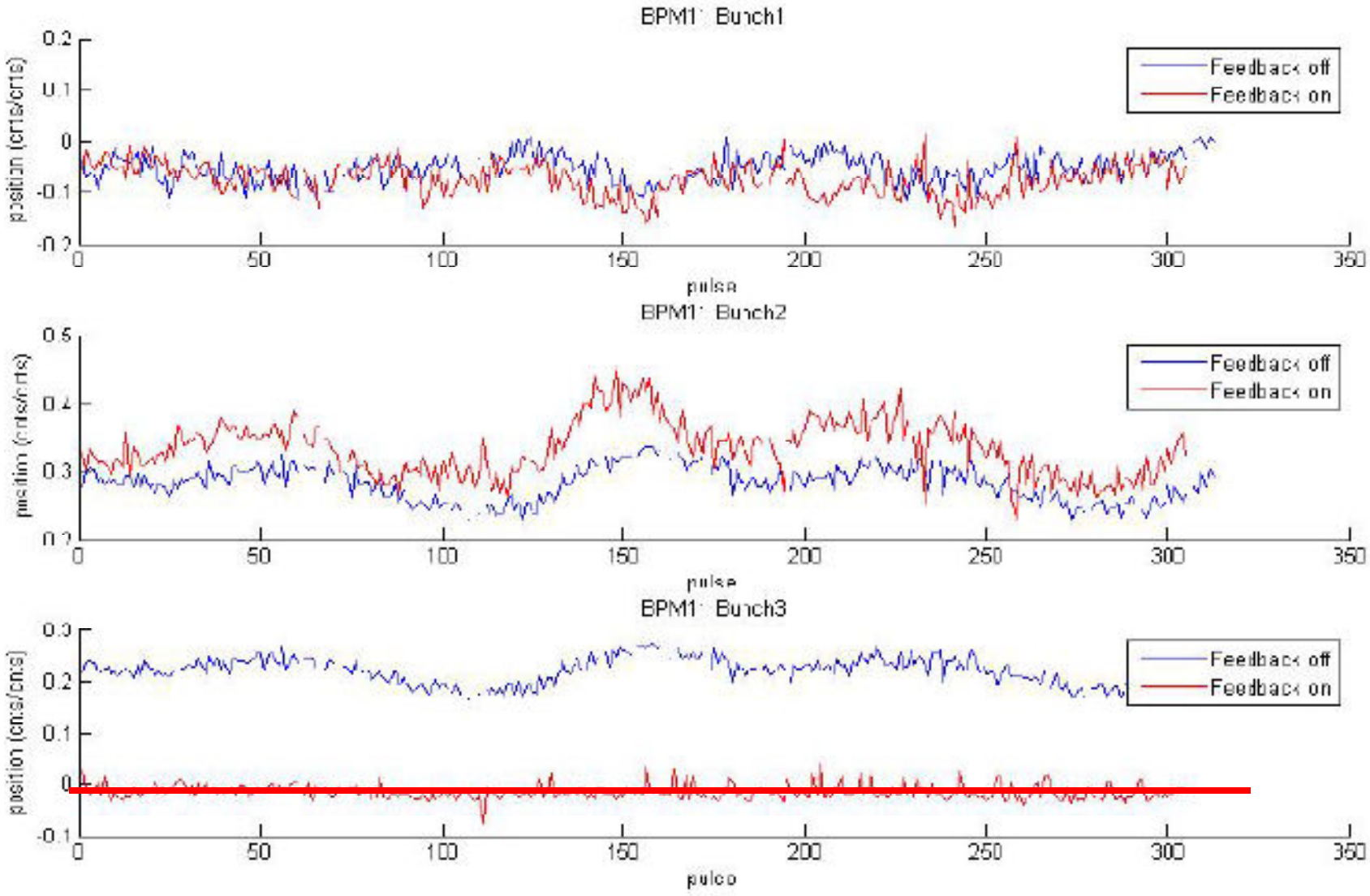
# Example (2) of Results



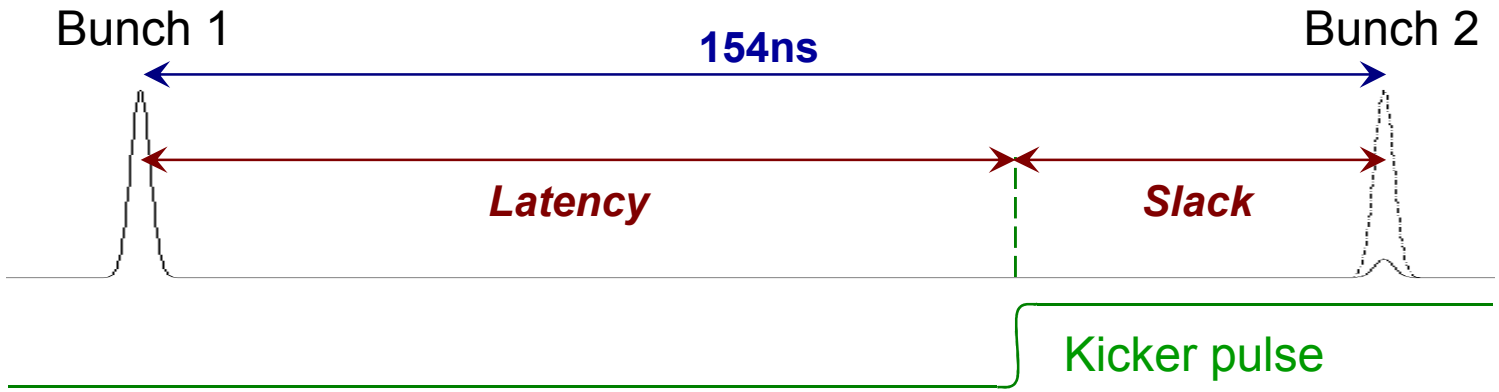
# Example (3) of Results

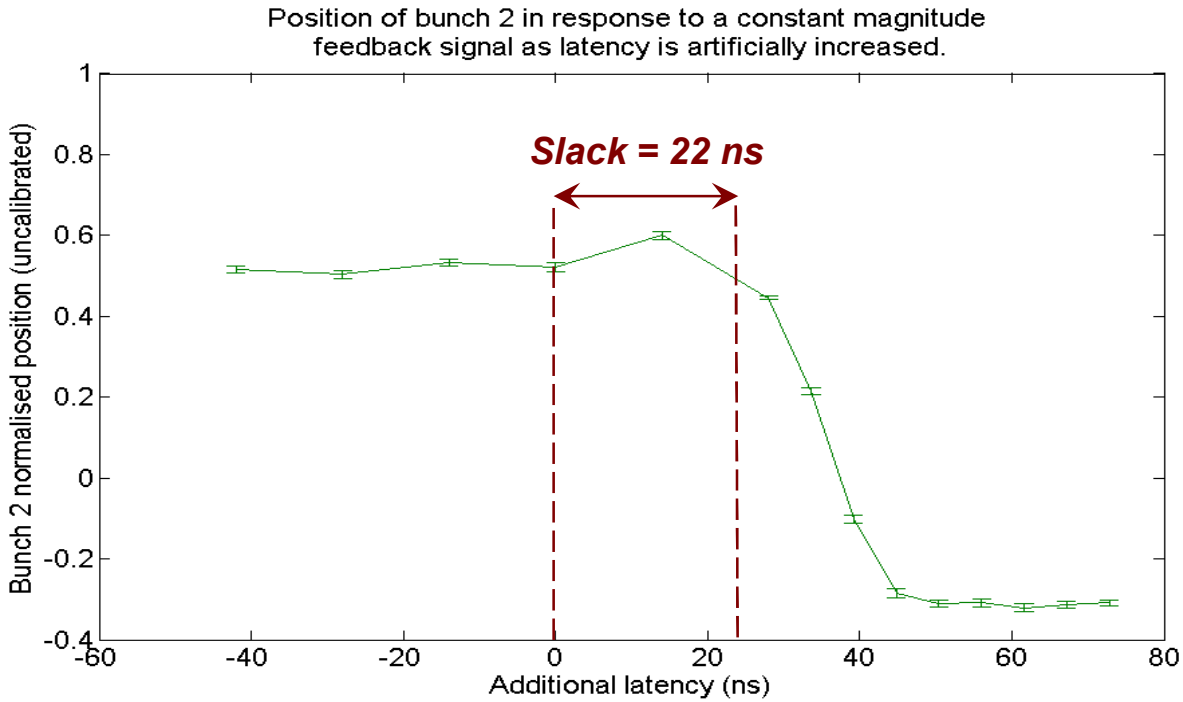


# Example (3) of Results



# Latency measurement




**Latency**

**= 154 - slack**

**= 132 ns**

**+ 8ns (1/Q)**

# CLIC feedback prototype status

# FONT Prototype Analogue Feedback Systems

- **NLCTA: 65 MeV beam, 170ns train, 87ps bunch spacing**

**FONT1 (2001-2):**

**First demonstration of closed-loop FB: latency 67ns**

**10/1 beam position correction**

**FONT2 (2003-4):**

**Improved demonstration of FB: latency 54ns**

**real time charge normalisation with logarithmic amplifiers**
**beam flattener to straighten train profile**
**solid-state amplifier**

- **ATF: 1.3 GeV beam, 56ns train, 2.8ns bunch spacing**

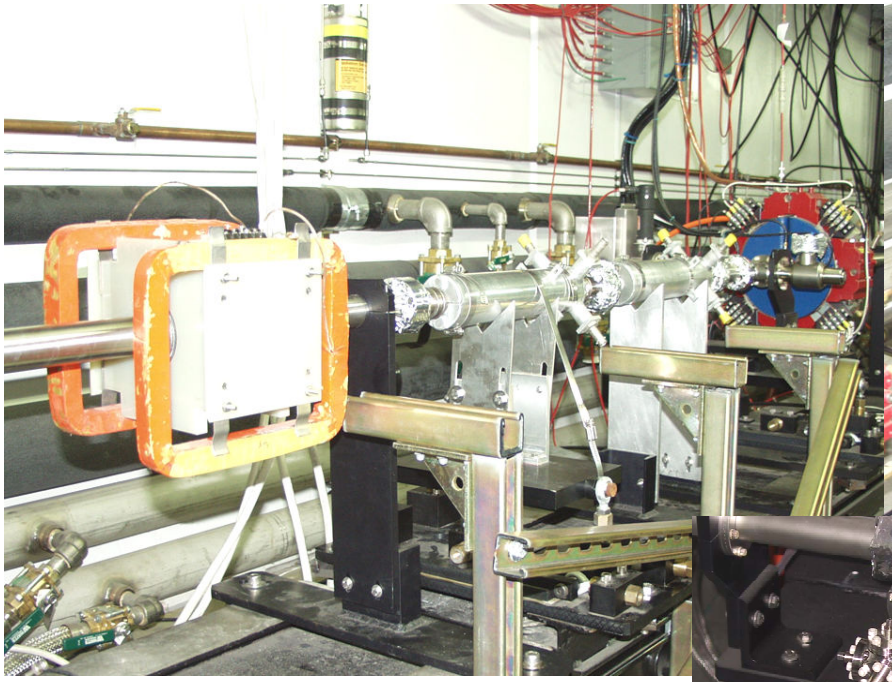
**FONT3 (2004-5):**

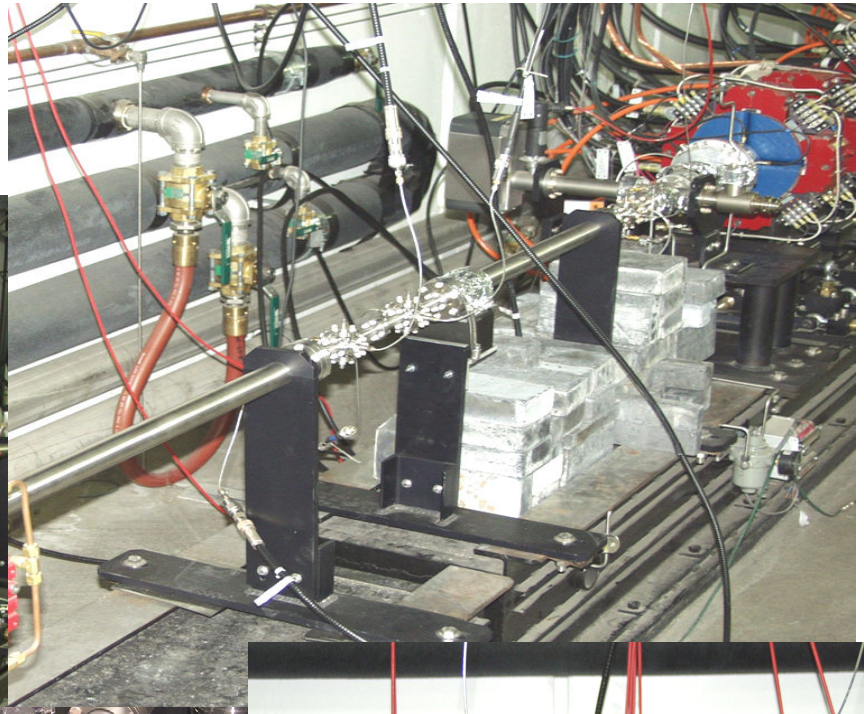
**Ultra-fast demonstration of FB: latency 23 ns**

**3 stripline BPMs**
**high-power solid-state amplifier**

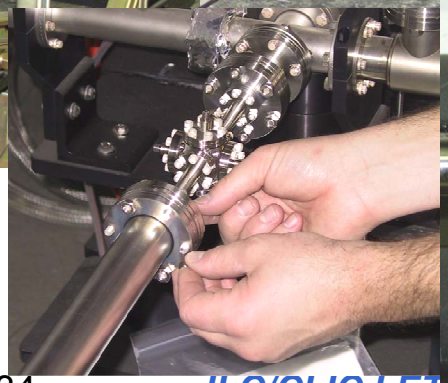
# FONT2 beamline installation at SLAC NLCTA
## (65 MeV 170ns-long train @ 87ns spacing)

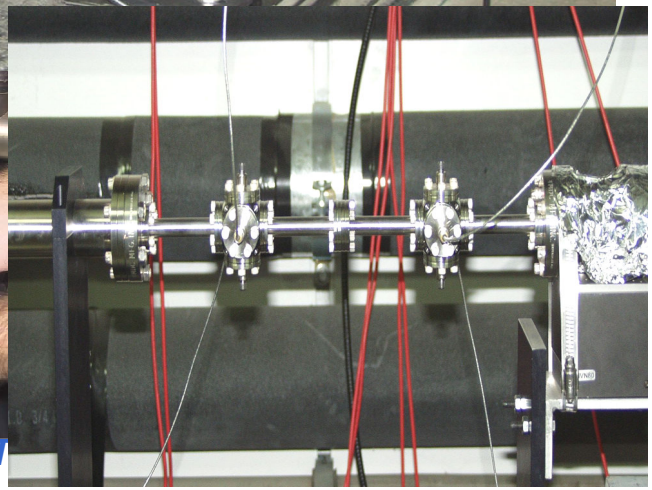
**Dipole and kickers**



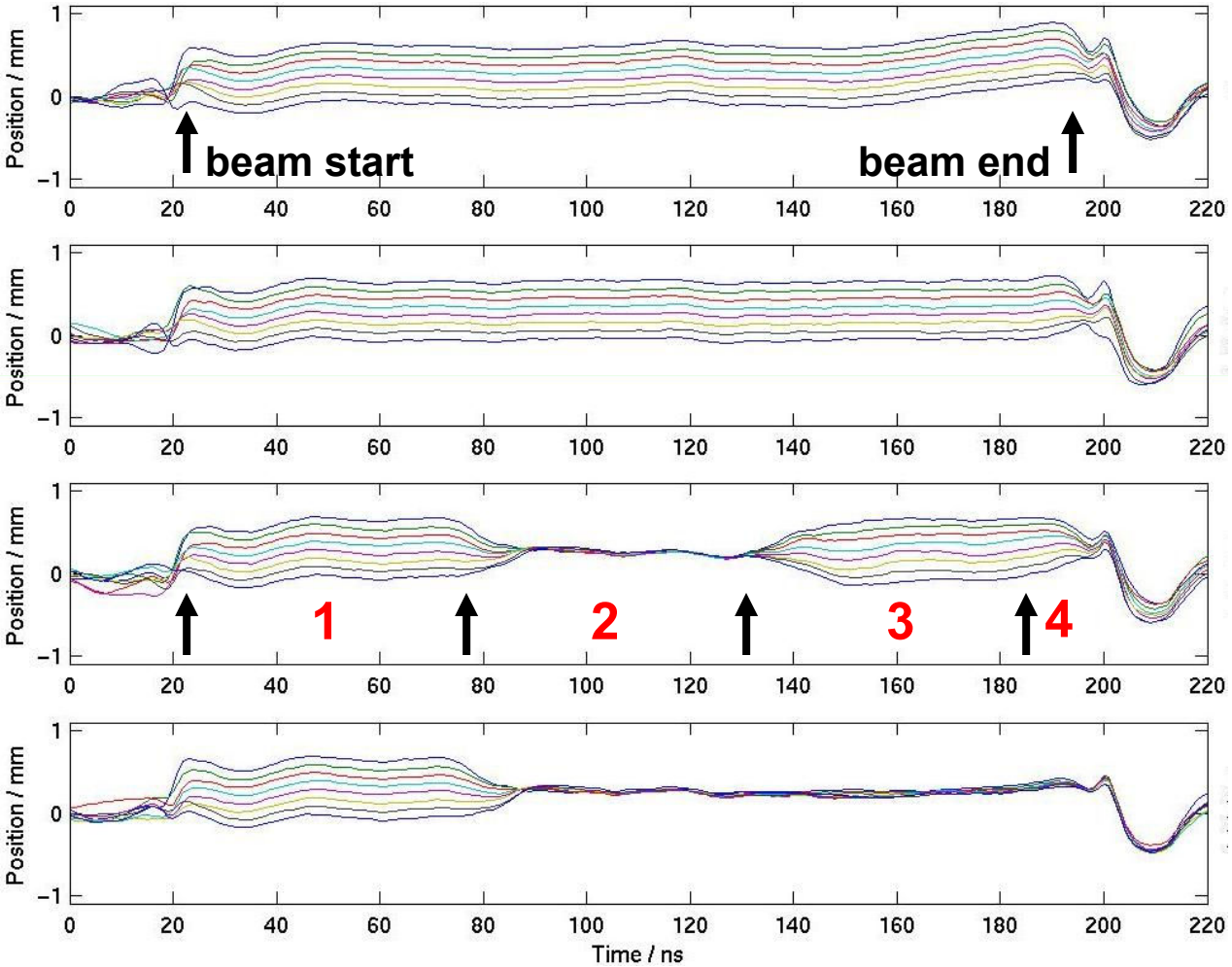


**New BPMs**





# FONT2 results: feedback BPM




Beam starting positions

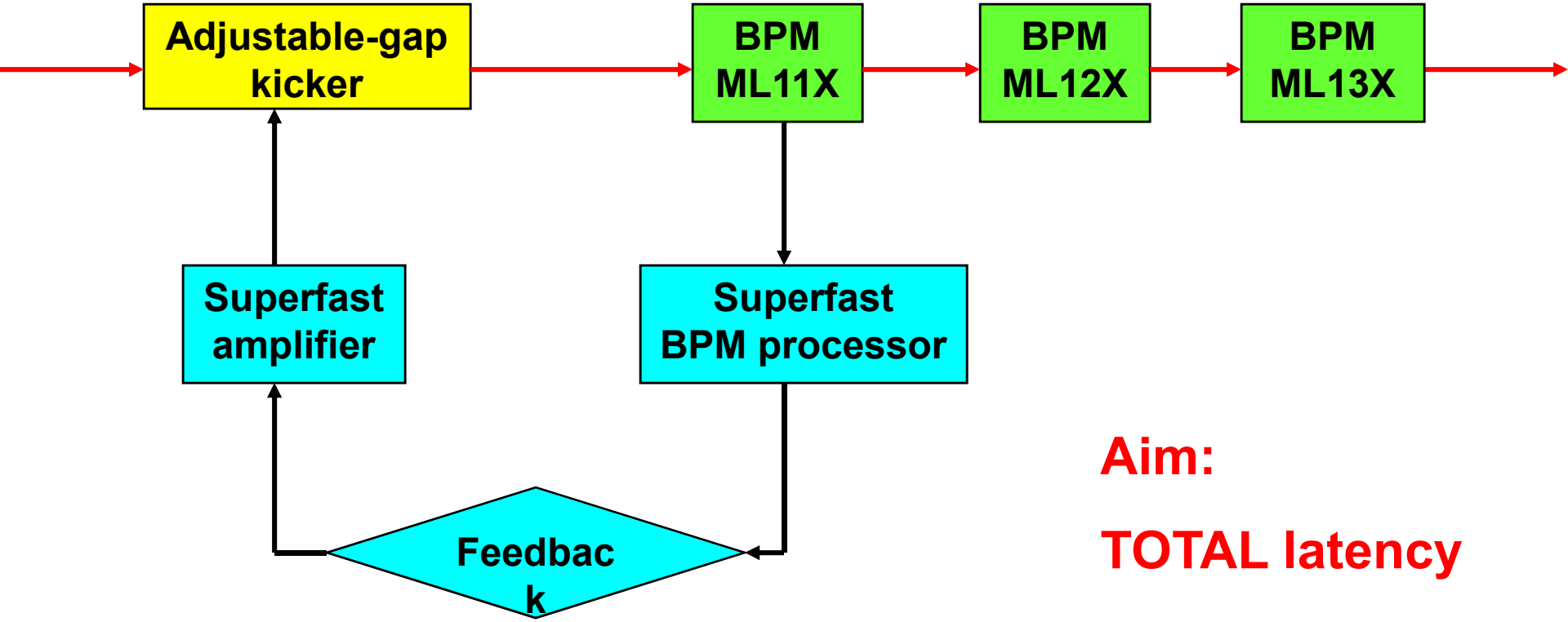
Beam flattener on

Feedback on

Delay loop on

# FONT3

## ATF: 1.3 GeV beam, 56ns-long train @ 2.8ns spacing




**Aim:**

**TOTAL latency**

**< 20 ns**

# FONT3: latency budget

- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 6ns

  Irreducible latency: 10ns

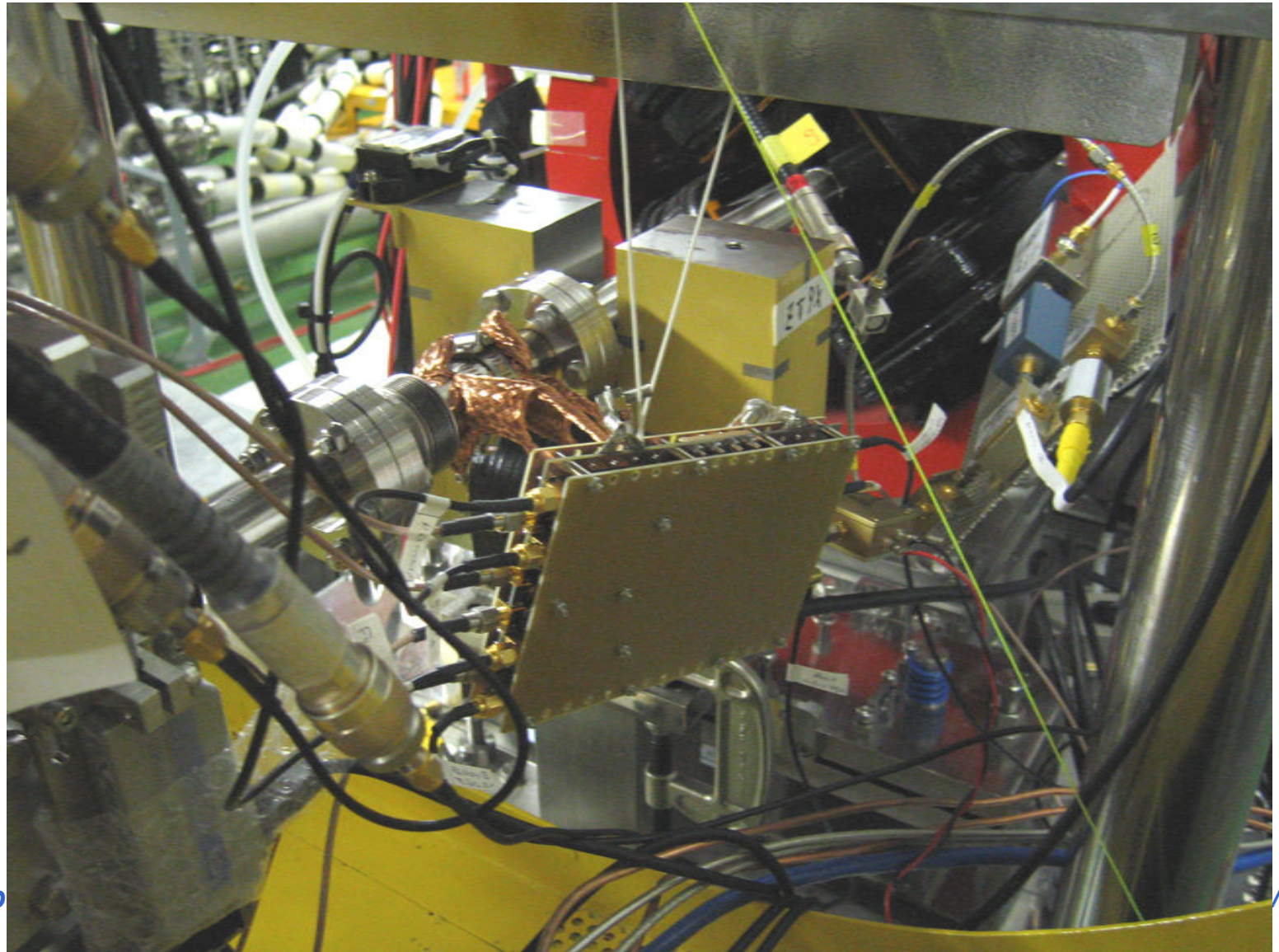
- BPM processor: 5ns
- Amplifier + FB: 5ns

  Electronics latency: 10ns

- Total latency budget: 20ns

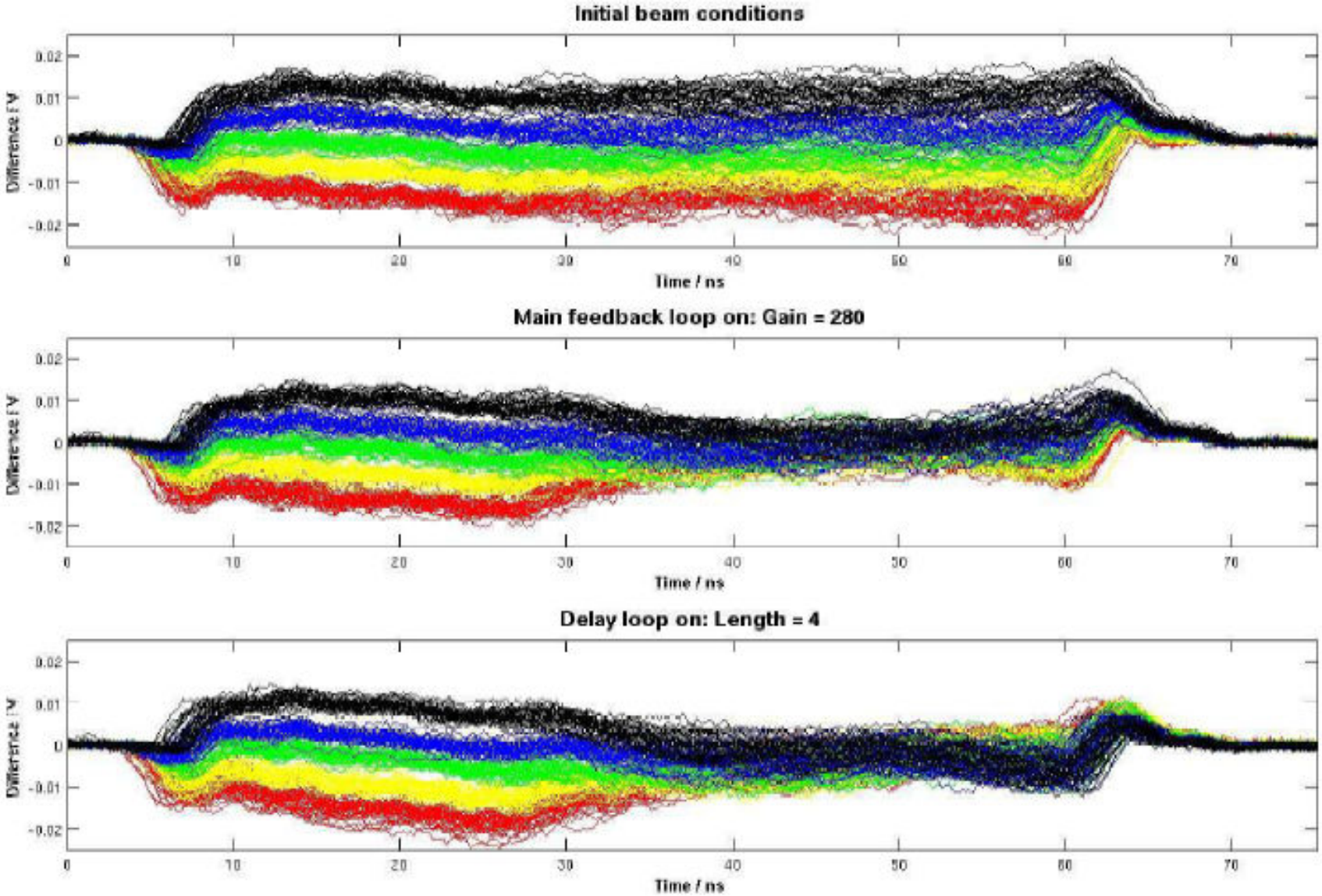
Allows 56/20 = 2.8 periods during bunchtrain

# FONT3: Beamline Installation

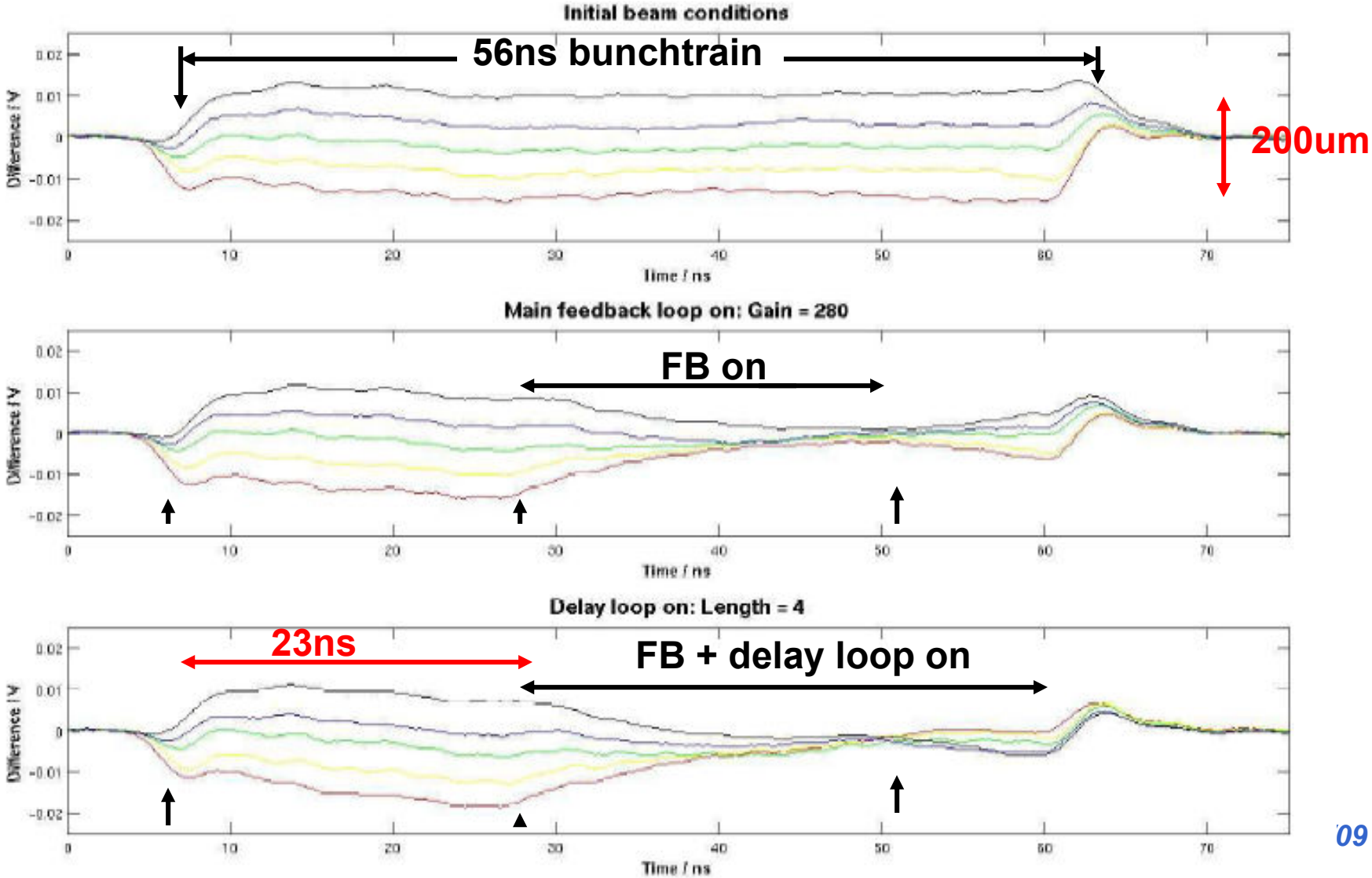


# FONT3: Results (June 3 2005)

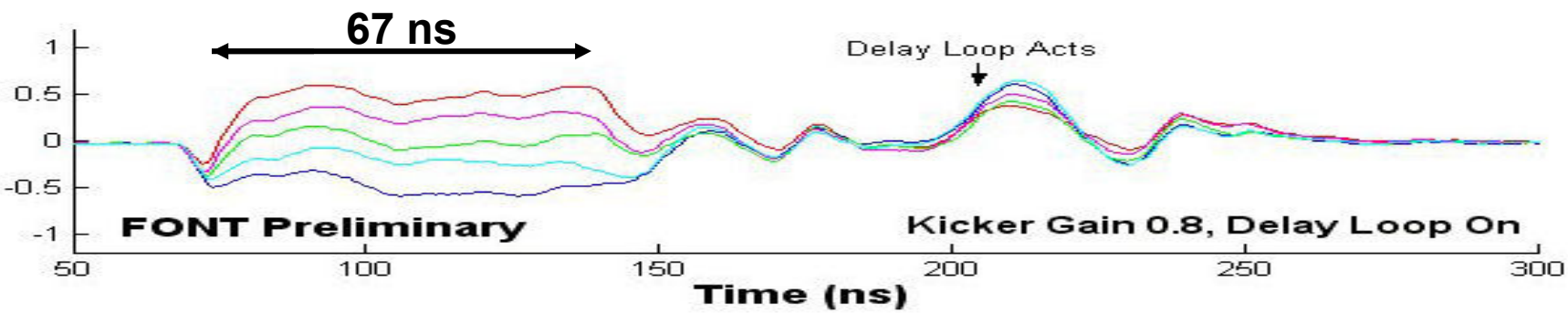
## 40 pulses per position setting

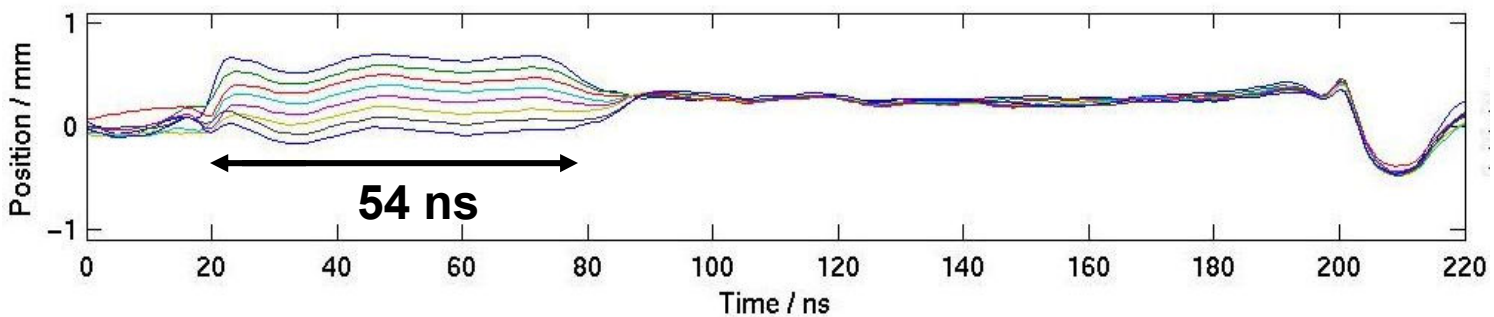


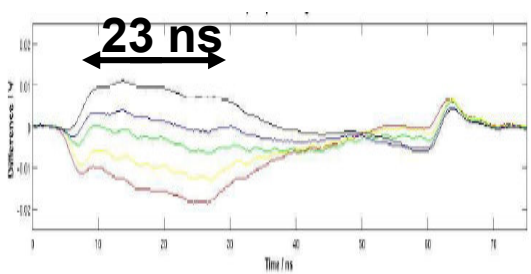
# FONT3: Results (June 3 2005):
## Delay-loop feedback w. latency 23 ns



# FONT1,2,3: Summary




**Fast enough for CLIC intra-train FB!**

# IP feedback engineering considerations

System component locations + specs listed in ILC RDR

No detailed engineering work done in terms of:

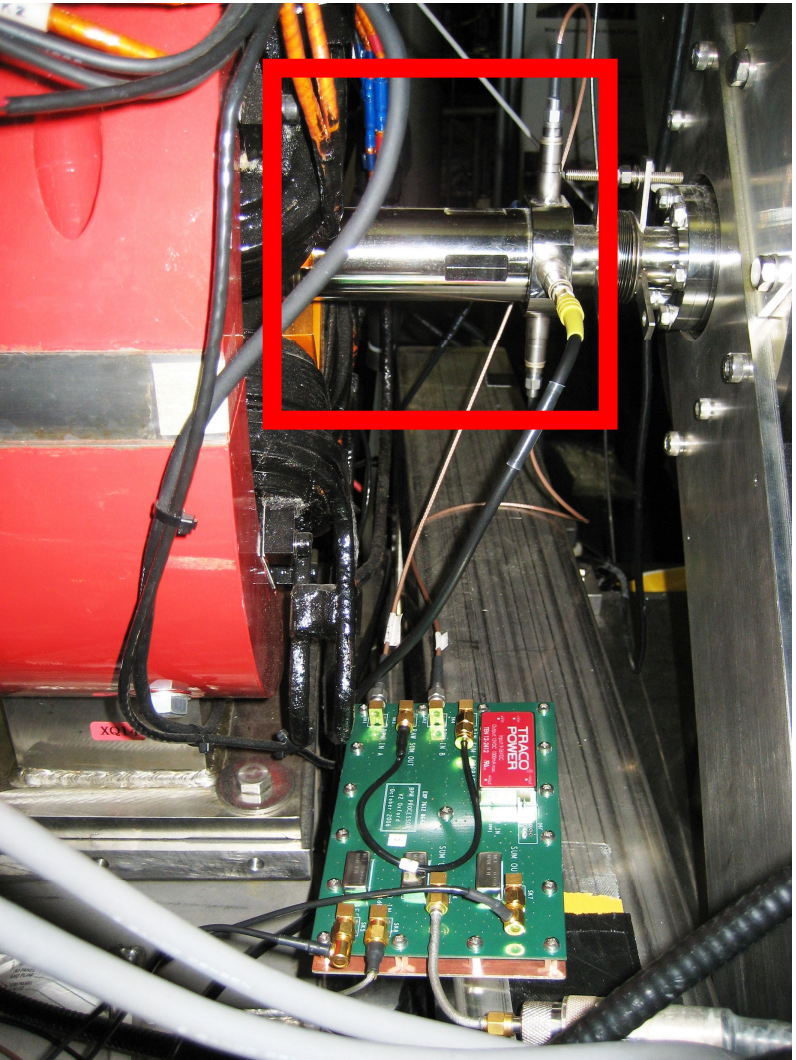
- actual designs of BPM and kicker
- integration into beamline design

However, components are envisaged to be 'standard':

| | |
|---|---|
| Stripline BPM c. 10-20cm long | (ATF: 12.5cm) |
| Stripline kicker c. 30-60cm long | (ATF ~ 30cm) |
| Stripline radius c. 1-2cm | (ATF ~ 1cm) |

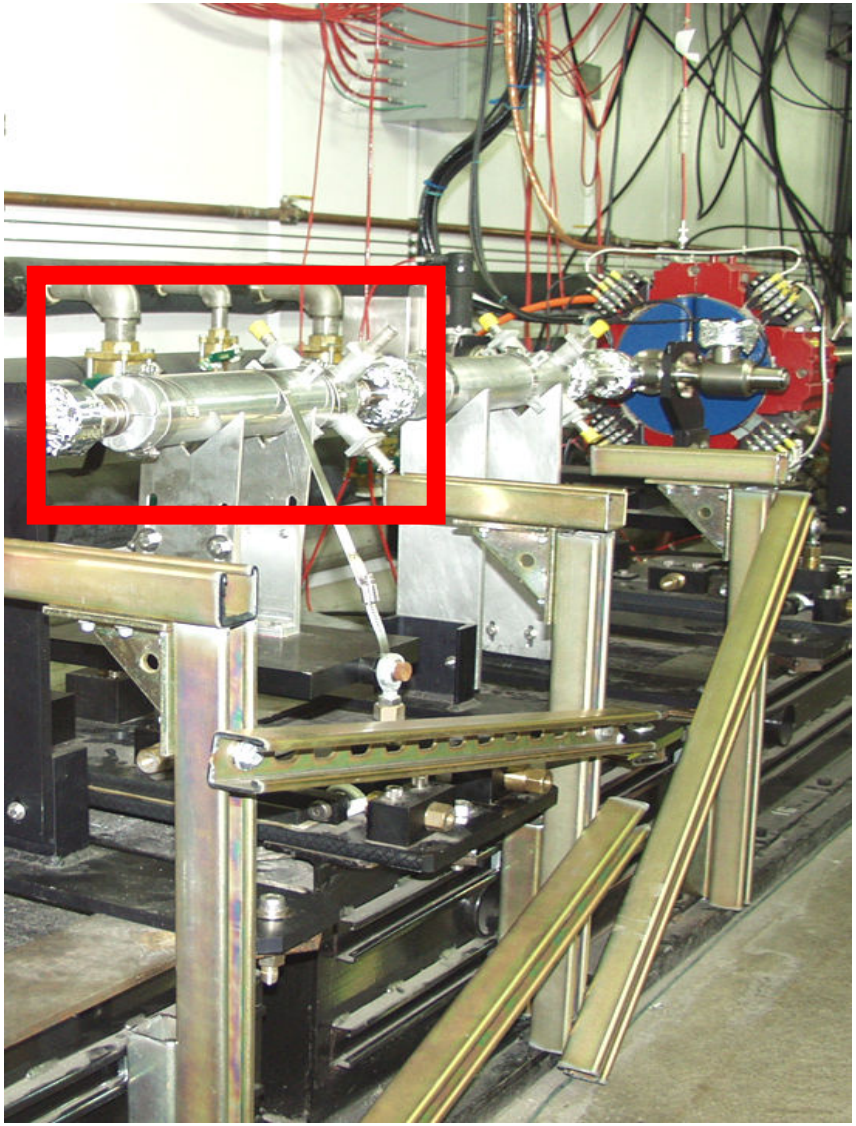
Possibly want to customise design to fit into tight beamline environment

# BPM engineering issues




- Connections to BEAMCAL, QD0 cryostat?
- Bellows, at both ends?
- Shorten pickoffs?
- Electronics off to side and shielded?
- Define cable runs: door opening, push-pull?

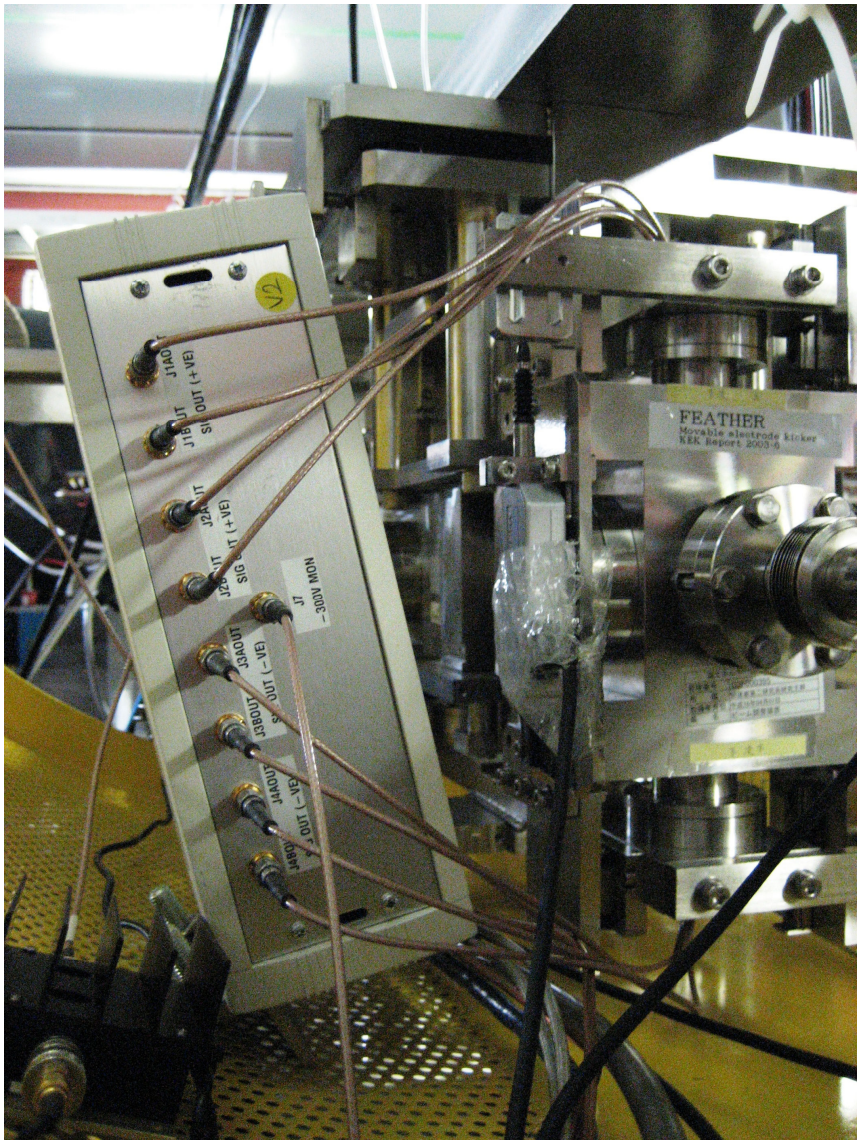
# Kicker engineering issues



**Real-estate more generous**

- **Does warm section move with detector in push-pull?**
- **Amplifier detector-side or machine-side of break?**
- **Flanges, bellows, at both ends?**
- **Shorten pickoffs?**

# Amplifier engineering issues




**FONT4 amplifier performance:**

**Kicker 30cm long, 2cm aperture, 1kW drive**

**100 nrad deflection**
**(250 GeV beam)**

**lever arm 4m**
**+- 400 nm at IP**
**( > 50 sigma_y)**

**Kick ~ I, 1/r, sqrt(P), 1/p …**

# Summary and issues

**Several prototype intra-train feedbacks developed by FONT**

**Detailed mechanical/integration engineering needs to be done for ILC and more work on conceptual design for CLIC**

**Radiation environment for BPM electronics, feedback electronics, kicker amplifier:**

**radiation tolerance, locations, shielding …**

**EM interference:**

**Pickup on BPM or kicker**

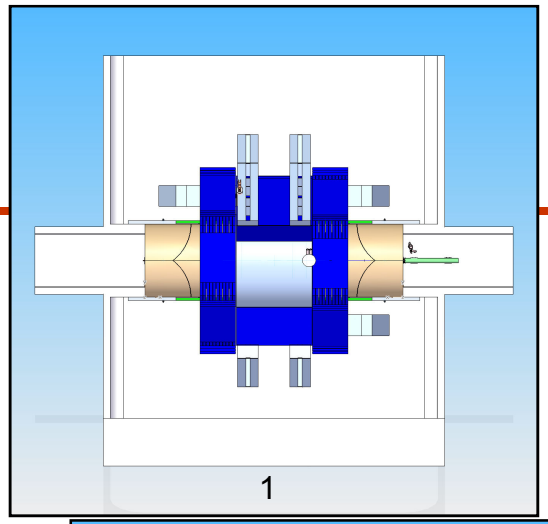
**Broadcast RF (eg. to detector!)**

**Ground loops**

**Interface to BEAMCAL for luminosity scan system**

# Extra material

# Detector opening on the beam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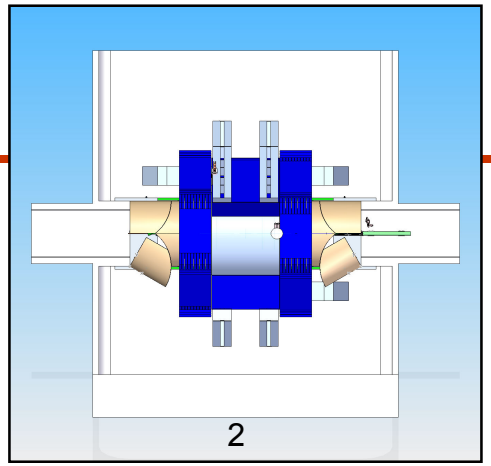
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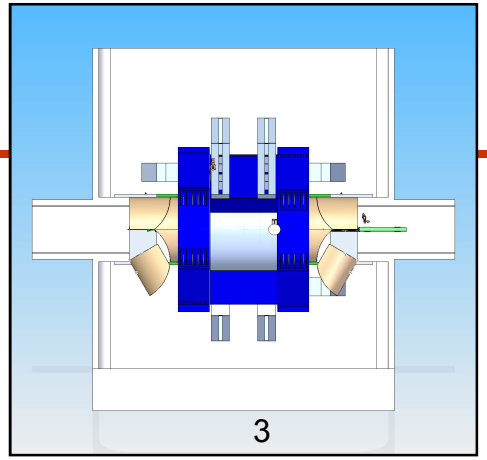
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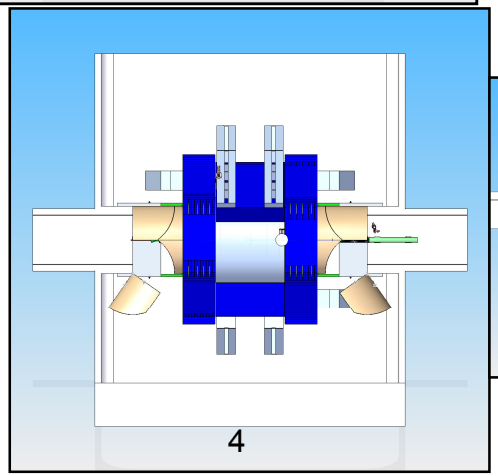
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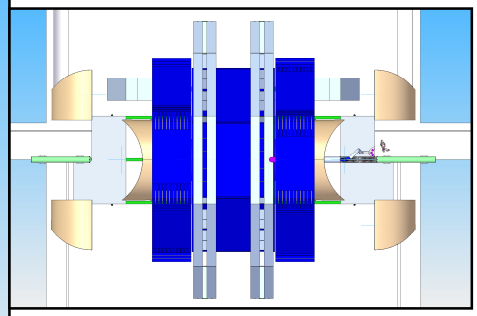
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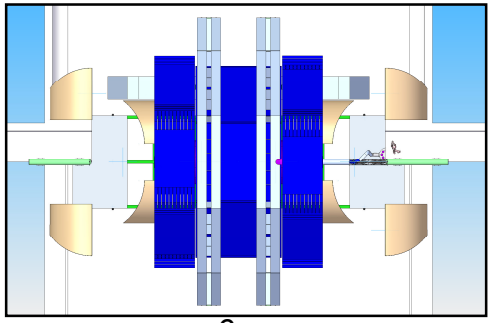
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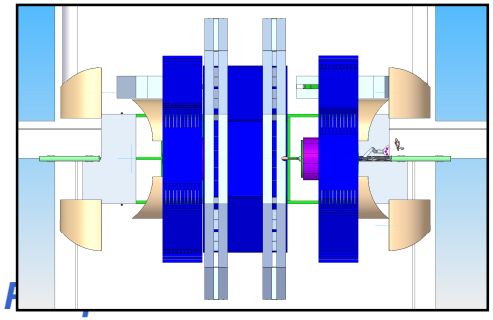
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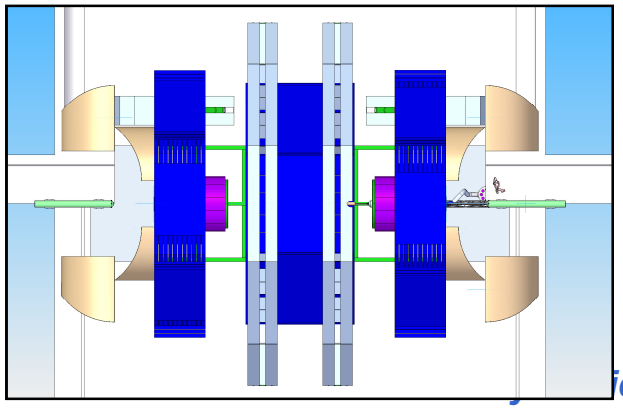
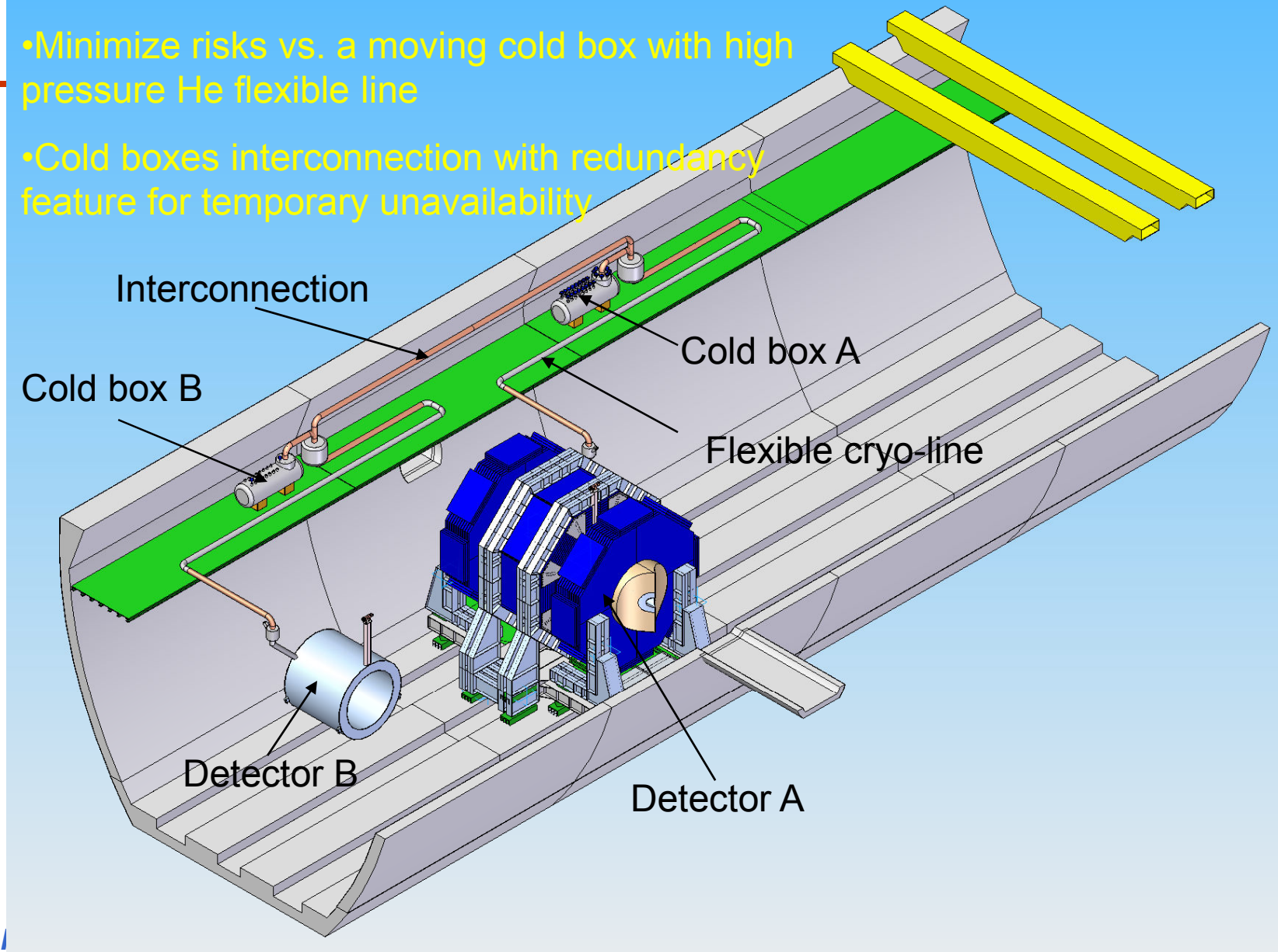
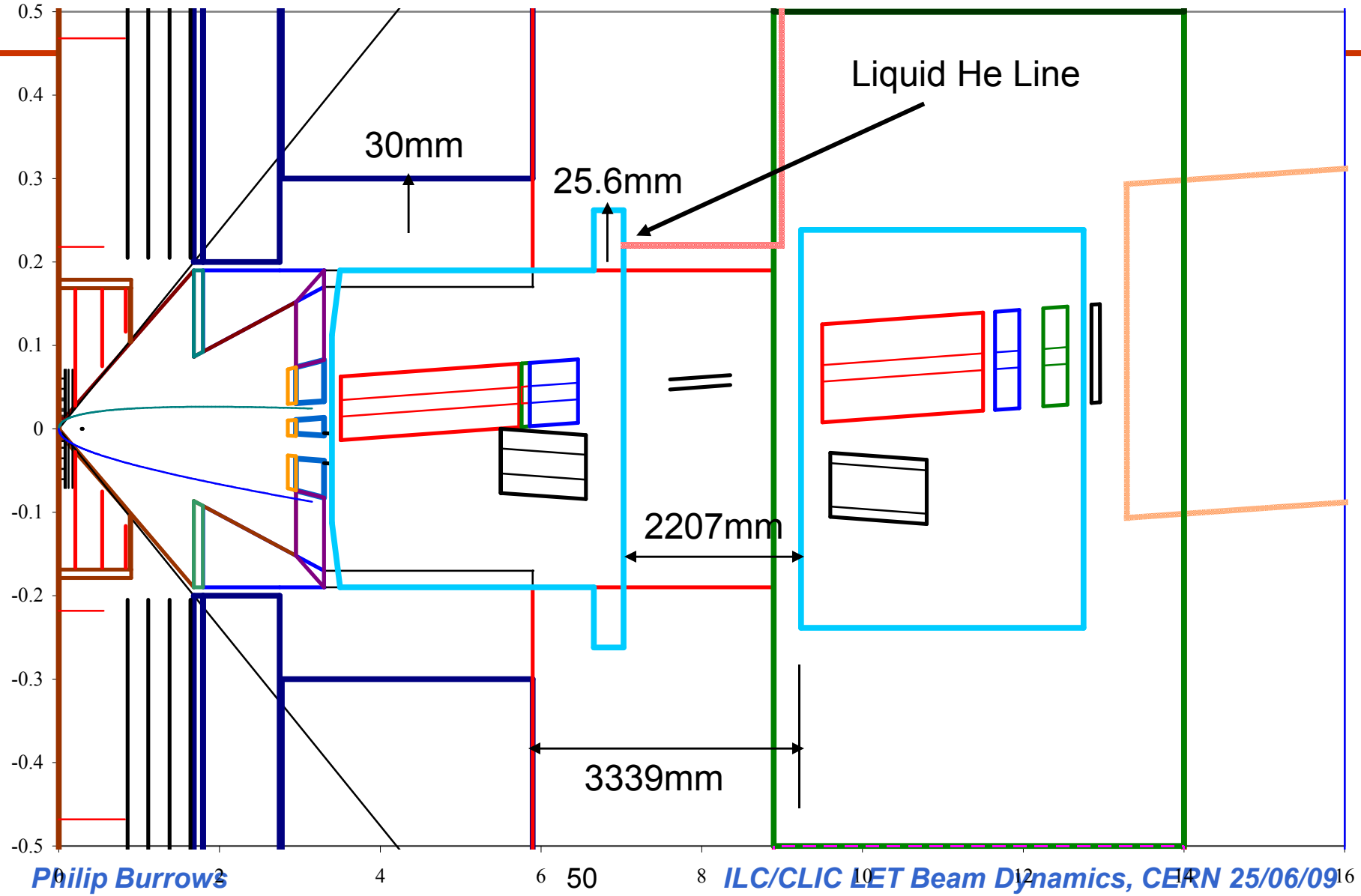

8

# Cryogenics system design for push-pull

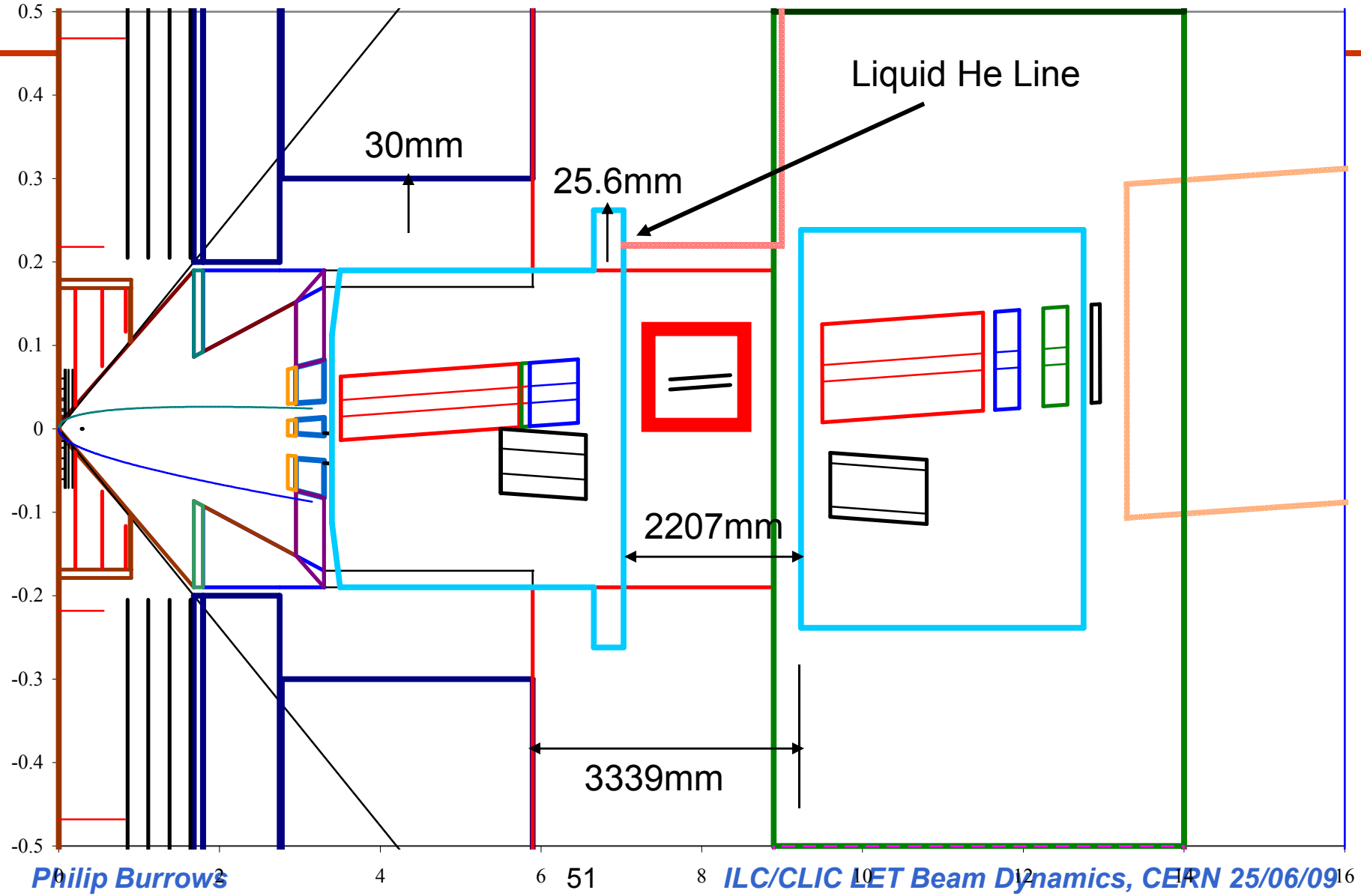
- Stationary cold box with flexible cryo-transfer line
- Minimize risks vs. a moving cold box with high pressure He flexible line
- Cold boxes interconnection with redundancy feature for temporary unavailability



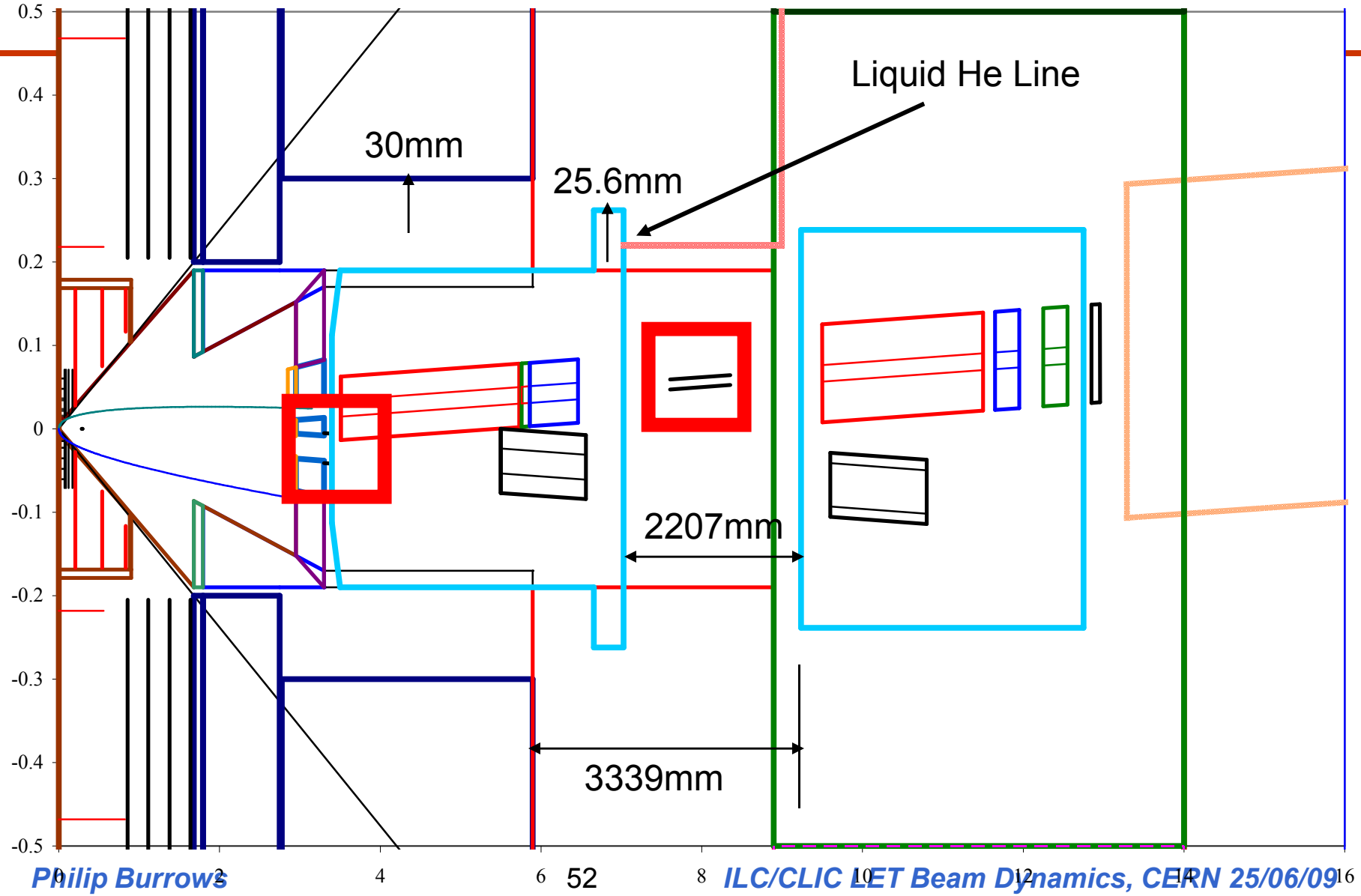
# Location of FB hardware (SiD, L*=3.7m)



# Location of FB hardware (SiD, L*=3.7m)



# Location of FB hardware (SiD, L*=3.7m)



# Zoom-in showing BPM location