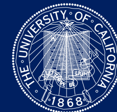
Radiation Effect Studies on ALPIDE at 88” Cyclotron

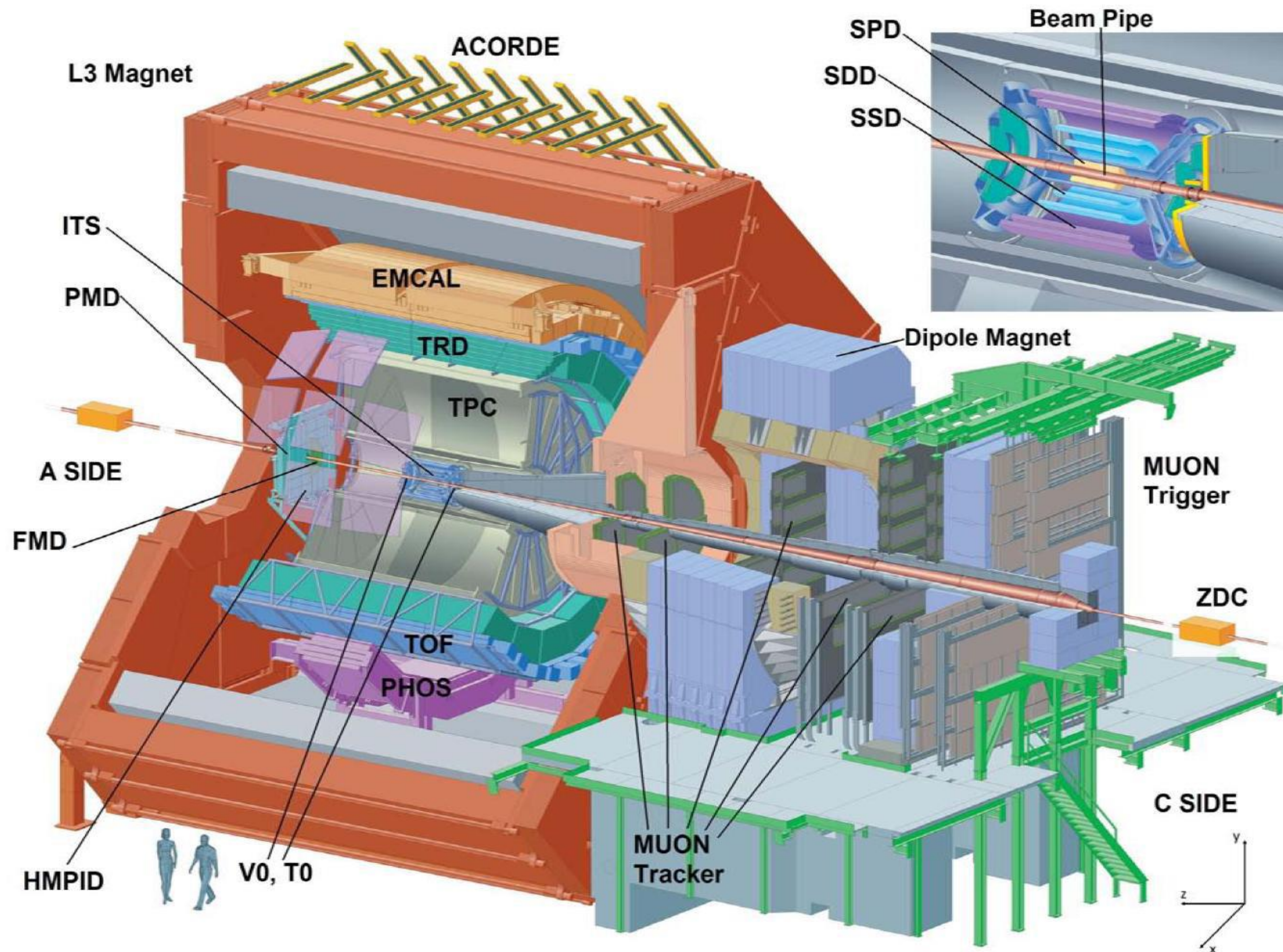
Joanna Szornel

US LHC User’s Meeting

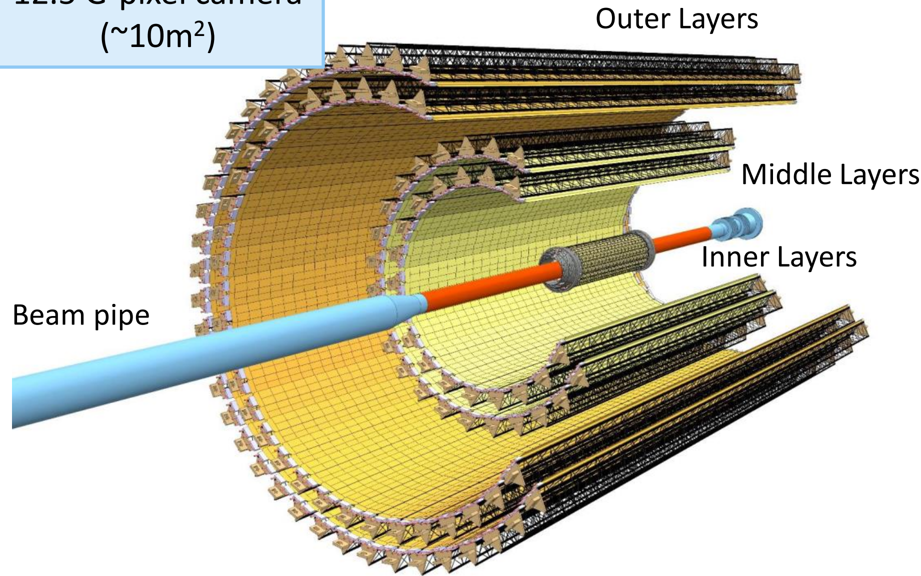
November 2016



The ALICE Experiment



ALICE Inner Tracking System (ITS) Upgrade



7-layer barrel geometry

- r coverage: 23-400 mm
- η coverage: |η| ≤ 1.22
- 3 Inner Barrel layers (IB), 4 Outer Barrel Layers (OB)
- Material/layer: 0.3% X_0 (IB) 0.8% X_0 (OB)
- To be installed 2020

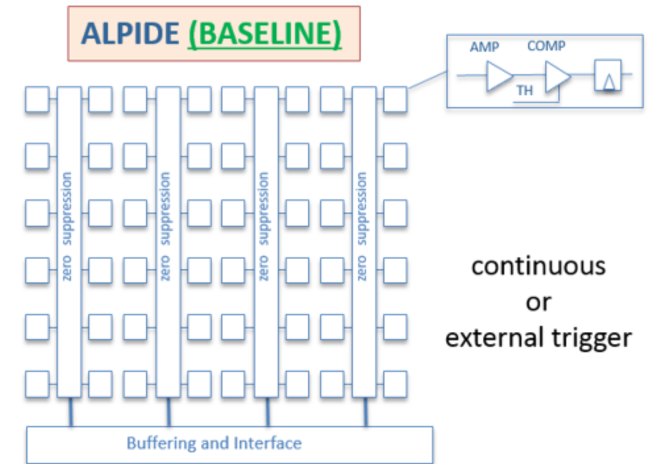
The new ITS will allow the study of:

- Thermalization and hadronization of heavy quarks in Quark Gluon Plasma (QGP)
- Heavy quark in-medium energy loss and its mass dependence
- Thermal radiation from Quark Gluon Plasma (QGP) via photons detected as di-electrons

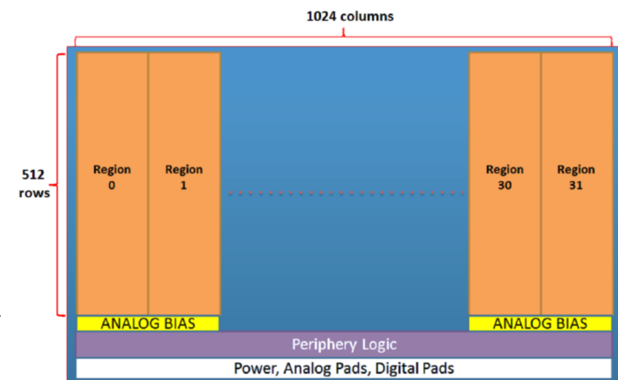
Joanna Szornel | jszornel@berkeley.edu

ALPIDE (ALICE PIxel DEtector)

- Designed for the new Inner Tracking System
- Monolithic Active Pixel Sensor (MAPS) technology
  - Sensitive volume and front end electronics in the same silicon wafer
  - Lower pixel pitch, extremely low material budget
- Each pixel contains analog and digital sections
- Characterized single event effects for ALPIDE prototypes
  - Single Event Latch-ups for ALPIDE-1, ALPIDE-3, ALPIDE-4
  - Single Event Upsets for ALPIDE-4



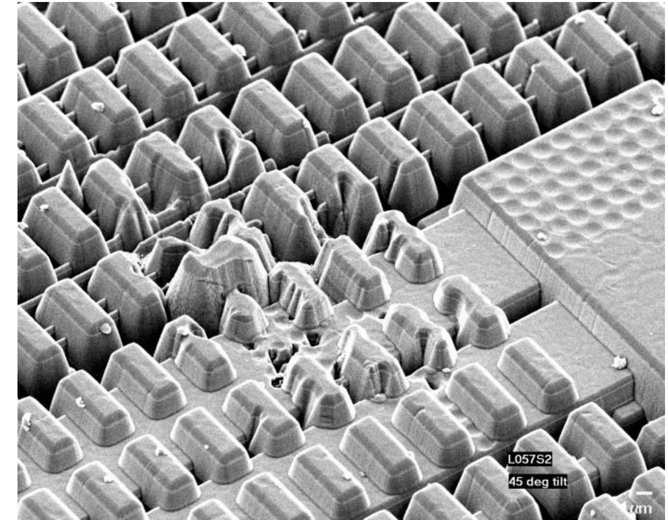
ALPIDE matrix



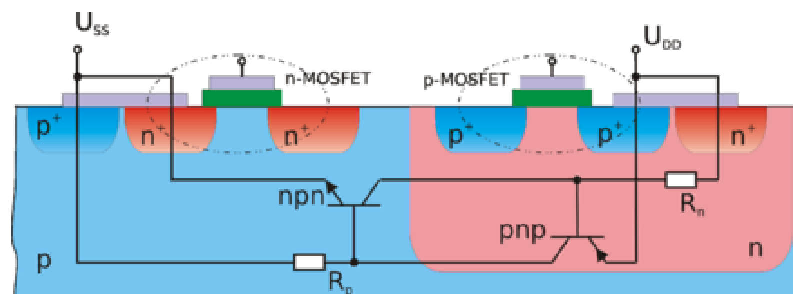
ALPIDE block diagram showing matrix (blue, orange) and periphery (purple)

Single Event Latch-up (SEL)

- Common problem with CMOS technology
- A heavy ion travels through and creates a low impedance path, which results in an uncontrolled increase in current
- The parasitic structure exhibits positive feedback and will continue to exist unless power-cycled
- Can cause permanent damage



STAR HFT pixel layers deconstructed and imaged (with SEM).
Layers appear to have melted.



parasitic structure

ALPIDE SEL Tests

Use cocktail beam at 88-inch cyclotron with various ions with different Linear Energy Transfer (LET) values.

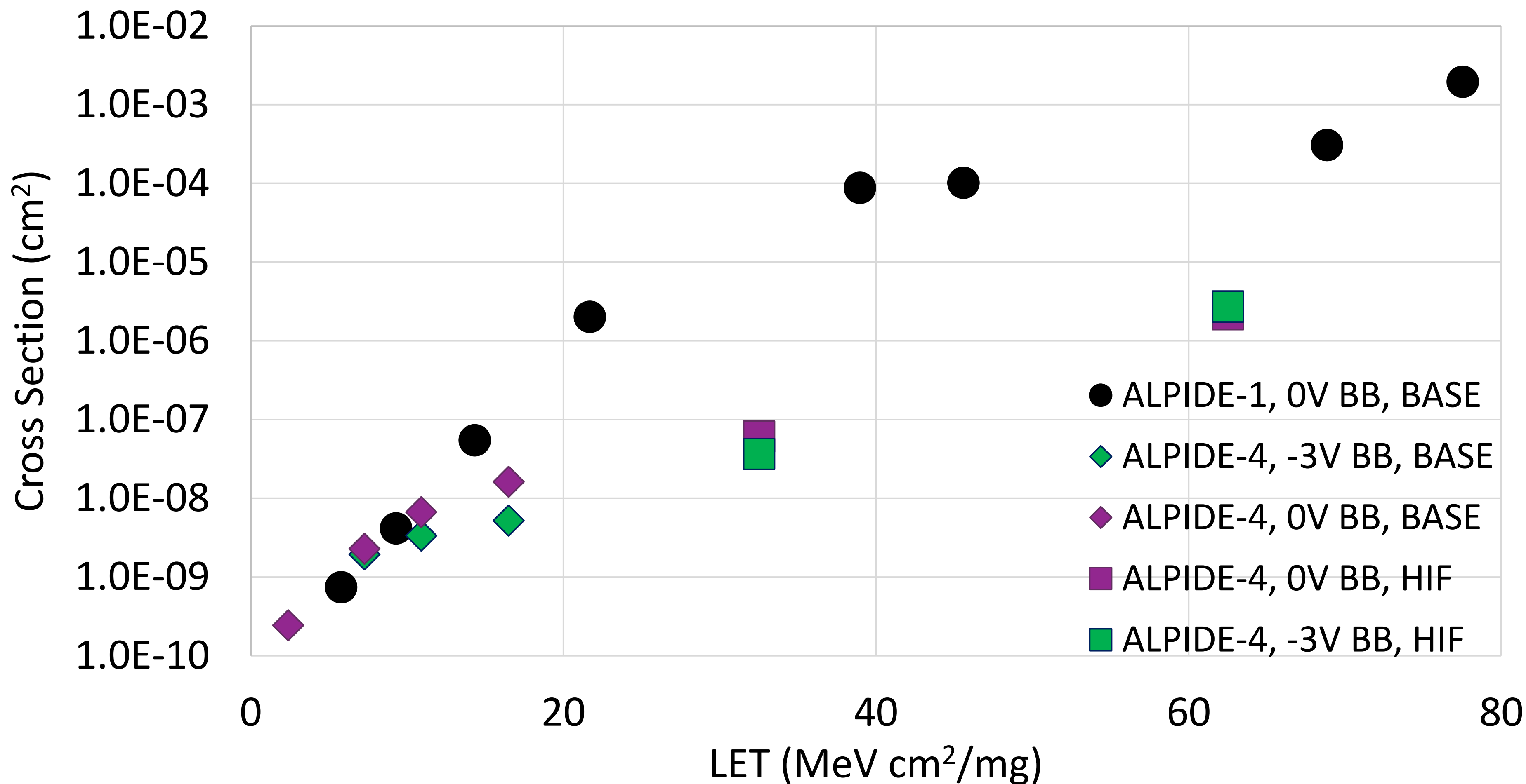
Objectives:

- Determine ALPIDE-4 SEL sensitivity and compare with previous prototypes (ALPIDE-1, ALPIDE-3)
- Study current profiles

These tests helped identify regions particularly susceptible to latch-up and find design changes to mitigate latch-up sensitivity

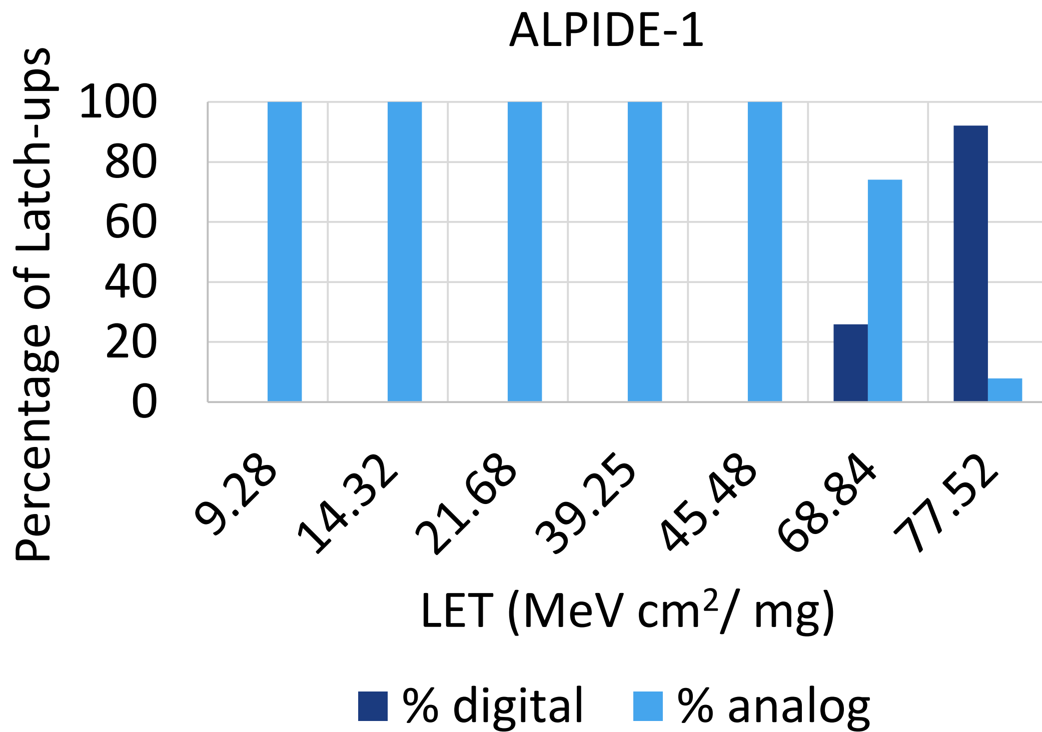
ALPIDE-1		ALPIDE-4	
Ion	LET (MeV cm^2/mg)	Ion	LET (MeV cm^2/mg)
Ne	5.77	Ne	2.39
Si	9.28	Ar	7.27
Ar	14.32	V	10.9
V	21.68	Cu	16.53
Kr	39.25		
Y	45.58		
Xe	68.84		
Tb	77.52		

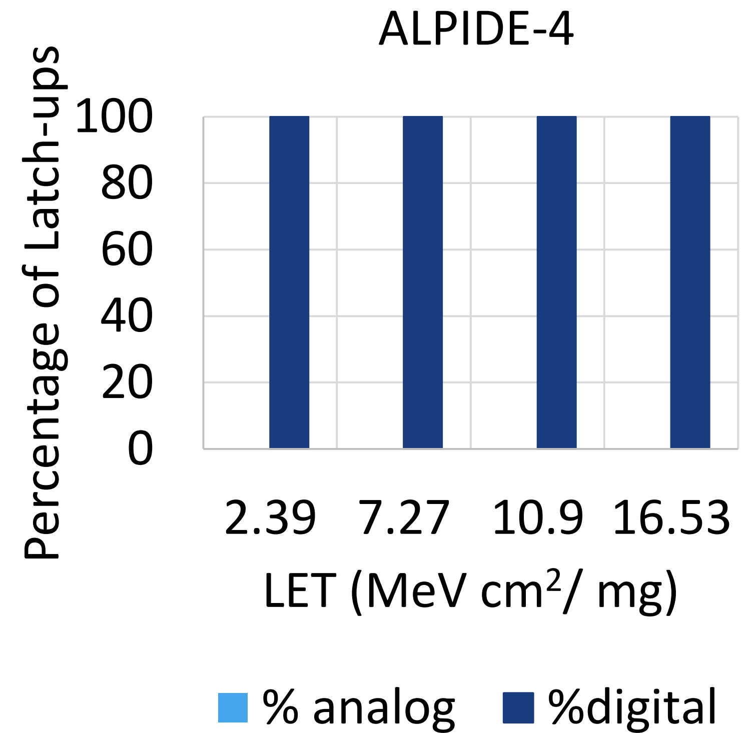
ALPIDE-1 and ALPIDE-4 SEL Results



ALPIDE-4 has decreased susceptibility to latch-up, compared to ALPIDE-1

Relative Latch-ups





- In ALPIDE-1, latch-ups in analog blocks were prevalent
- In ALPIDE-4, latch-ups seen only in digital blocks

Single Event Upset (SEU)

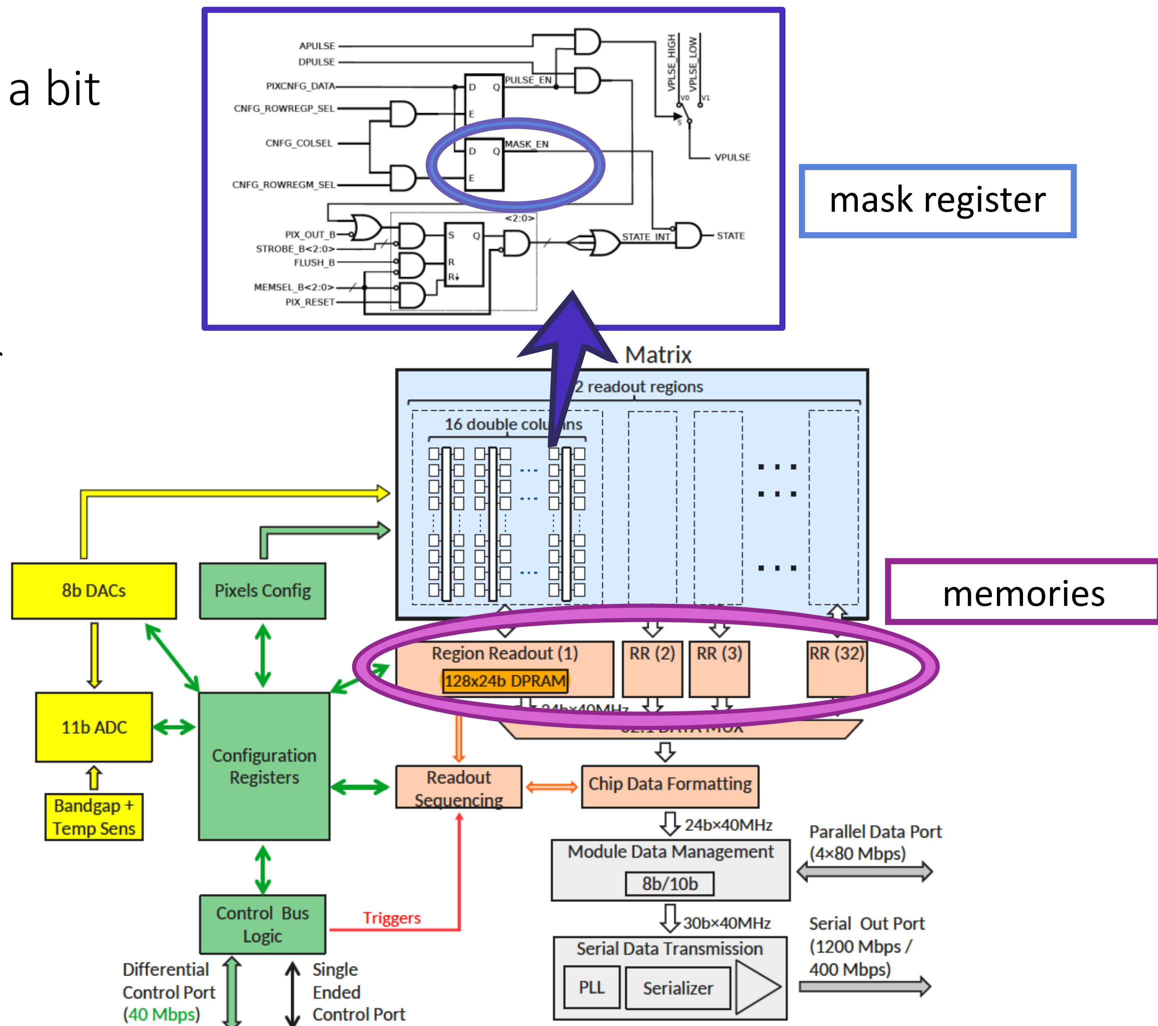
SEU: An ionizing particle causes a bit flip in a register

Goals:

- Determine cross section for SEU
- Study dependency of cross section on bias voltage

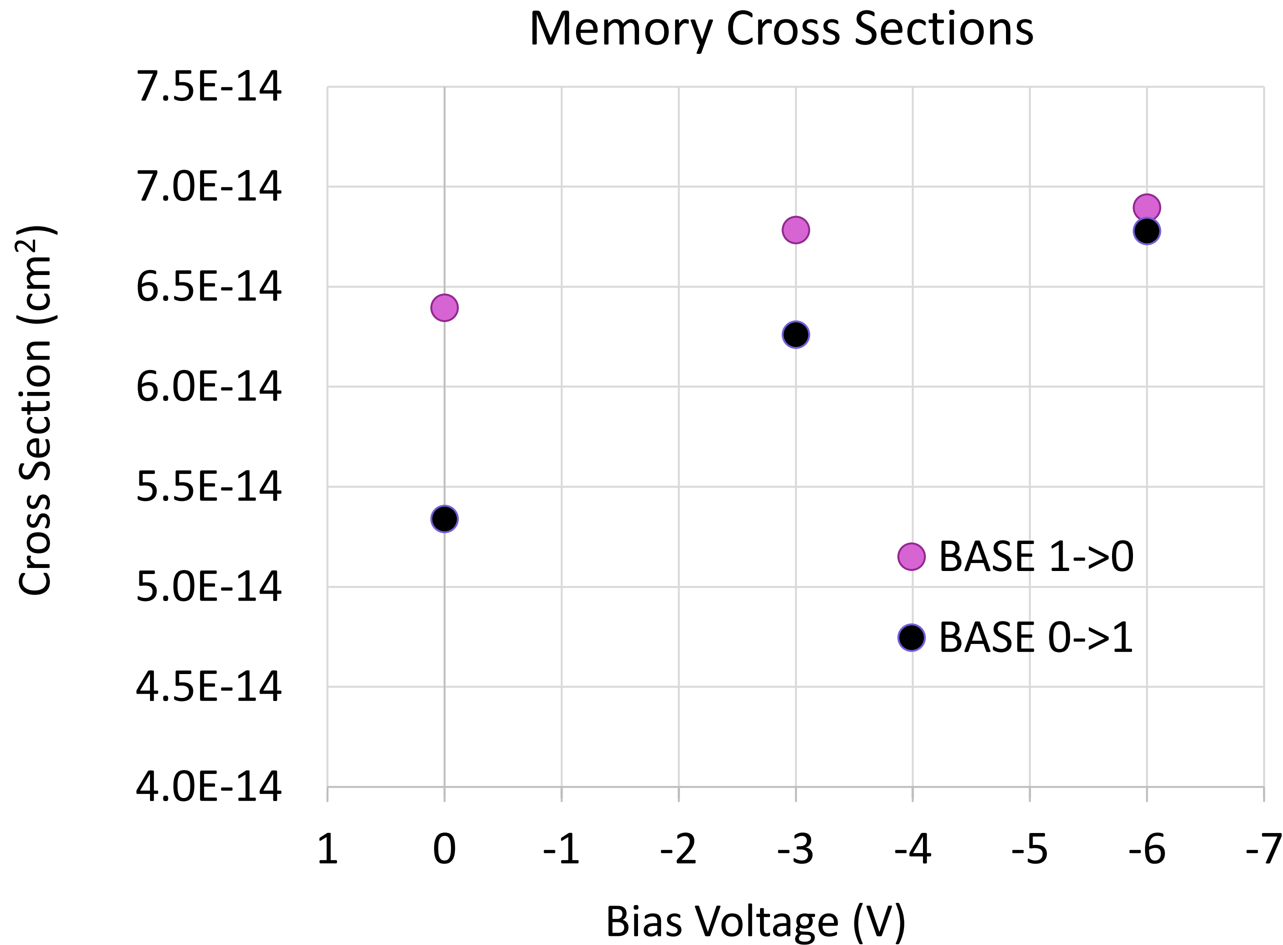
Tests performed on:

- In-pixel mask registers
- memories



ALPIDE Block Diagram

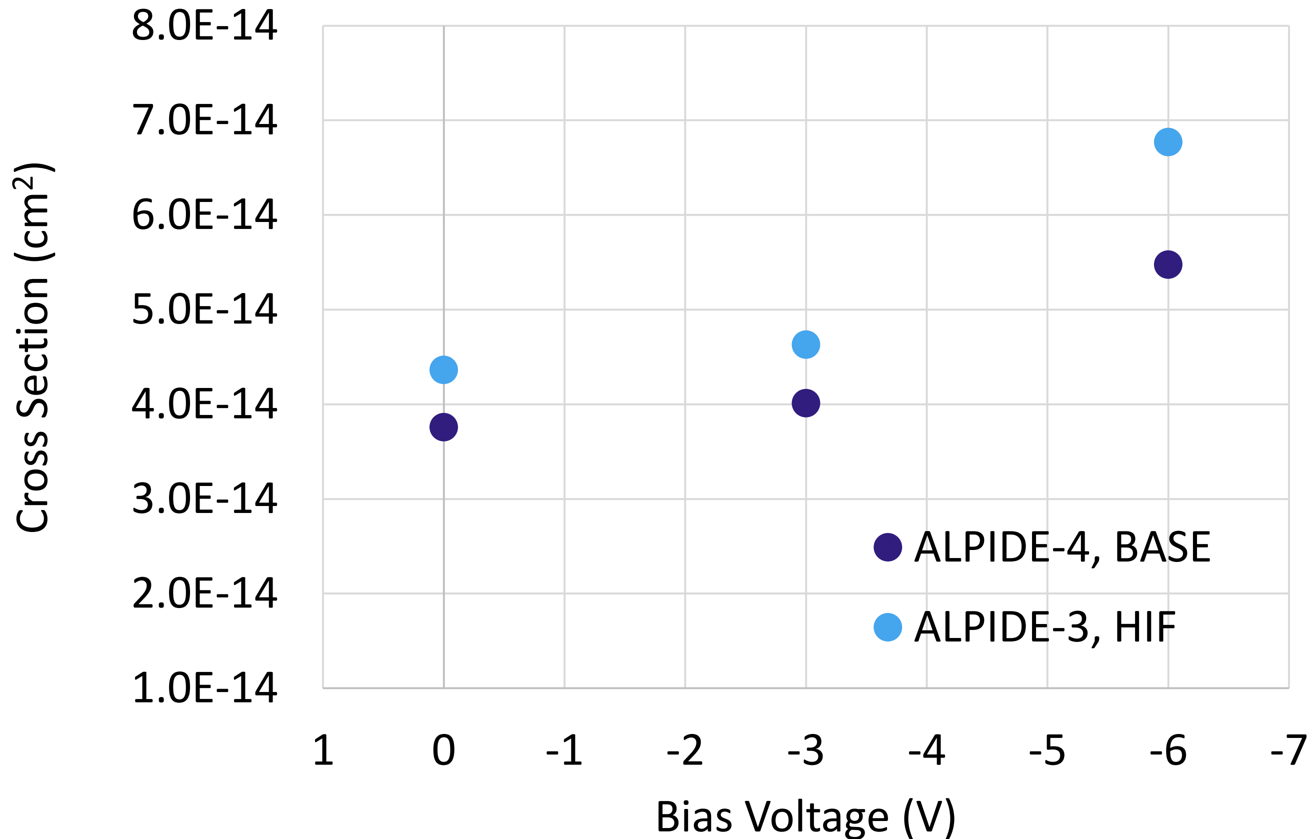
SEU Memory Cross Sections



In the memory block tested:

- 1 → 0 bit flips are more likely than 0 → 1 bit flips
- Bias voltage affects cross section

SEU Mask Bit Cross Sections



In the mask registers:

- ALPIDE-4 has similar cross sections to ALPIDE-3 (as expected)
- Bias voltage affects cross section

Summary

For ALPIDE prototypes characterized cross section for:

- Single Event Latch-ups
- Single Event Upsets

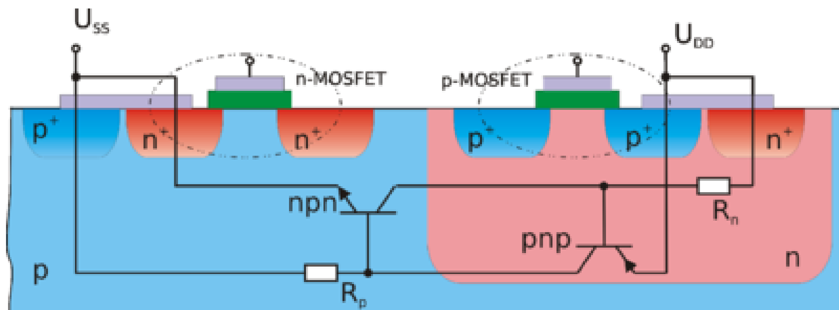
ALPIDE-4 has decreased susceptibility to latch-up, compared to ALPIDE-1

- Improvement at high LET values
- Analog cross sections improved at all LET values

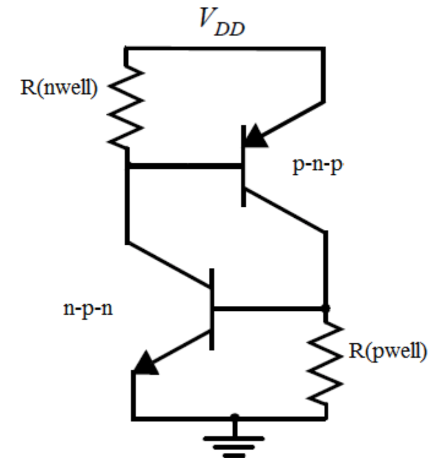
Bit flips in memories and mask registers show dependence on bias voltage. This is currently being studied.

Backup

Single Event Latch-up (SEL) Mitigation

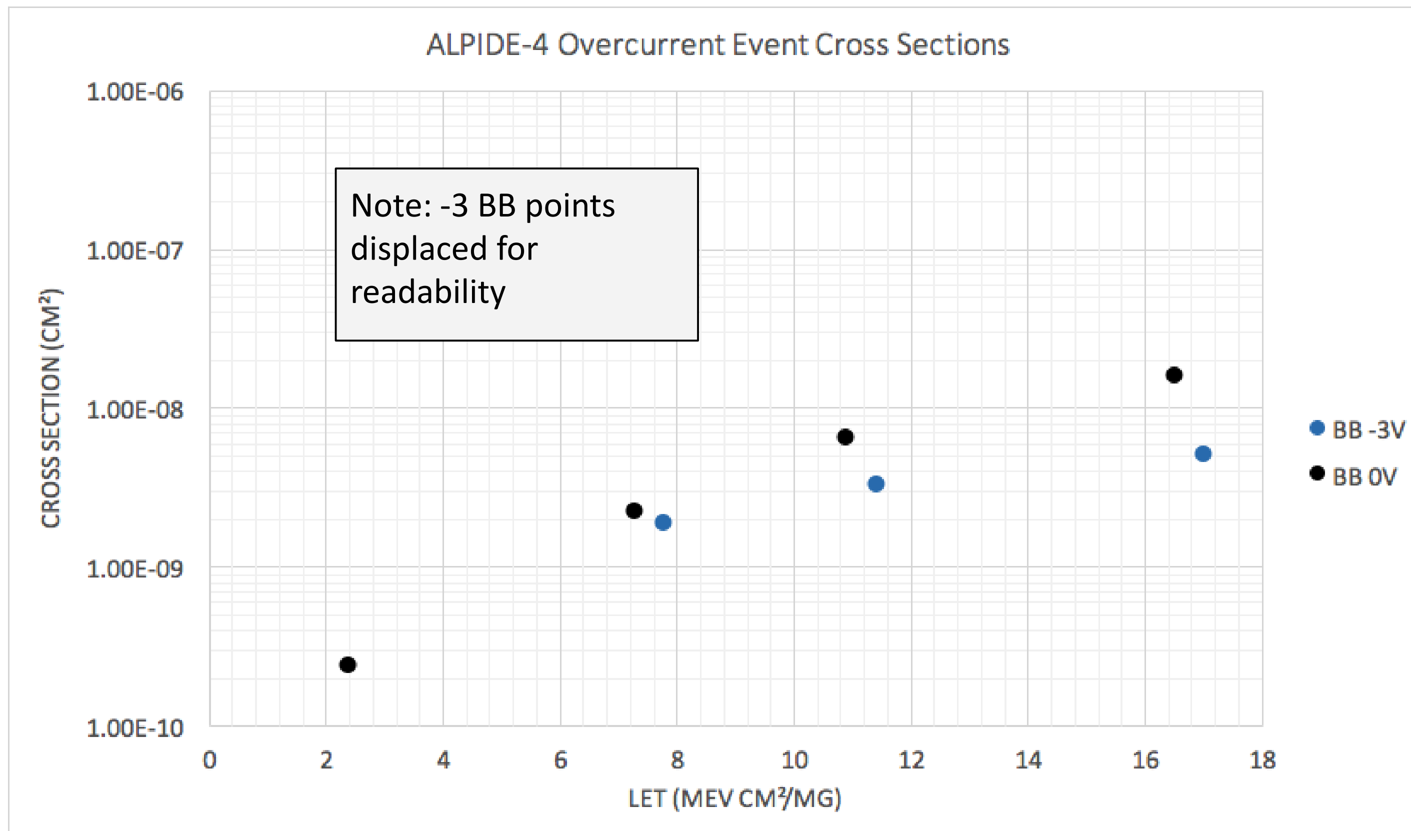


parasitic structure



Contact area of the p^+ wells inside the matrix was increased to reduce the resistance to the substrate, which reduces the gain of the parasitic circuit which initiates a latch-up.

ALPIDE-3 SEL Results



ALPIDE-3 SEL Results