The Upstream Tracker Upgrade Project

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On behalf of the LHCb Collaboration

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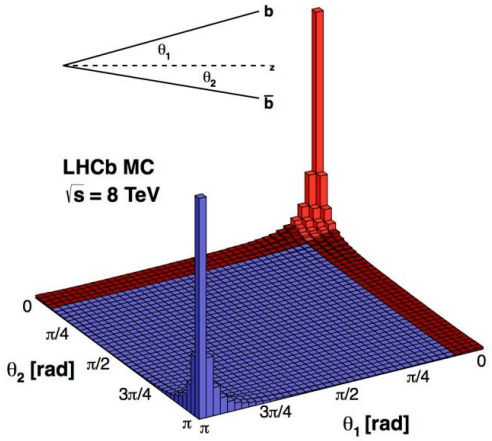
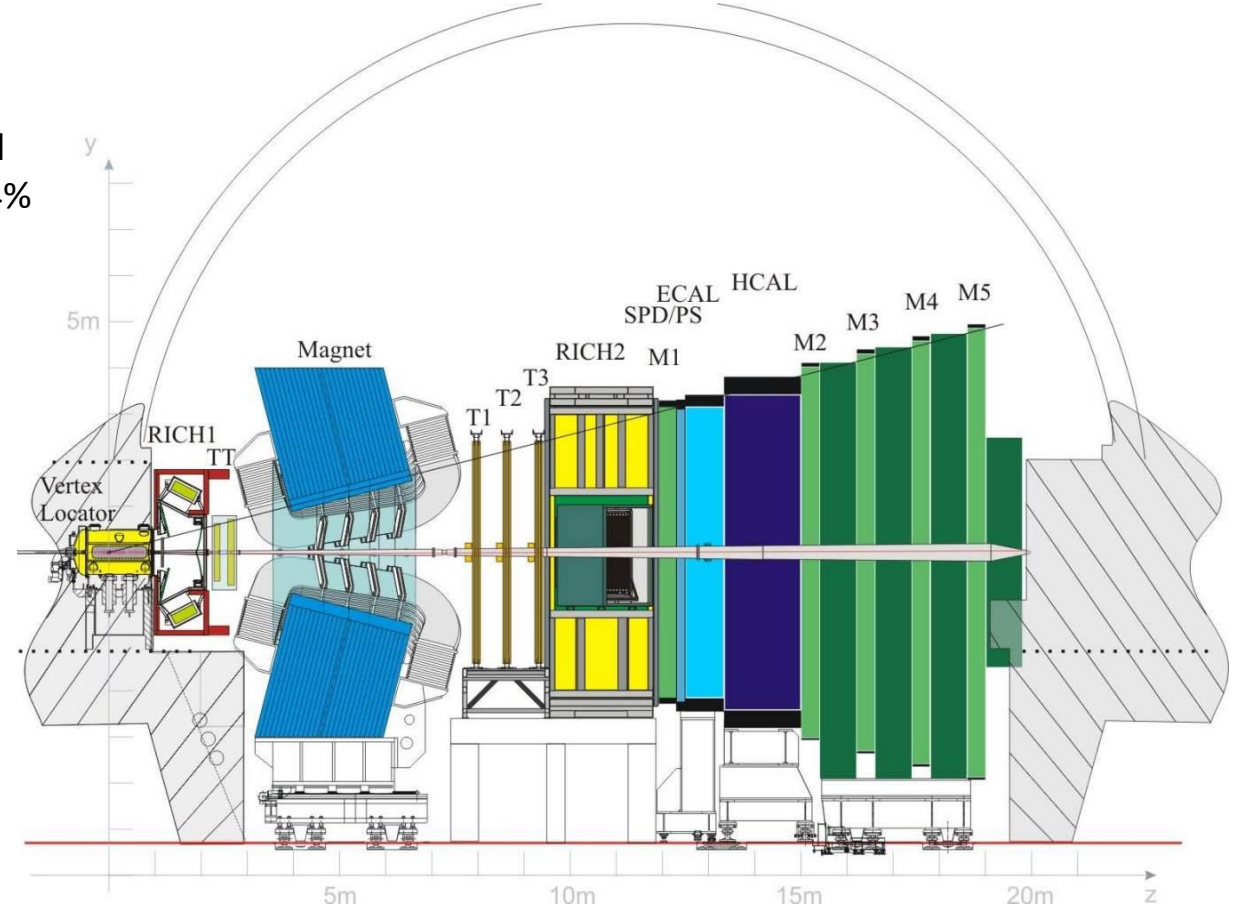
LHCb Detector

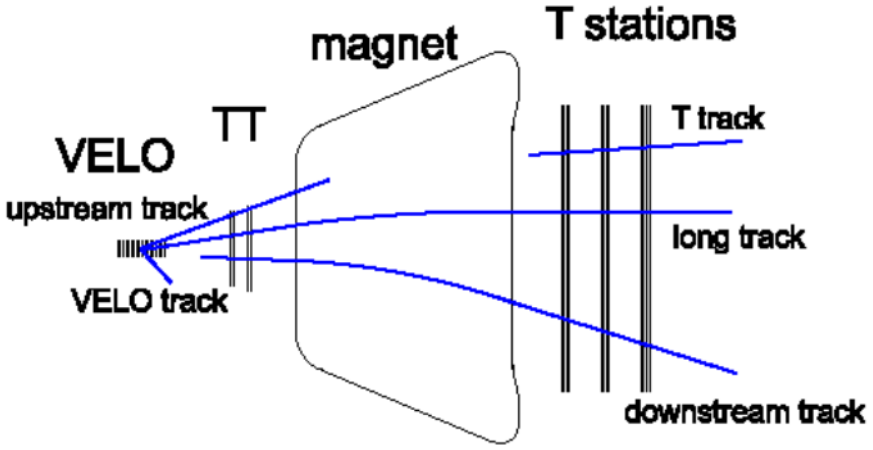
- Single arm forward spectrometer covering 2<η<5
- $b\bar{b}$ production peaked forward and backward – 25% within ~4% solid angle of detector acceptance
  - σ_{inel}~70-80 mb
  - $\sigma_{b\bar{b}}$~500 μb (14 TeV)

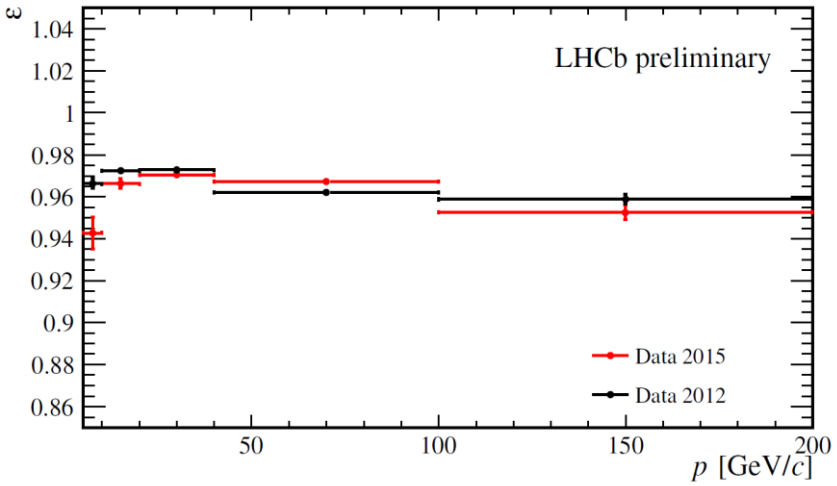




LHCb Tracking

- Three silicon strip detectors
  - Vertex Locator (precision tracking near interaction region)
  - Tracker Turicensis
  - T stations (also straw tubes)
- Tracks formed by linking segments from one or more detectors
- 96% reconstruction efficiency for long tracks
- Fake tracks (ghosts) can be formed by linking real segments from VELO track with wrong T station track

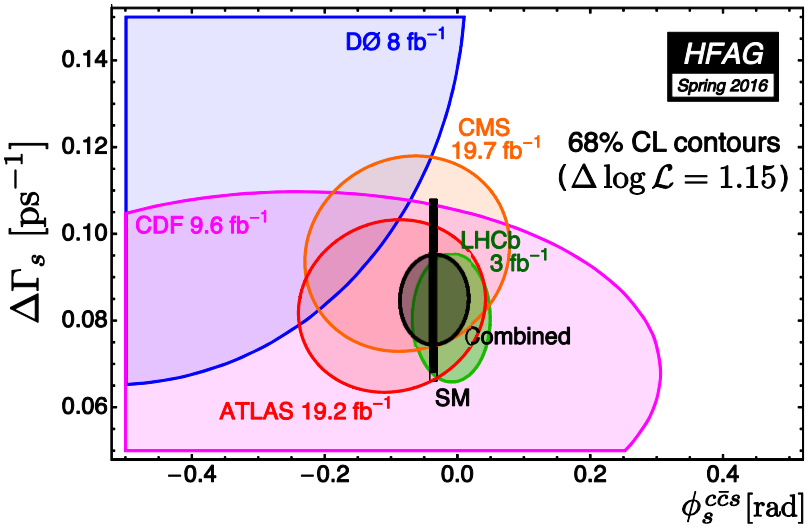


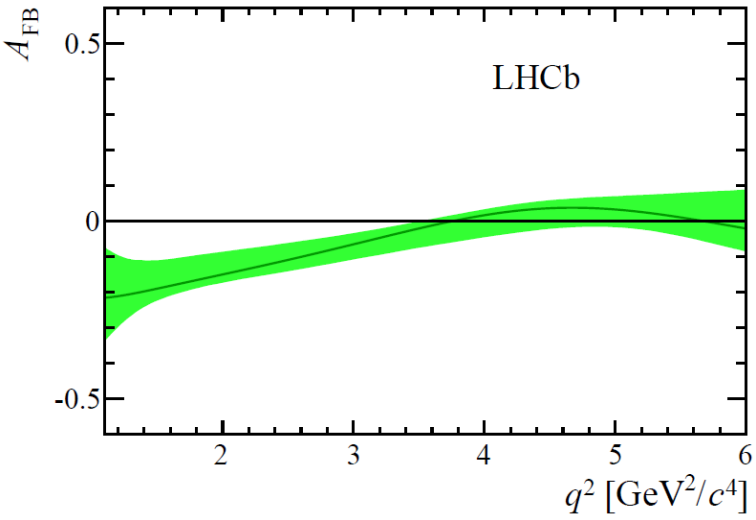


Track reconstruction efficiency for long tracks for 2012 and 2015

Upgrade Motivation

- 3 fb^{-1} of data collected by LHCb in Run 1, plan to collect >5 fb^{-1} in Run 2 at up to L = 4 x 10^{32} cm^{-2} s^{-1}
- **After LS2, plan to collect ~50 fb^{-1} at L = 2 x 10^{33} cm^{-2} s^{-1}**
- Flavor physics observables provide key inputs to the Standard Model (SM) and greatly constrain BSM physics
- New particles above the TeV scale could induce deviations from SM, e.g.
  - ϕ_s, B_s mixing
  - q_0^2 A_{FB}, B_0 -> K^{*0} mu^+ mu^-
- Aim to reduce statistical uncertainties and achieve precision comparable to theoretical predictions in these and many other modes

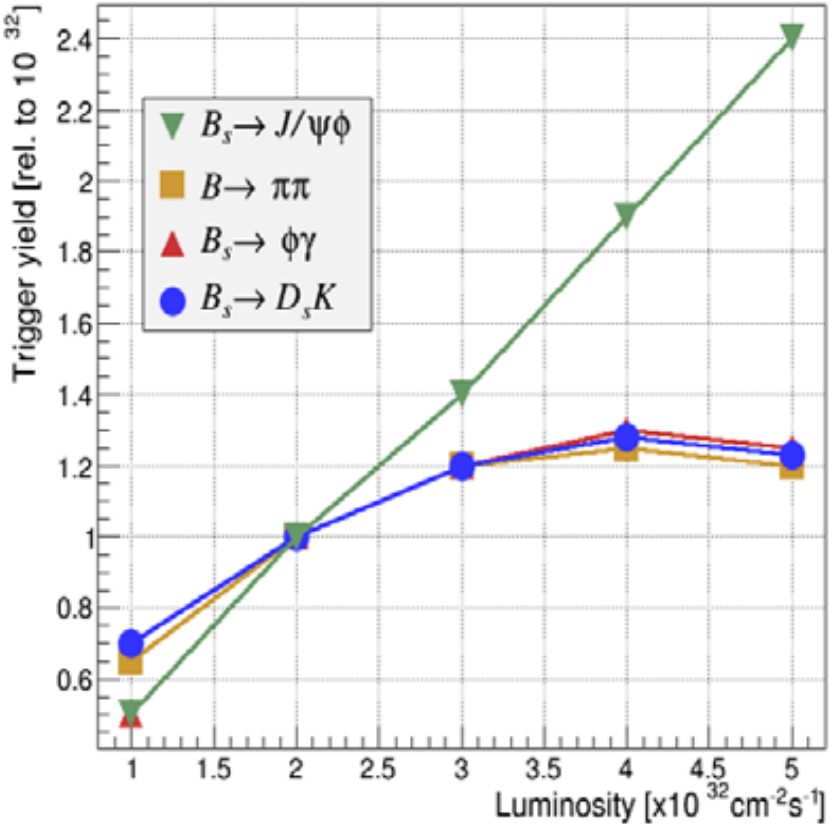




Observable	LHC Run 1	LHCb 2018	**LHCb upgrade**	Theory
$\phi_s(B_s^0 \to J/\psi\phi)$ (rad)	0.049	0.025	**0.009**	~ 0.003
$q_0^2 A_{\rm FB}(B^0 \to K^{*0}\mu^+\mu^-)$	10%	5%	**1.9%**	$\sim 7\%$

Upgrade Strategy

- Current low-level trigger
  - Calorimeters and muon system make 40 MHz decisions
  - Read-out rate of 1 MHz for complete detector
  - E_T threshold substantial fraction of B mass – saturates for hadronic modes at increasing luminosity
- Upgrade strategy
  - Read out full detector at 40 MHz
  - Use tracking information to make trigger decisions in software
  - Replace tracking system, modify detectors for high luminosity, replace front-end electronics and integrated elements

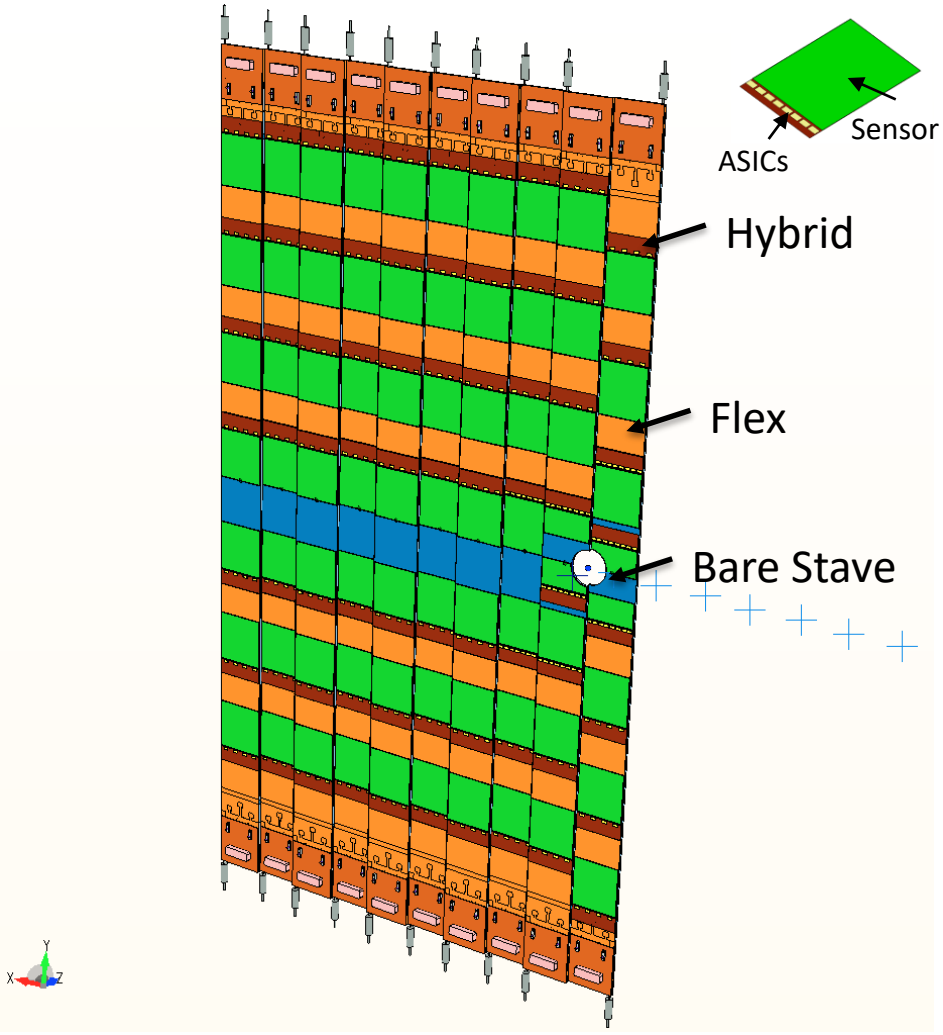


Trigger yield vs. Luminosity with current trigger scheme

The New Upstream Tracker

- Replaces current upstream tracker (TT)
  - Compatible with 40 MHz readout
  - Increased granularity to accommodate increased occupancy
  - Minimize gaps in acceptance
  - Radiation tolerant through at least 50 fb^{-1} of data collection (up to 40 MRad near beamline with safety factor of 4)
- Dipole fringe field gives VELO+UT momentum resolution of $\sigma(P_T)/P_T$ ~15%
  - Sufficient to determine sign of charge and suppress low-momentum tracks
- Reduce ghost tracks by providing intermediate measurements between VELO and downstream tracking
- **Decreases time required to extrapolate VELO tracks to T station search window by at least a factor of 3 (LHCb-TDR-015)**
- Target single hit efficiency of 99%

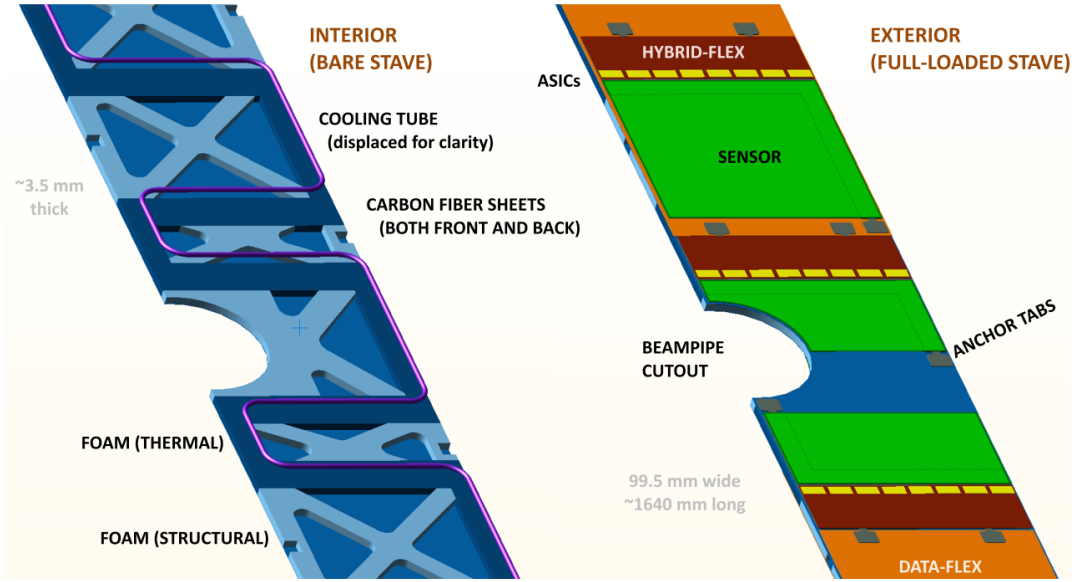
UT Design



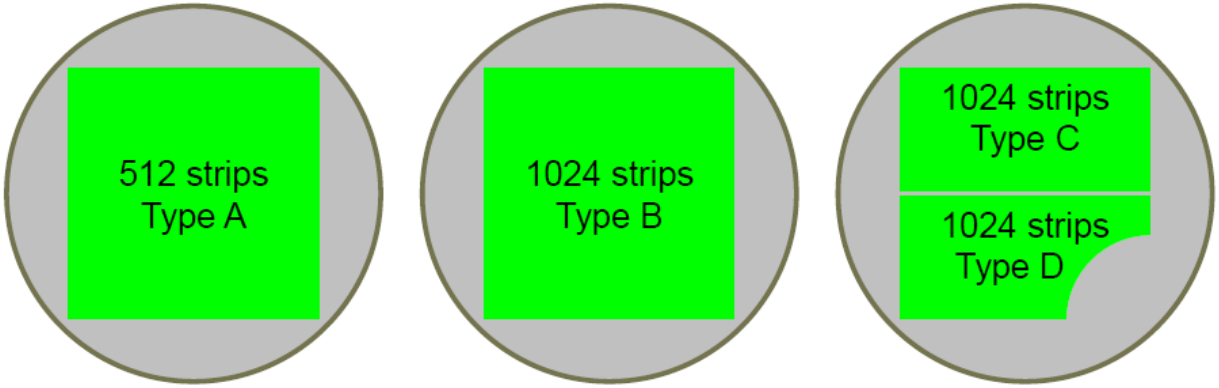
- Four planes composed of vertical staves
- Single-sided silicon strip sensors mounted on either side of staves, partially overlapping in Y direction
- Staves staggered in Z for partial overlap in X direction
- U and V layers provide stereo information
- Sensors feature improved segmentation in high-occupancy region, cutout for beam
- Integrated FE electronics wirebonded to sensor on hybrid flex circuits transmit zero-suppressed digital signals

Stave

- Primary mechanical element of the UT
- Bare stave composed of thermal and structural foam core sandwiched between carbon fiber sheets
- Each stave supports up to 16 hybrid modules, 4 flex cables, single CO_2 cooling tube
- Targeted precision of few hundred μm driven by thermal considerations
- Inspired by ATLAS upgrade design
- Each plane composed of 16/18 staves



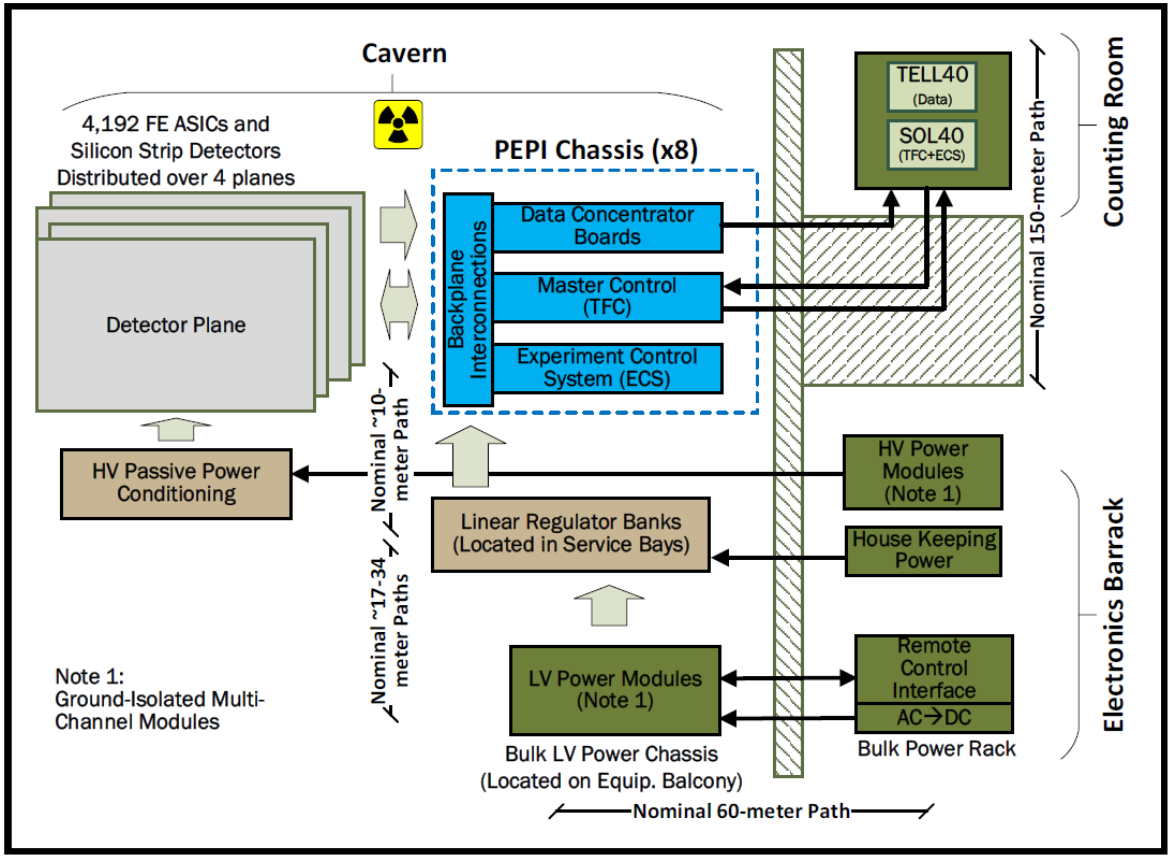
Silicon Sensors



- 99.5mm by 97.5mm (and half-height) strip sensors
- Type A: 320 µm thickness, Type B,C,D: 250 µm
- Type A: embedded pitch adapters match strip pitch (~190 µm) to readout pitch (80 µm), mostly p-in-n technology
- Other sensors: n-in-p for improved radiation hardness
- Type D: circular beam cutout to maximize acceptance
- Biased from front side, backside passivated

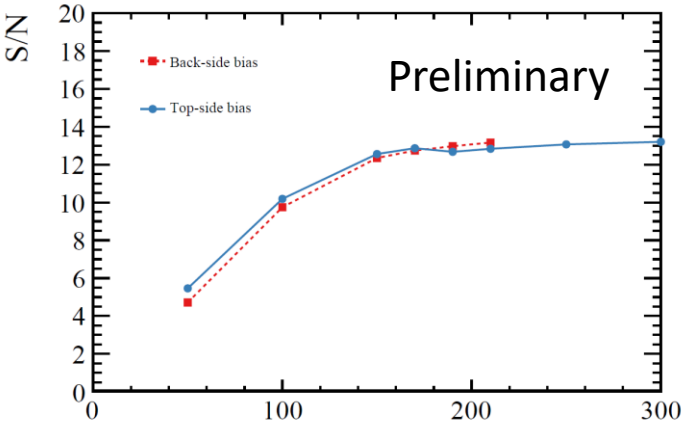
Electronics Overview

- Front-end electronics digitize, process, zero suppress data on-detector
- Processed data transmitted through hybrids and data-flex cables to peripheral electronics
- Peripheral electronics read out, repackage, and convert data to optical
- Event building in counting room by TELL40
- Power regulated remotely from service bays (~10m away)

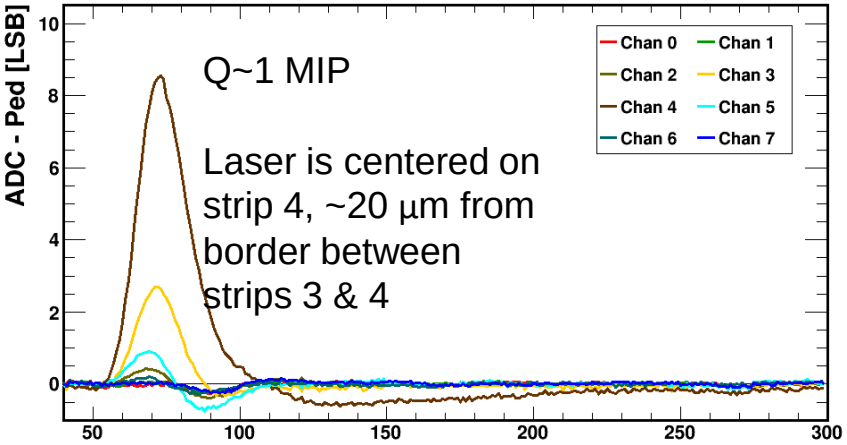


Selected R&D Highlights

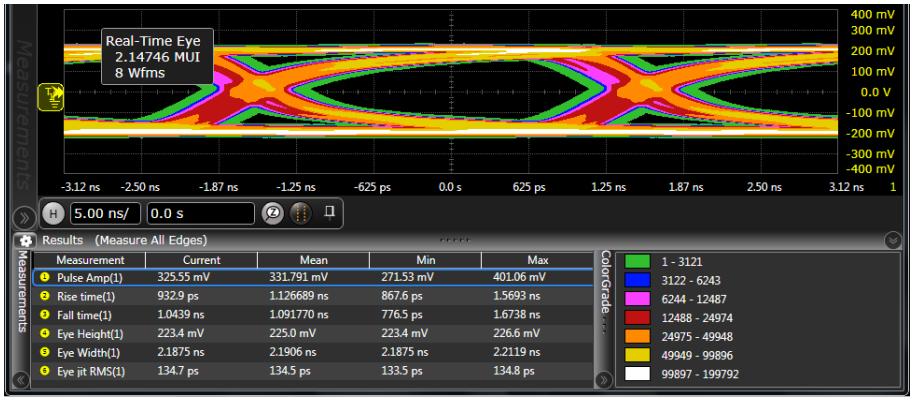
- Staves
  - Construction methods validated
- Sensors
  - Tests of signal to noise, pitch adapters, front-side biasing
- Front-end electronics
  - Tests of analog front-end, DSP, TID tests in progress
- Flex cable
  - Signal integrity and crosstalk evaluated
- Low voltage regulator and readout boards
  - Successful power regulation
  - Configuration and communication with readout electronics



Half-A p-in-n 320 µm, after irradiation



Laser scan of full-length type A sensor



Eye diagram through flex cable

Summary

- The Upstream Tracker is a critical part of the planned LHCb upgrade
  - Fast readout and reduced time for track reconstruction allow for software based event decisions
- Research and development wrapping up
  - Staves mount sensors and electronic and cooling support
  - Silicon sensors with embedded pitch adapters, top-side biasing, and beamline cutouts
  - Rapid data processing by front-end electronics, readout and power regulation from outside detector area
- Transitioning to construction, starting with bare staves

Backup

Sensitivities to Key Observables

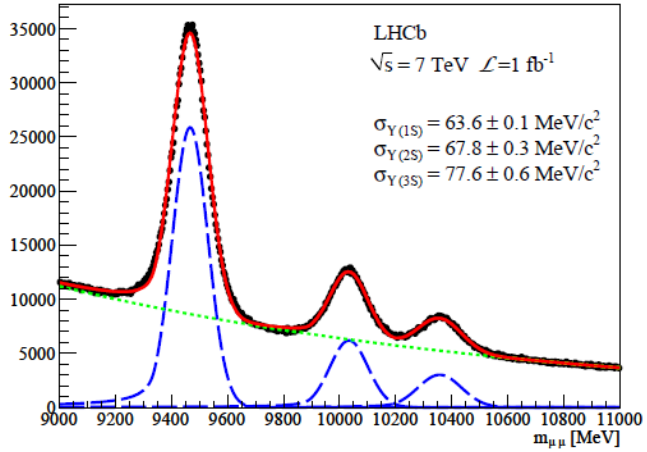
Table 27: Statistical sensitivities of the LHCb upgrade to key observables. For each observable the expected sensitivity is given for the integrated luminosity accumulated by the end of LHC Run 1, by 2018 (assuming $5\,\text{fb}^{-1}$ recorded during Run 2) and for the LHCb Upgrade ($50\,\text{fb}^{-1}$). An estimate of the theoretical uncertainty is also given – this and the potential sources of systematic uncertainty are discussed in the text.

Type	Observable	LHC Run 1	LHCb 2018	**LHCb upgrade**	Theory
B_s^0 mixing	$\phi_s(B_s^0 \to J/\psi\,\phi)$ (rad)	0.049	0.025	**0.009**	~ 0.003
	$\phi_s(B_s^0 \to J/\psi\ f_0(980))$ (rad)	0.068	0.035	**0.012**	~ 0.01
	$A_{\rm sl}(B_s^0)$ (10^{-3})	2.8	1.4	**0.5**	0.03
Gluonic penguin	$\phi_s^{\rm eff}(B_s^0 \to \phi\phi)$ (rad)	0.15	0.10	**0.018**	0.02
	$\phi_s^{\rm eff}(B_s^0 \to K^{*0}\bar{K}^{*0})$ (rad)	0.19	0.13	**0.023**	< 0.02
	$2\beta^{\rm eff}(B^0 \to \phi K_{\rm S}^0)$ (rad)	0.30	0.20	**0.036**	0.02
Right-handed currents	$\phi_s^{\rm eff}(B_s^0 \to \phi\gamma)$ (rad)	0.20	0.13	**0.025**	< 0.01
	$\tau^{\rm eff}(B_s^0 \to \phi\gamma)/\tau_{B_s^0}$	5%	3.2%	**0.6%**	0.2 %
Electroweak penguin	$S_3(B^0 \to K^{*0}\mu^+\mu^-; 1 < q^2 < 6\,\text{GeV}^2/c^4)$	0.04	0.020	**0.007**	0.02
	$q_0^2\,A_{\rm FB}(B^0 \to K^{*0}\mu^+\mu^-)$	10%	5%	**1.9%**	$\sim 7\%$
	$A_{\rm I}(K\mu^+\mu^-; 1 < q^2 < 6\,\text{GeV}^2/c^4)$	0.09	0.05	**0.017**	~ 0.02
	$\mathcal{B}(B^+ \to \pi^+\mu^+\mu^-)/\mathcal{B}(B^+ \to K^+\mu^+\mu^-)$	14%	7%	**2.4%**	$\sim 10\%$
Higgs penguin	$\mathcal{B}(B_s^0 \to \mu^+\mu^-)$ (10^{-9})	1.0	0.5	**0.19**	0.3
	$\mathcal{B}(B^0 \to \mu^+\mu^-)/\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	220%	110%	**40%**	$\sim 5\,\%$
Unitarity triangle angles	$\gamma(B \to D^{(*)}K^{(*)})$	7°	4°	**0.9°**	negligible
	$\gamma(B_s^0 \to D_s^\mp K^\pm)$	17°	11°	**2.0°**	negligible
	$\beta(B^0 \to J/\psi\,K_{\rm S}^0)$	1.7°	0.8°	**0.31°**	negligible
Charm	$A_\Gamma(D^0 \to K^+K^-)$ (10^{-4})	3.4	2.2	**0.4**	–
CP violation	ΔA_{CP} (10^{-3})	0.8	0.5	**0.1**	–

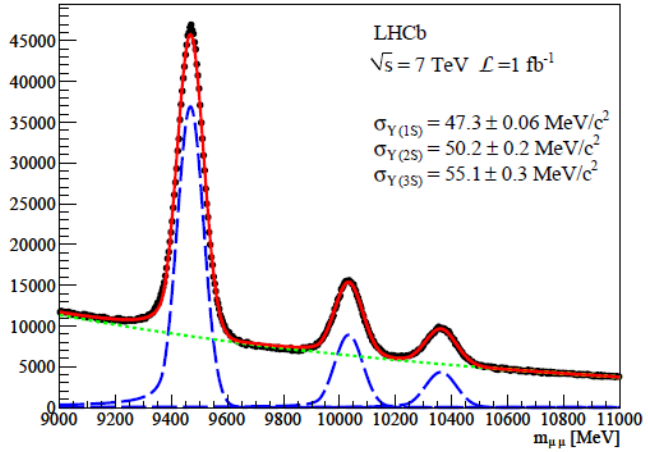
LHCb-PUB-2014-040

UT function

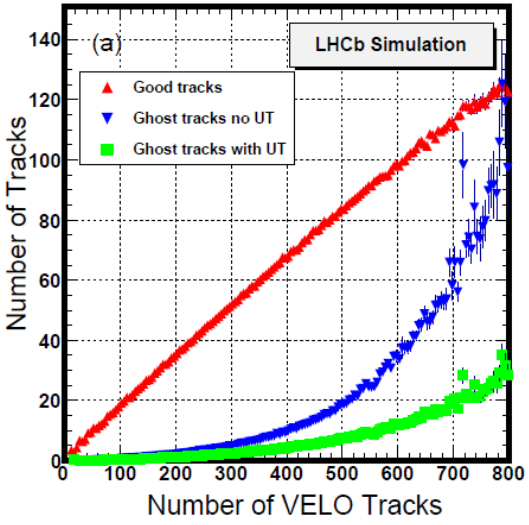
No TT

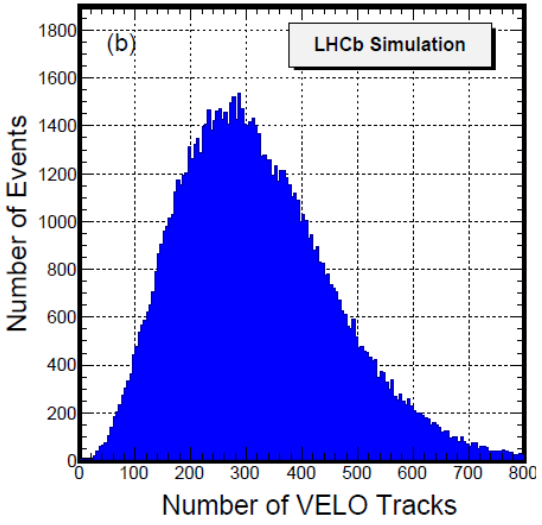


With TT (both hits)



Dimuon resolution in ϒ region

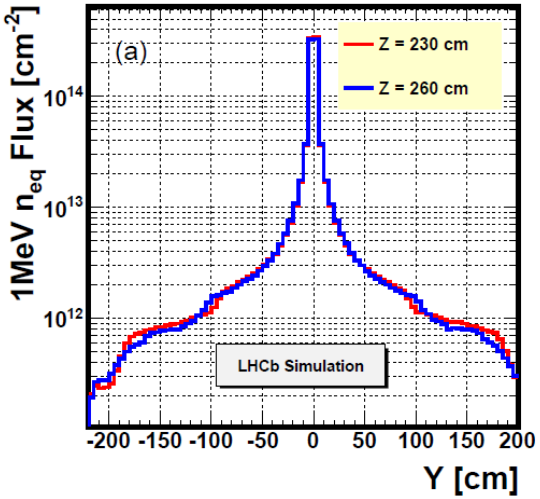


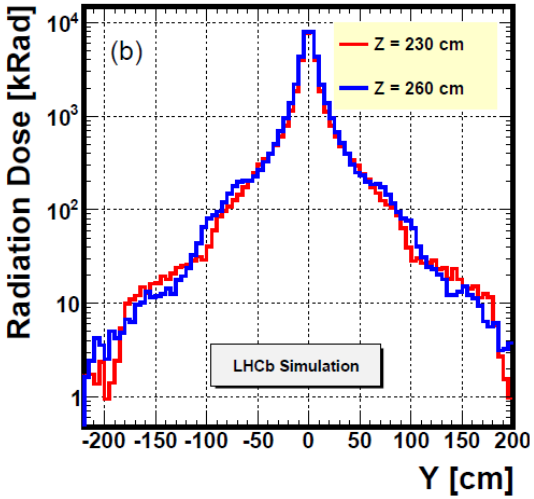


Ghost tracks as a function of VELO tracks at L = 2 x 10^{33} cm^{-2} s^{-1}, and VELO track distribution. With UT requires 3/4 hits

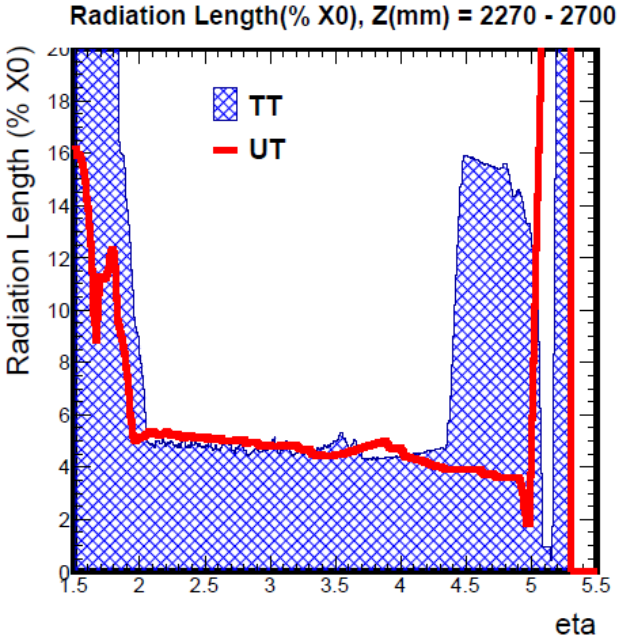
Radiation Environment and Material

Expected fluence and dose for 50 fb-1 at X=0





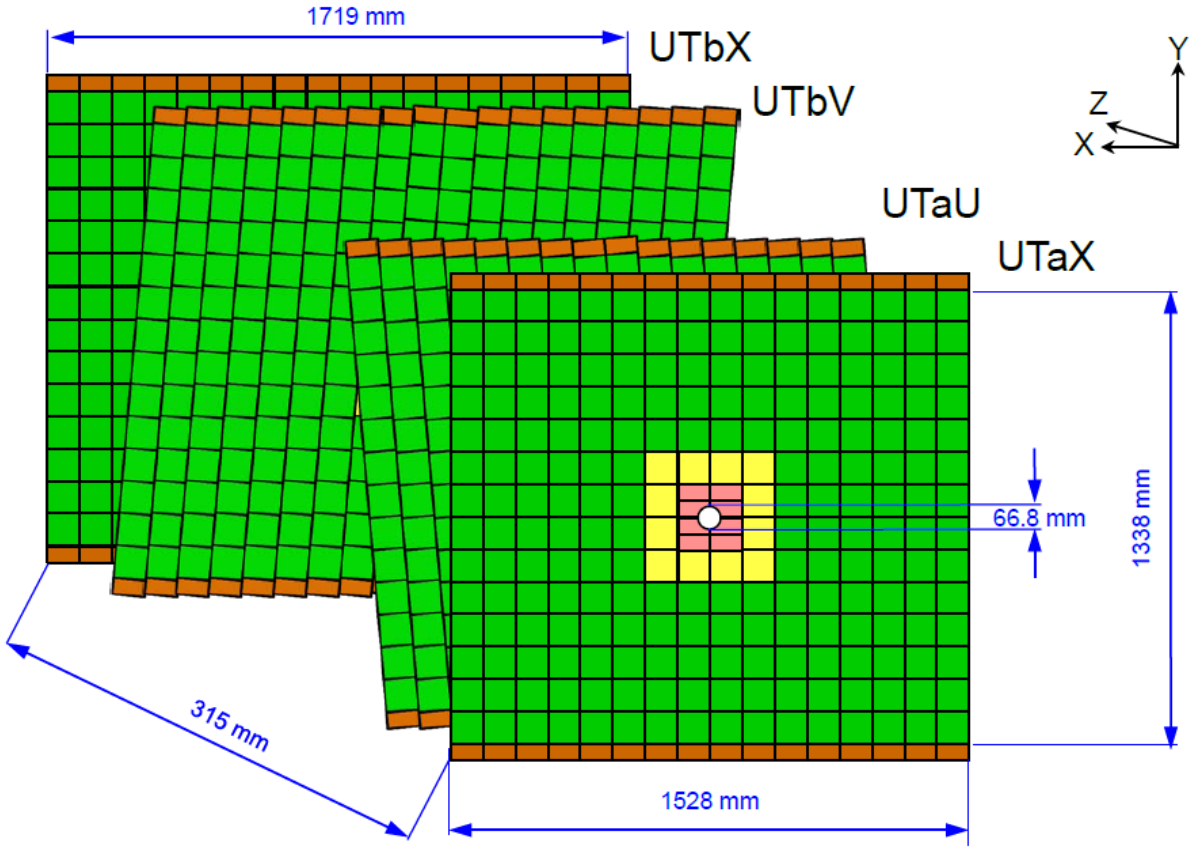
Radiation length of UT and TT



- From minimum bias simulation at **L = 2 x 10^{33} cm^{-2} s^{-1}**, sqrt(s) = 14 TeV
  - average #hits/event = 1000
  - average cluster size = 1.44
  - average occupancy = 1.8%
  - 0.34 hits/ASIC, 2.3 around beampipe

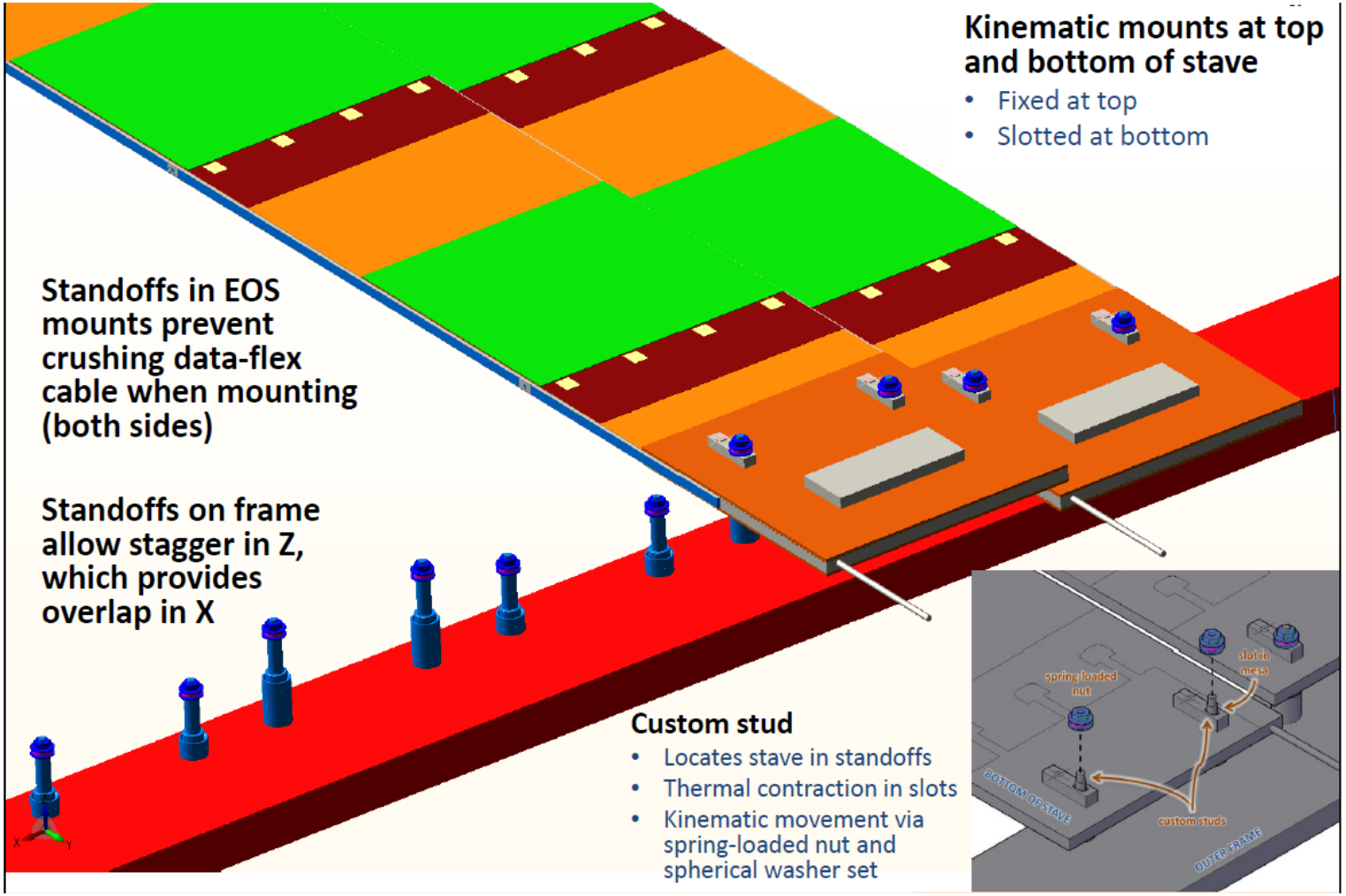
UT Coverage

1 Stave ~ 97.28 mm x 1336 mm
UTbX coverage: -314 < θx < -314, -248 < θy < 248)
Active area starts at ~34 cm (to be determined)



Stave Mounting

Align sensors to ~ 100 microns, with <20 micron stability

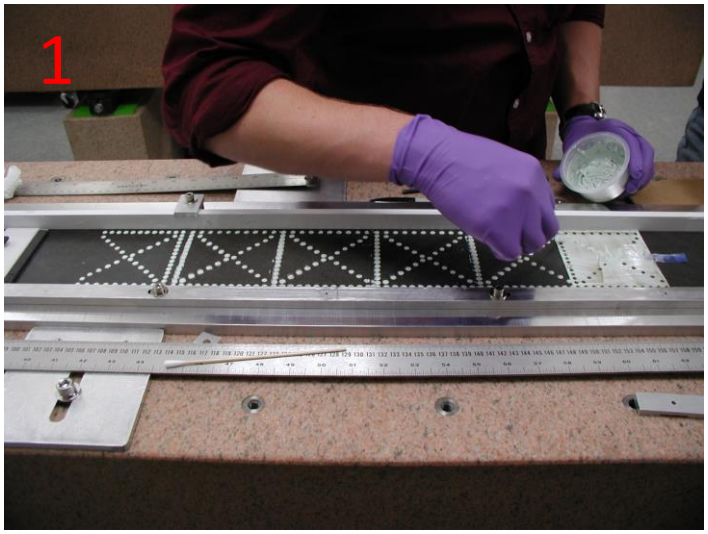


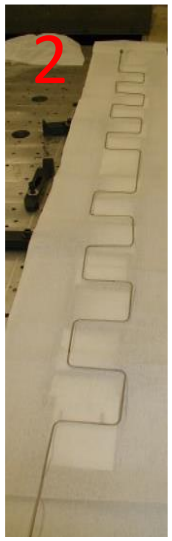
Stave Materials

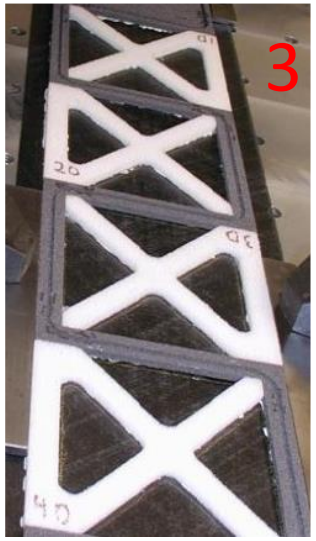
- Backing: K13C2U high-modulus carbon fibers in EX1515 epoxy matrix, 45gsm
- Thermal foam: AllcompK-9 carbon foam – high thermal conductivity (~35 W/m.K), low mass density (0.2 g/cm3)
- Structural foam: EvonikRohacell51 IG, a commercially-available polymethacrylimide(PMI) polymer foam – solid, not thermally conducting, very low mass density (0.051 g/cm3)
- Cooling tubes: Titanium CP2 alloy – OD 2.275 mm, 135 um wall thickness

Stave Construction

Start with carbon fiber backing held in vacuum fixture







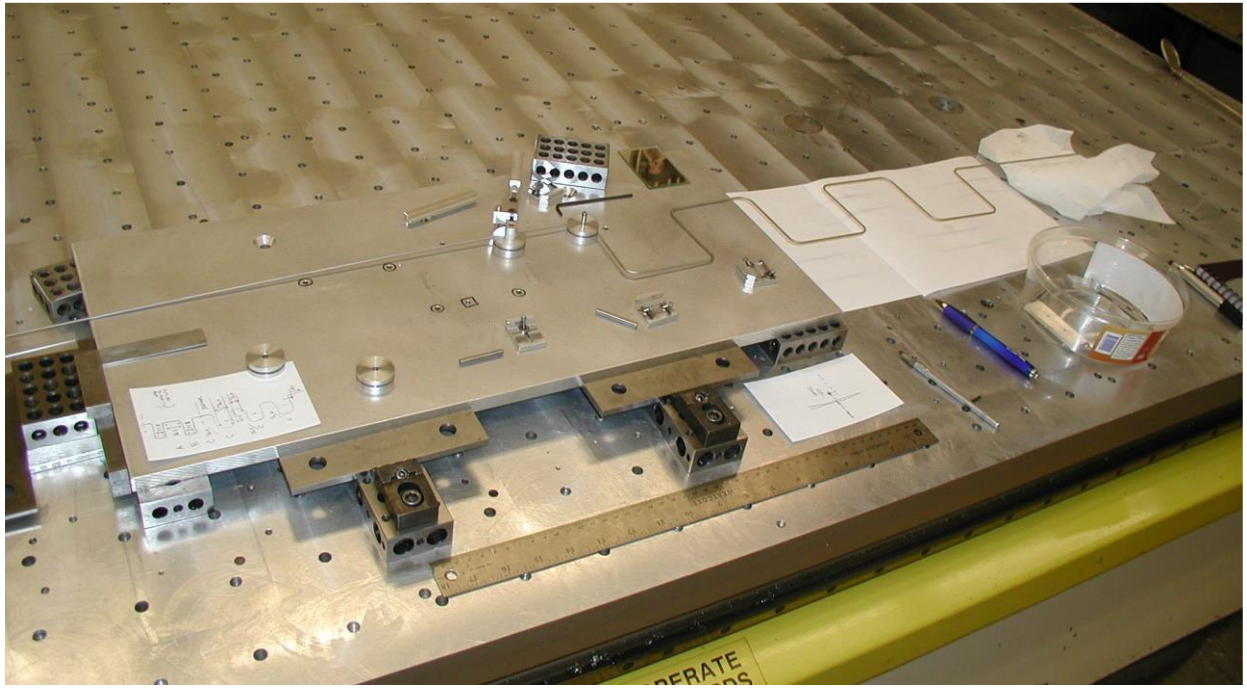
Foam core pieces epoxied to backing, cooling tube epoxied into milled trough in foam core

Metrology, trimming: target precision of foam element positions a few hundred µm, currently at 0.5 mm

Two bare staves assembled to validate construction process

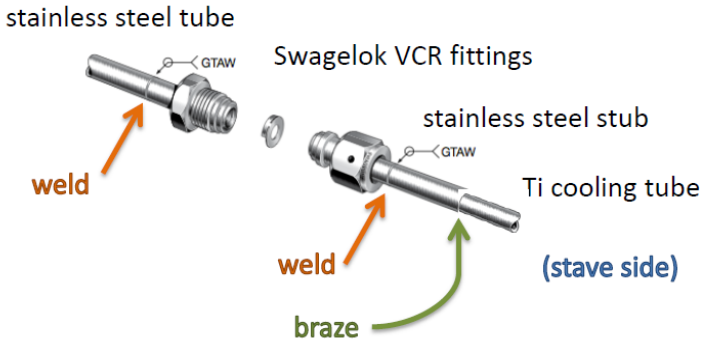
Second backing epoxied to assembly, aligning vacuum fixtures

Cooling Tubes

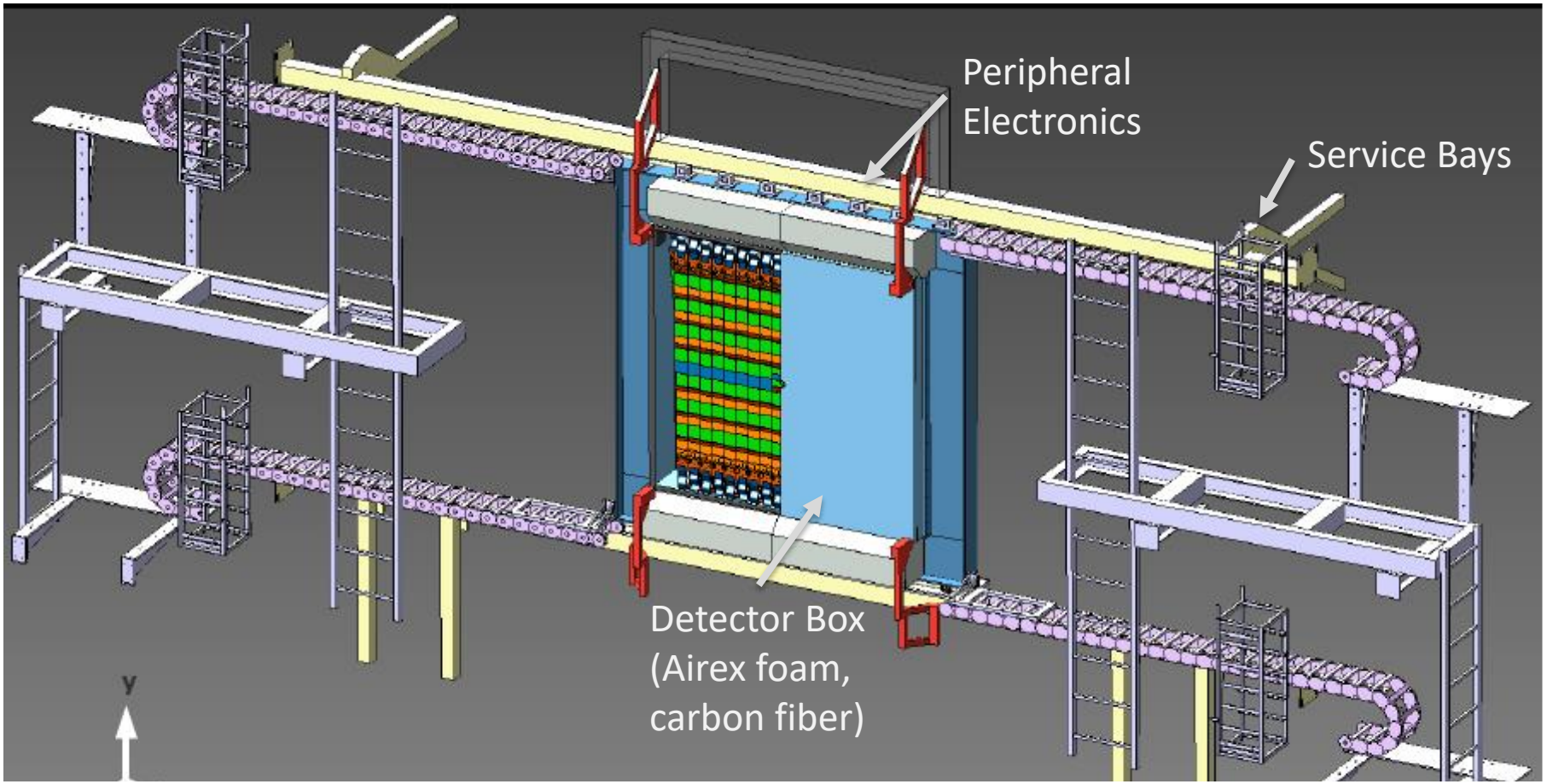


(cooling manifold side)

FITTING SCHEME



UT Exterior


Peripheral Electronics
Service Bays
Detector Box (Airex foam, carbon fiber)
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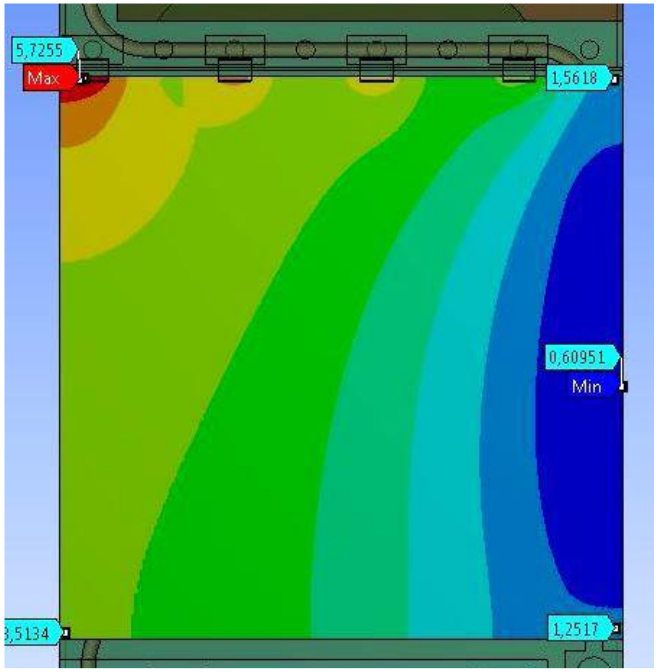
Mechanics and Cooling



Sensor temperature ranges from -24°C to -19°C

- Staves cooled by bi-phase CO_2 system
- Snaked cooling pipe positioned under each horizontal ASIC group for best thermal performance
- Finite Element Analysis assumes 0.768 W / ASIC, 10% power dissipation in flex cable, and 0.135 W type A sensor self heating
- Indicates sensors will be cooled to <-5°C, and uniformity Δ5°C
- Thermo-mechanical analysis performed to determine thermal deformations and vibrational modes
- Peripheral electronics cooled by water

TRACI

Multipurpose Refrigeration Apparatus for CO_2 Investigation

Cold box closed for testing

Dummy stave with titanium snake pipe cooling tube

Instrumented with heat loads, temperature sensors

TRACI pumps CO_2 at 1 g/s +/- 0.05 g/s

Stave successfully cooled to -27°C

Sensor R&D Phase I

- Quantify performance of Micron mini-sensors (1.1x1.1 cm^2) before and after irradiation
  - n-in-p and p-in-n
  - 80 µm pitch
  - With and without type D circular cutout
- Irradiated to ~4×10^{14} MeV N_{eq}/cm^2 (max fluence w/ safety factor of 2) at MGH in June 2014, tested in a 180 GeV proton beam at CERN in Oct. 2014
- Readout by Beetle chips (LHCb-2005-105)
- ~15% loss of charge collection after full irradiation
- S/N >18 for V>400 V
- No significant loss of efficiency around cutouts

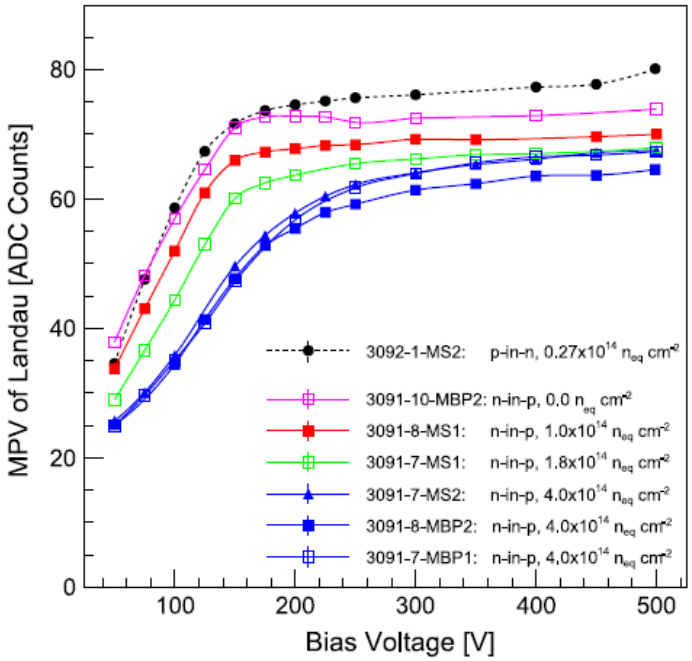


Fig. 12. The most probable value of the collected charge for all cluster sizes from the Landau fit as a function of bias voltage for each of the DUT. Tracks are at normal incidence to the sensor.

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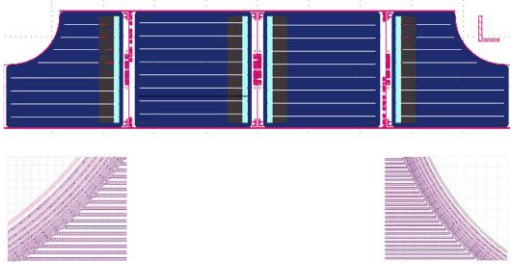
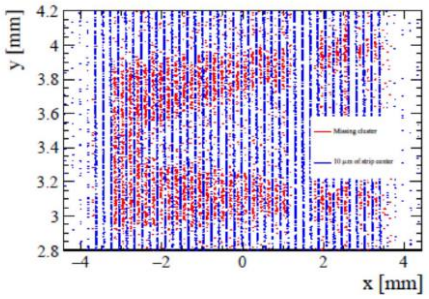
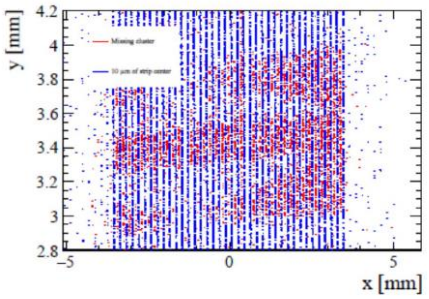


Sensor R&D Phase II

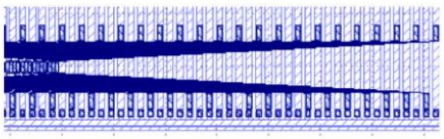
- Test full-length Hamamatsu sensors in addition to further studies of mini sensors
  - Evaluate effect of pitch adapters, fan-up and fan-in
  - Characterize D-type sensors (circular cutout)
  - Compare topside and backside biasing
- 200 µm sensors (manufacturing error), n-in-p
- Irradiated at CERN IRRAD facility, type A up to 3.3×10^{13} MeV N_{eq}/cm^2, type D up to 4.6×10^{14} MeV N_{eq}/cm^2
- Type A sensors (half width)
  - Inefficient region between strips where fan-in pitch adapter crosses – charge spread to other strips
  - PA region roughly 1mm: 0.2% inefficiency over entire sensor
  - No such effect observed in fan-up or no-PA case, but fan-in is still preferred design
  - S/N ~8 (expect 13 at 320 µm thickness), minor decrease with irradiation
  - Finalizing a design that maintains stability while improving efficiency
- Preliminary results show no difference between topside and backside biasing schemes



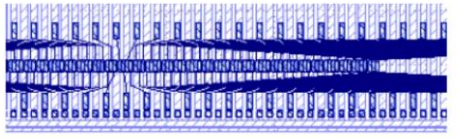
(a) Edge of pitch adapter region



(b) Center of pitch adapter region

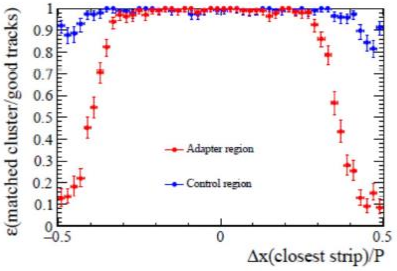


(c)

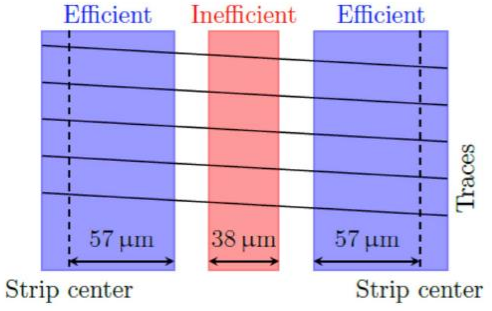


(d)

Position of tracks with missing clusters



(a)

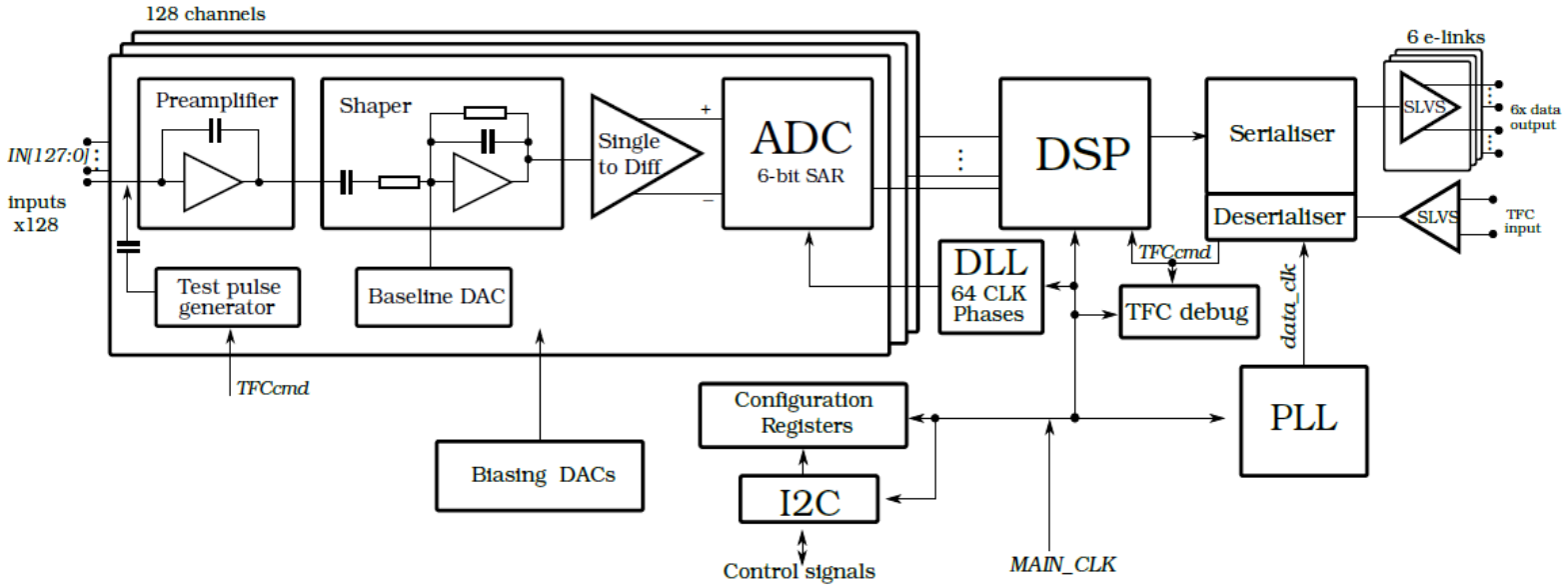


(b)

Efficiency vs. interstrip position for PA region

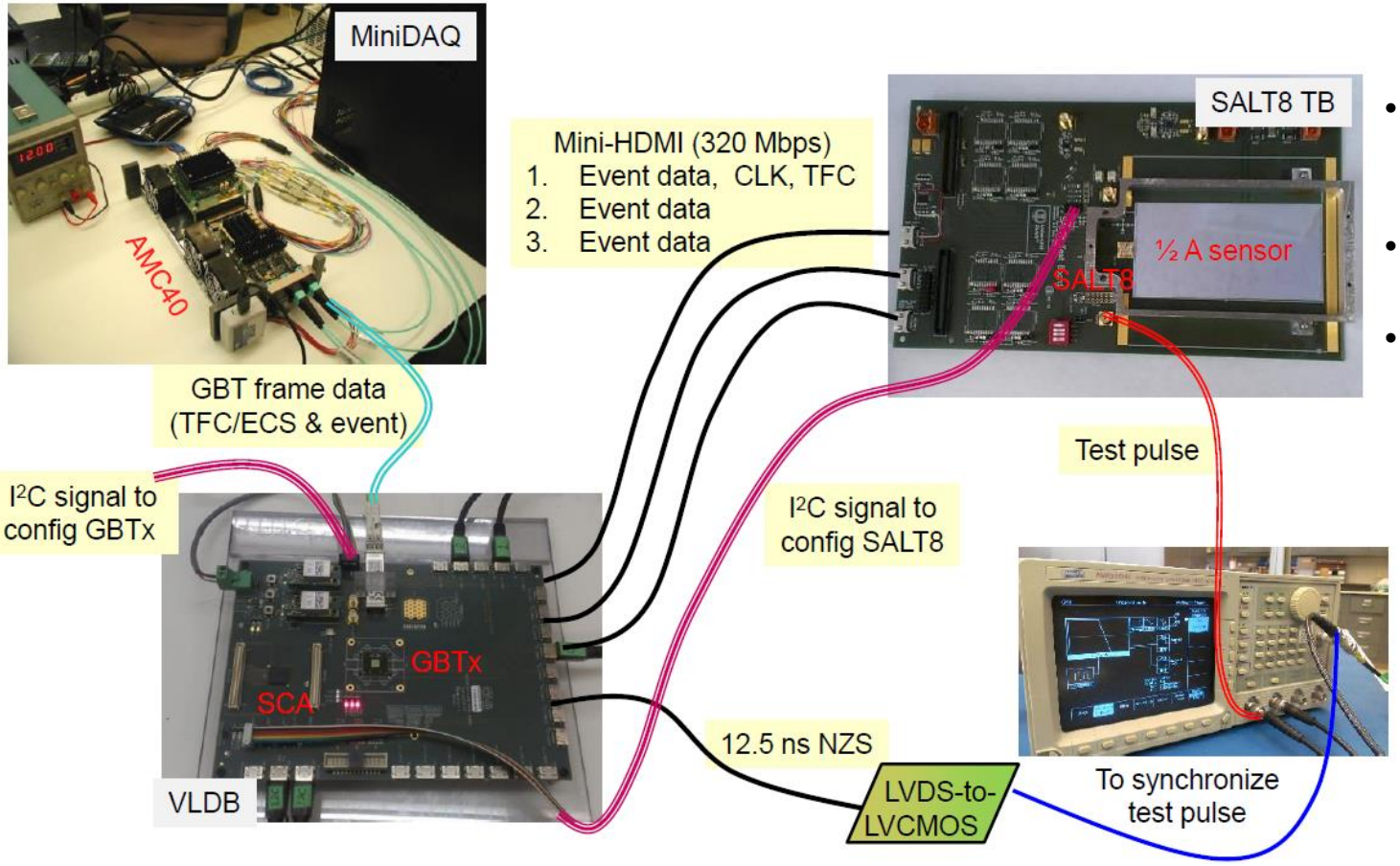
LHCb-PUB-2016-007

Front-end Electronics



- 128 channel **S**ilicon **A**SIC for **L**HCb **T**racking (SALT) wirebonded to sensors
- TSMC CMOS 130 nm technology, 50 MRad radiation tolerance
- Extracts and digitizes analog signals, performs pedestal and common mode subtraction, zero suppression
- Serialize and transmit data via 320 Mbps e-ports
- Sensor capacitance 5-20 pF, AC coupled
- Noise: ~1000e^- at 10 pF + 50e^-/pF
- 40 MHz readout: shaper $T_{peak} \leq 25$ ns, <5% after 2 T_{peak}
- Power consumption ~768mW/ASIC

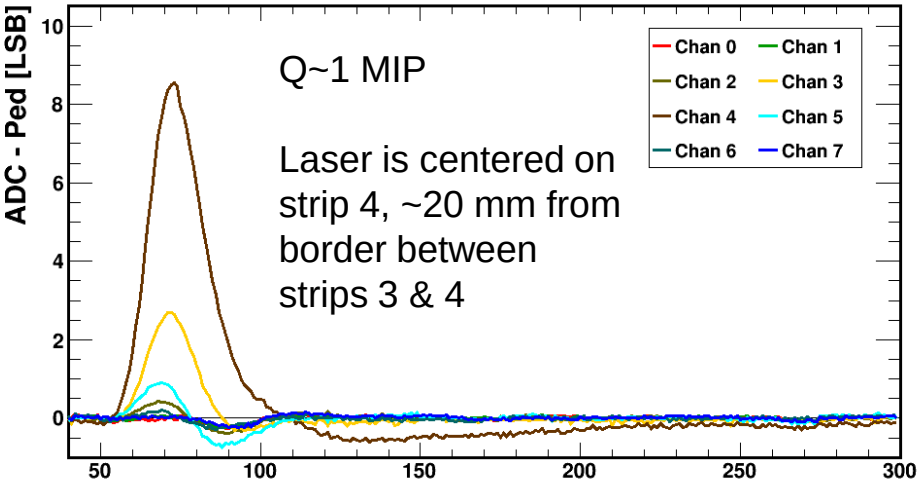
SALT Test Setup



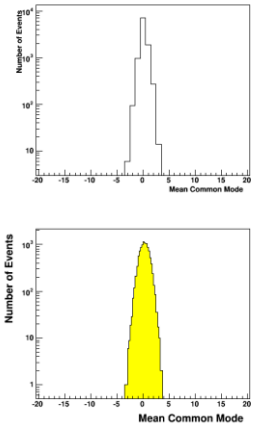
- Test pulse can also be injected to laser generator
- Pulse width ~10 ns, height 1.3V, 1.56V
- Output width ~ 7 ns, energy deposition ~ 1 & 2 MIPs.

SALT8 Tests

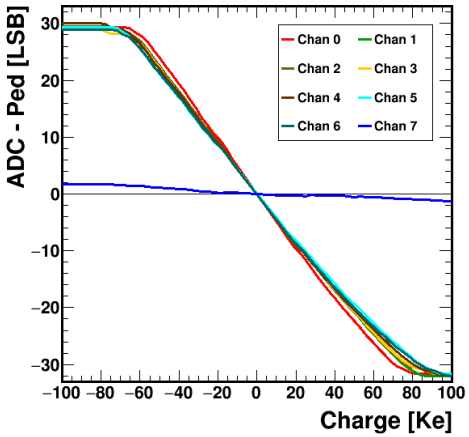
- Two 8-channel SALT versions produced
  - Tests of analog front-end, DSP
  - Noise performance matches expectation
  - Data packet format validated
  - Successful communication with GBTx, GBT-SCA (VLDB)
- 128-channel SALT prototype produced
- TID tests underway at CERN x-ray facility
  - Performance
  - Power consumption



Laser scan of full-length type A sensor



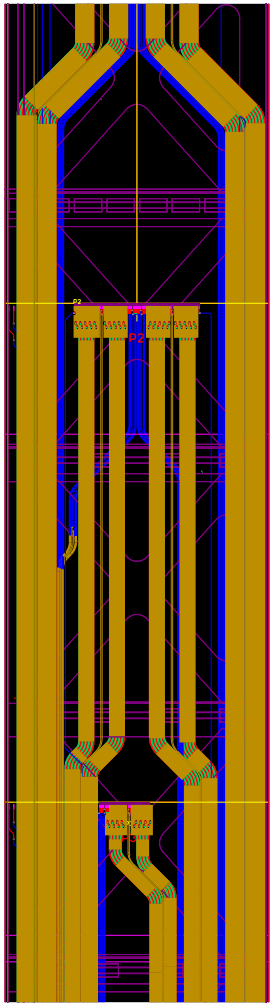
Common mode calculation, from offline (yellow) and SALT8 (white)

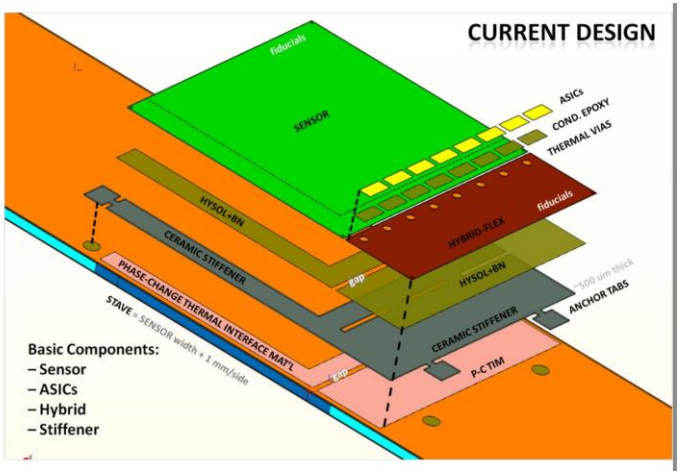


Gain curve is symmetric

Flex Circuits

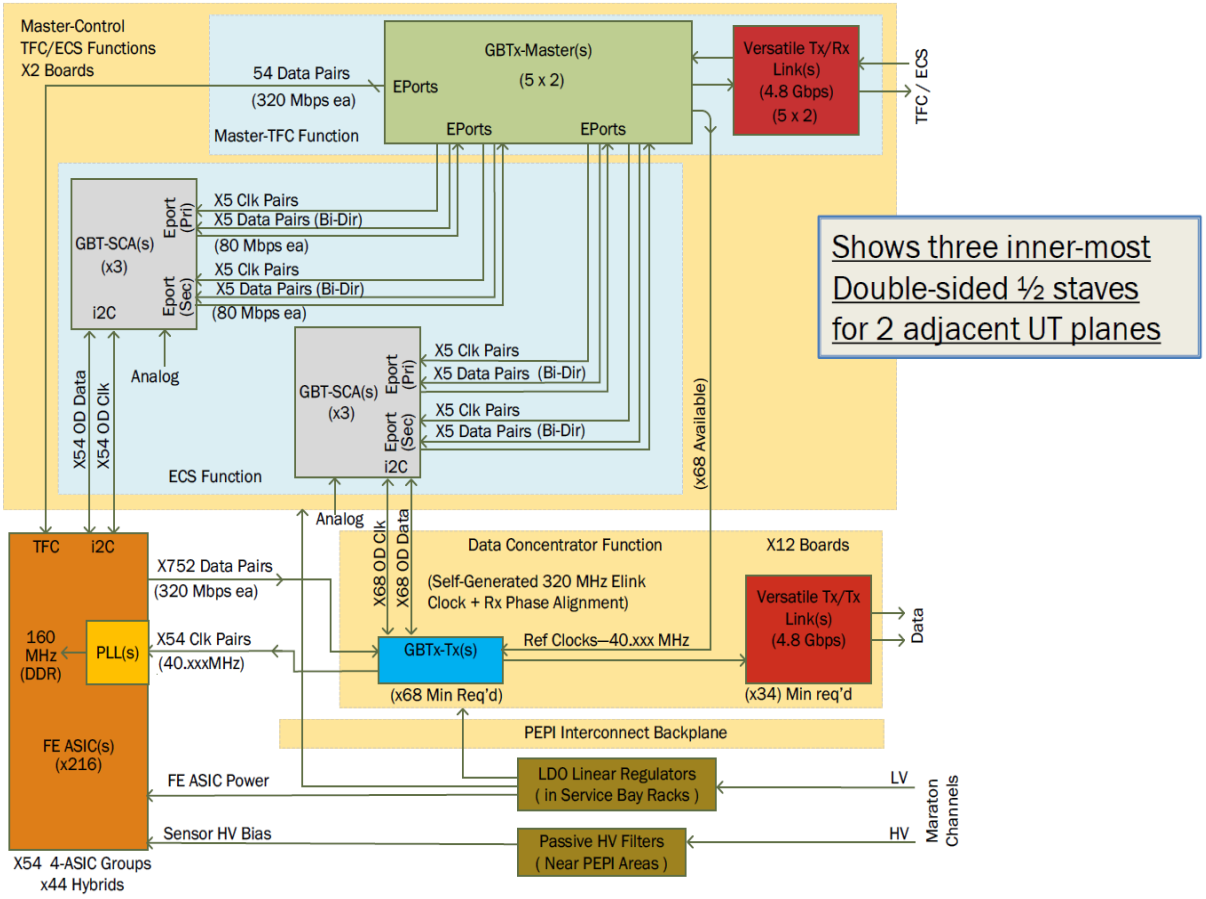
- Hybrid: flex circuit supporting one sensor, hosting 4 or 8 ASICs and providing thermal bridge
- Wire-bonded to flex cables (similar technology)
- Connected to peripheral electronics through BGA connectors and flexible ‘pigtails’
- 3 types of flex cable accommodating various sensor configurations
- Up to 120 differential pairs for data, clock, and control lines
- Also distributes remotely regulated 1.2V power to SALT chips at each hybrid (2.4A/4-ASIC group)
- Restrict total copper to minimize radiation length



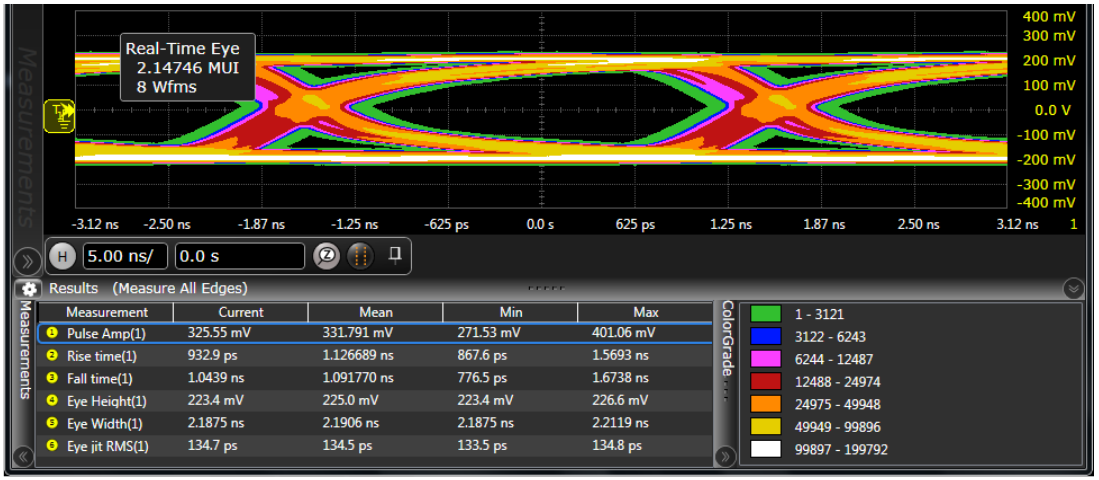


Peripheral Electronics

- Each PEPI (Peripheral Electronics Processing Interface) chassis supports 3 backplanes, each mounting 2 Master Control Boards and up to 12 Data Concentrator Boards
- MCBs: Distribute TFC, ECS, reference clock
- DCBs: Read out data from and provide reference clock to SALT ASICs
- Low voltage regulated and distributed to peripheral and FE electronics by dedicated circuits in service bay



Flex Circuit Validation

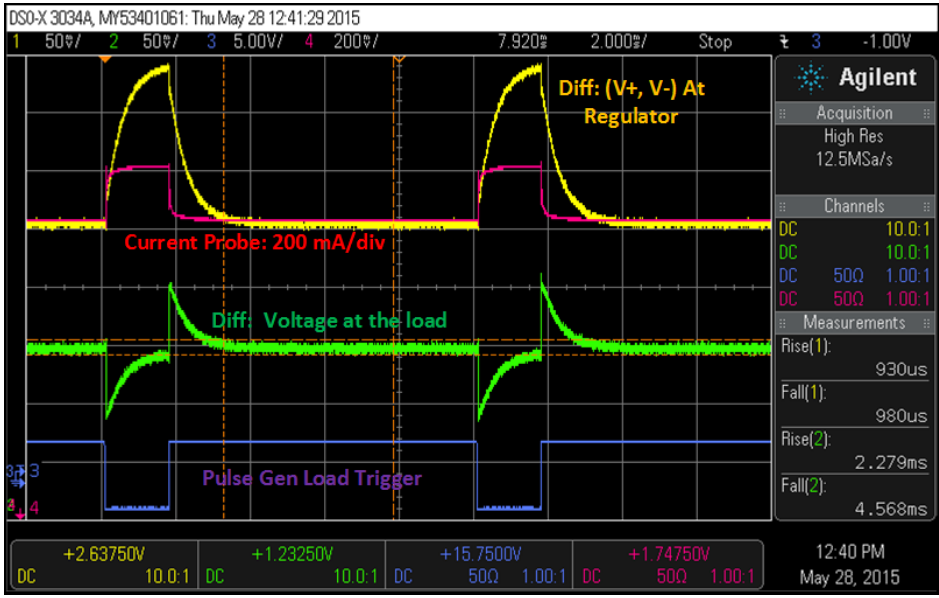


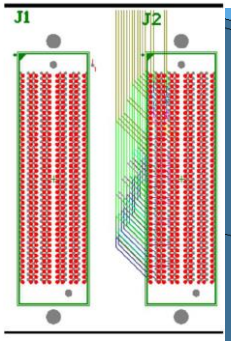
Measurement	Current	Mean	Min	Max
Pulse Amp(1)	325.55 mV	331.791 mV	271.53 mV	401.06 mV
Rise time(1)	932.9 ps	1.126689 ns	867.6 ps	1.5693 ns
Fall time(1)	1.0439 ns	1.091770 ns	776.5 ps	1.6738 ns
Eye Height(1)	223.4 mV	225.0 mV	223.4 mV	226.6 mV
Eye Width(1)	2.1875 ns	2.1906 ns	2.1875 ns	2.2119 ns
Eye jit RMS(1)	134.7 ps	134.5 ps	133.5 ps	134.8 ps

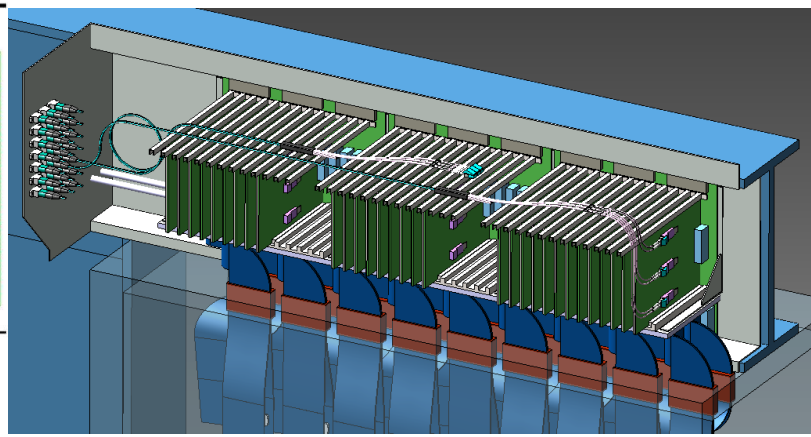
- Hybrid circuit prototype in production
- Two generations of flex cables produced and tested
  - Some challenges: producing flex circuit of ~80cm, controlling impedance of lines
- Signal integrity maintained through flex in realistic signal environment, BER tests ongoing
- ~100 mV crosstalk to I2C slow control lines
- Successfully regulating power through cable
- Next generation cables feature double-thickness power layer to reduce voltage drop to regulator

Peripheral Electronics Validation

- Prototype low voltage regulator board
  - Regulate power over distance from service bay through flex cable
  - Returns to baseline in ~1 ms
  - Radiation tests at MGH indicate SETs are rare and pose no threat to electronics
  - Next gen preproduction board in progress
- Prototype GBT board
  - GBTx-GBTx communication established
  - Will be integrated with SALT, DAQ
  - Evaluating power consumption – feedback to LV distribution plan
- Studies of PEPI volume and routing constraints
  - 3D modeling to validate space and installation procedure
  - Able to route DCB-backplane connection in available space







Flex and Hybrid

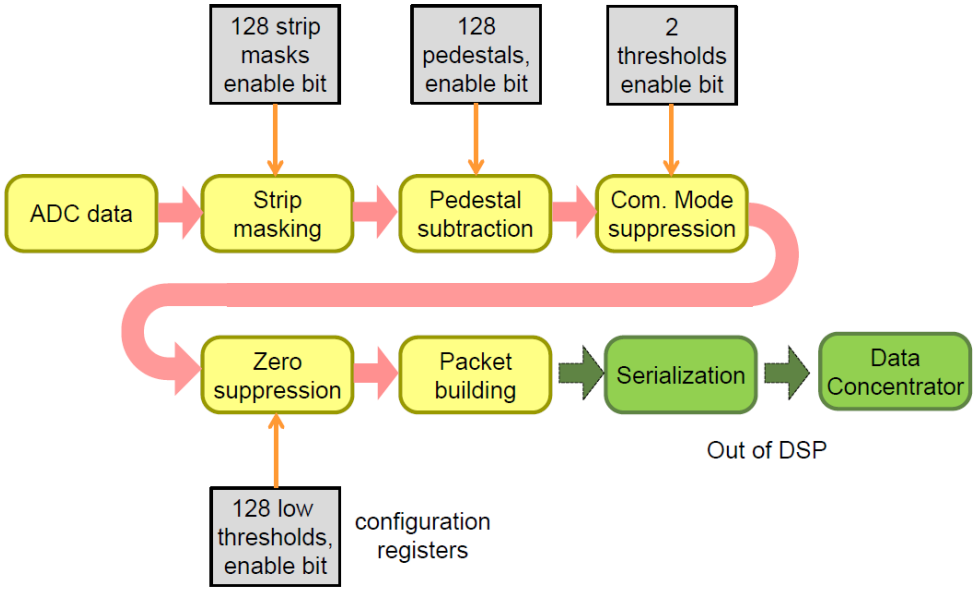
Board Stack Report						
Stack Up			Layer Stack			
Layer	RIGID STACK	FLEX STACKUP	Name	Material	Thickness	Constant
1			Top Paste			
2			Top Overlay			
3			Top Solder	Solder Resist	0,010mm	4,8
4			Top Layer	Copper	0,017mm	
5			Dielectric1	Poliammide	0,100mm	3,4
6			Inner-1	Copper	0,017mm	
7			Dielectric2	Poliammide	0,100mm	3,4
8			Inner-2	Copper	0,017mm	
9			Dielectric3	Poliammide	0,100mm	3,4
10			Bottom Layer	Copper	0,017mm	
11			Bottom Solder	Solder Resist	0,010mm	4,8
12			Bottom Paste			
	Height : 1.6mm	Height : 0,388mm				

17 micron copper thickness
Total thickness ~390 micron
Full flex + stiffener

Hybrid Requirements

- Chip positioning +/- 50 microns
- 2mm clearance between sensor and ASIC
- CTE matching silicon
- Accommodate bowing of sensor
- Anchor tabs for removal and replacement

SALT Data Flow and Format



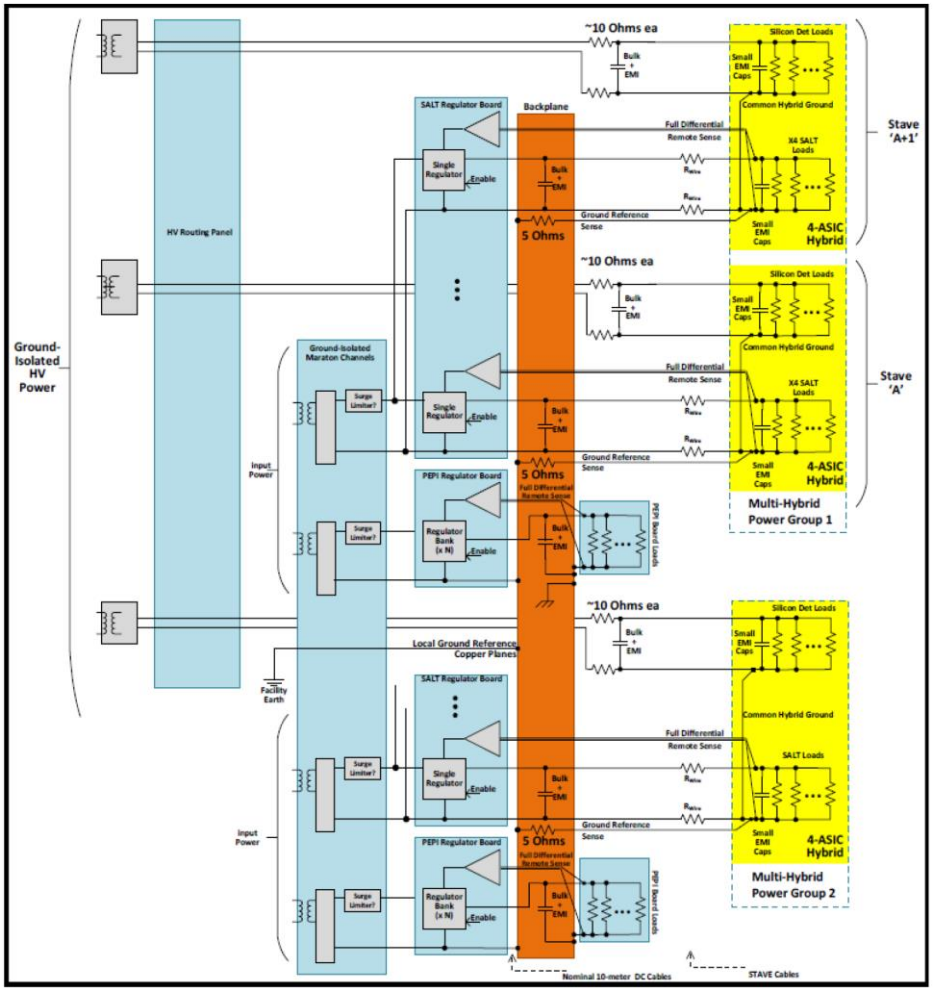
Header (12 bits)				Data	Comment
BXID	Parity	Flag	Length		
4-bit	1-bit	1-bit	6-bit	12n-bit	
0000_b	1_b	1_b	$11\ 0000_b$	not present	Idle packet (append if no enough data)
bxid	*		$01\ 0001_b$		BXVeto
			$01\ 0010_b$		HeaderOnly
			$01\ 0011_b$		BusyEvent (nHits > 63)
			$01\ 0100_b$		BufferFull
			$01\ 0101_b$		BufferFullNZS
			$00\ 0110_b$	data	NZS, true length is fixed in firmware
	*	0_b	nHits	data	NormalEvent (nHits≤63)
12-bit				pattern	Synch packet, fill one whole sub-frame (e-port lane)

Power and Grounding

Quadrant of the UTb plane style:

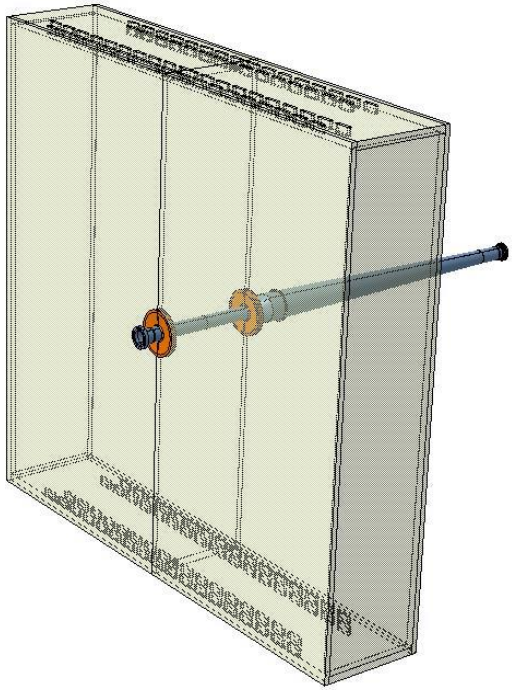
FE ASICs

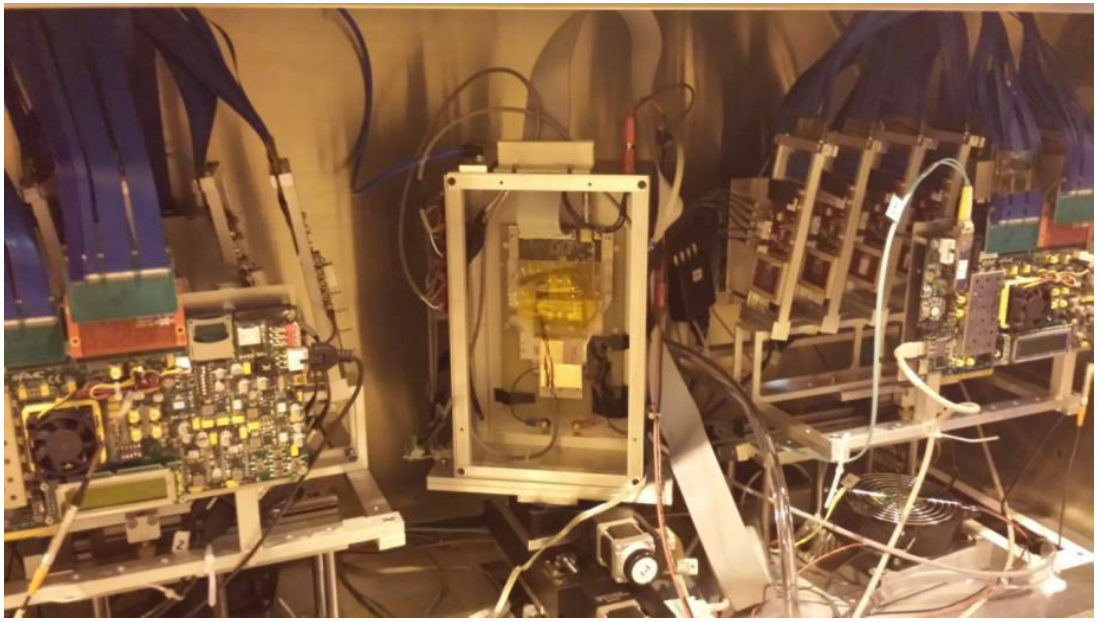
	0	1	2	3	4	5	6	7	8	Per Pwr Grp # of FE ASICs	Per Pwr Grp Total Current (Amps)	
0	4	4	4	4	4	4	4	4	4	72	38.376	Power Group 4
1	4	4	4	4	4	4	4	4	4			
2	4	4	4	4	4	4	4	4	4	72	38.376	Power Group 3
3	4	4	4	4	4	4	4	4	4			
4	4	4	4	4	4	4	4	4	4	64	34.112	Power Group 2
5	8	8	4	4	4	4	4	4	4			
6	8	8	4	4	4	4	4	4	4	68	36.244	Power Group 1
											147.108	



Detector Box

- Detector box composed of Airex foam sandwiched between layers of carbon fiber
- Two halves on rails retract for detector access front and back panels removable
- Thermal insulation to prevent moisture buildup on outside
- Gas-tight, flushed with nitrogen
- Plug surrounds beamline, composed of either polymer or Airex+Armaflex
  - Pending radiation tests
- Stave frames suspended from top of box
  - Precision of ~500 µm in X and Y, but measured to within less than 100 µm
- Prototype box produced for thermal tests – no moisture observed on outside



Sensors R&D Setup

- Read out by Beetle chips and Alibava DAQ, tracks recorded by TimePix telescope (2 µm resolution, continuous recording with timestamp)
- Phase II: DAQ changed to MAMBA (faster readout, more robust matching)