

SOI status

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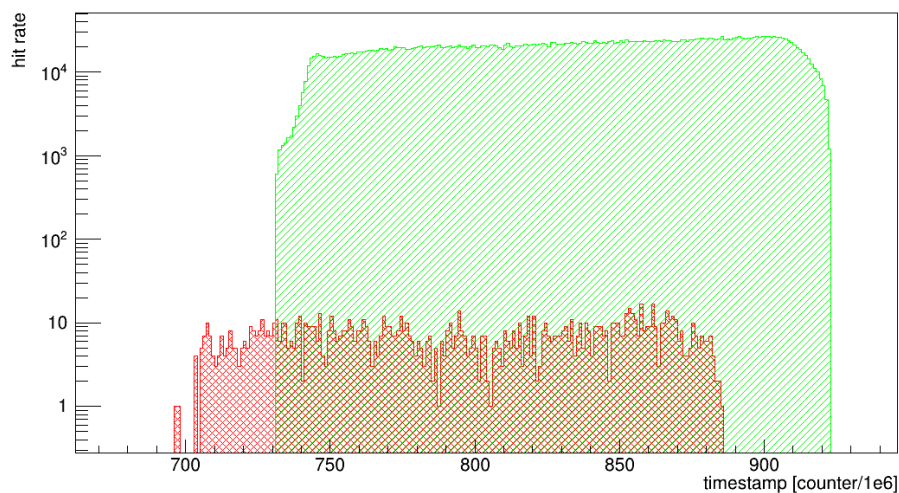
Outline

1. Preliminary results from June test beam
2. Improvements done for upcoming test beam
3. Plans for test beam

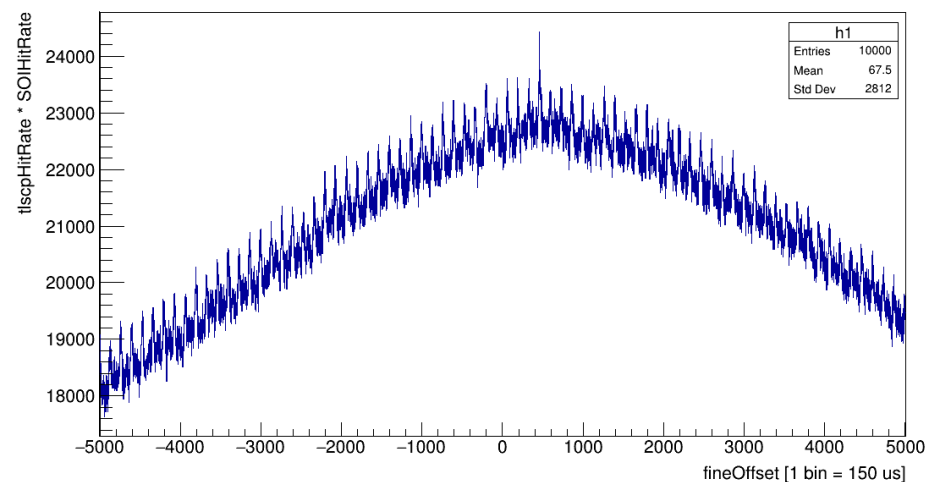
Results from June test beam – standalone analysis

- **T0 misalignment** - using the algorithm proposed by Dominik we are able to find **proper time offset** for each run

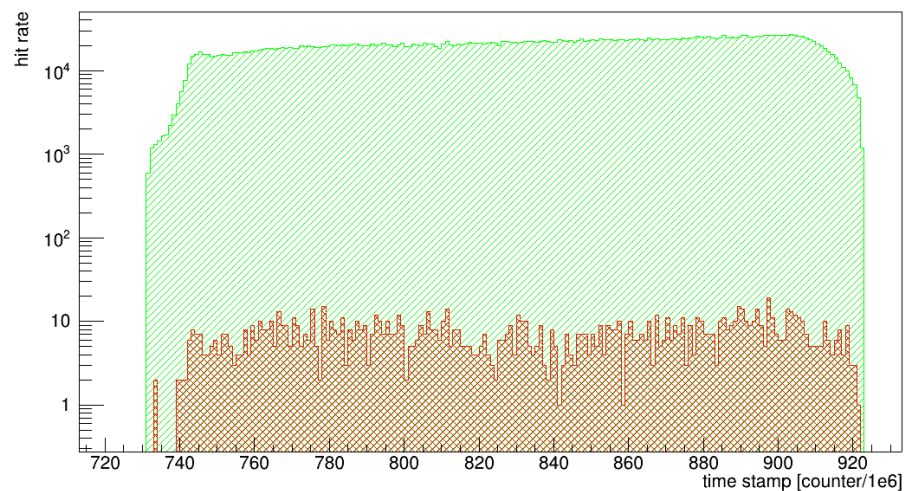
Hit Rate Comparison from SOI and telescope



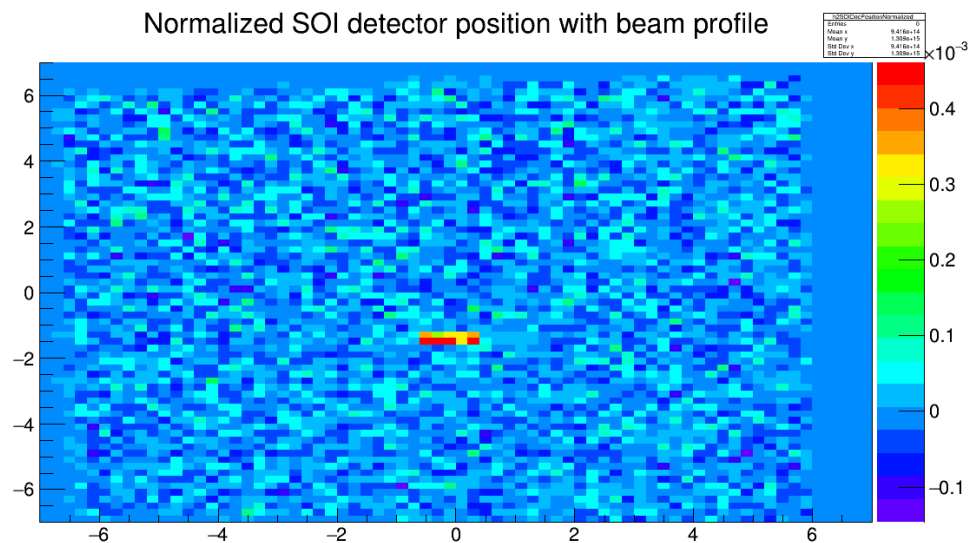
FineOffset estimation



Hit Rate Comparison from SOI and telescope



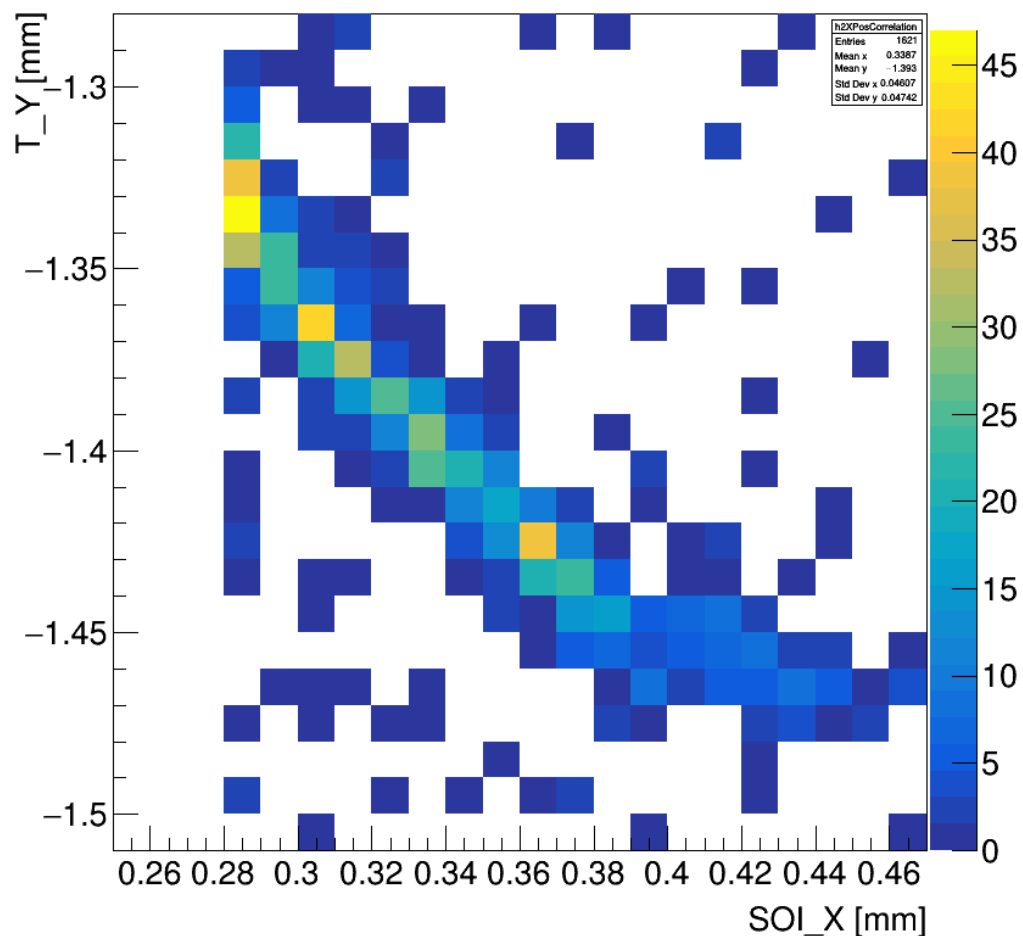
Normalized SOI detector position with beam profile



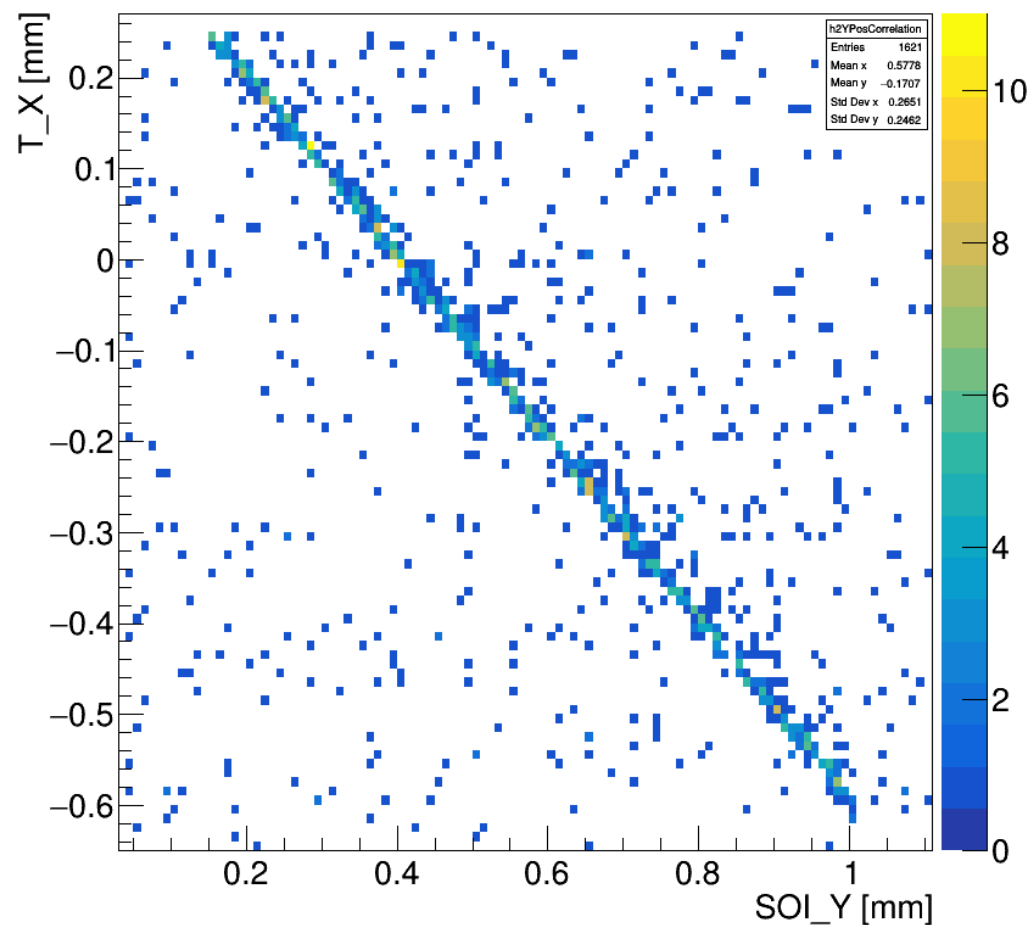
Results from June test beam – standalone analysis

- With the **proper time offset** we have observed **correlations between telescope and SOI tracks**

SOI_X vs Telescope_Y

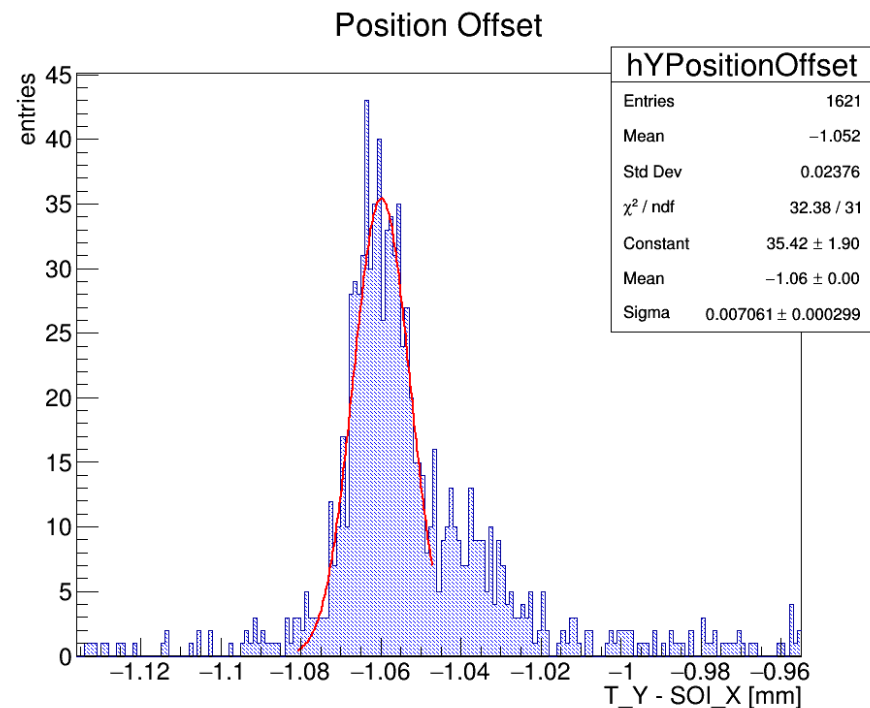
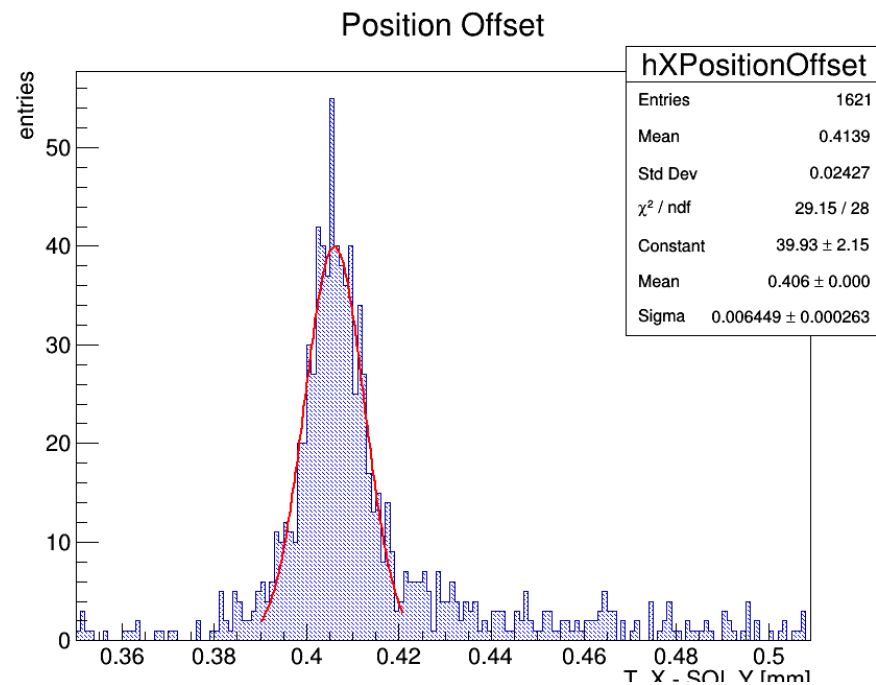


SOI_Y vs Telescope_X



Results from June test beam – standalone analysis

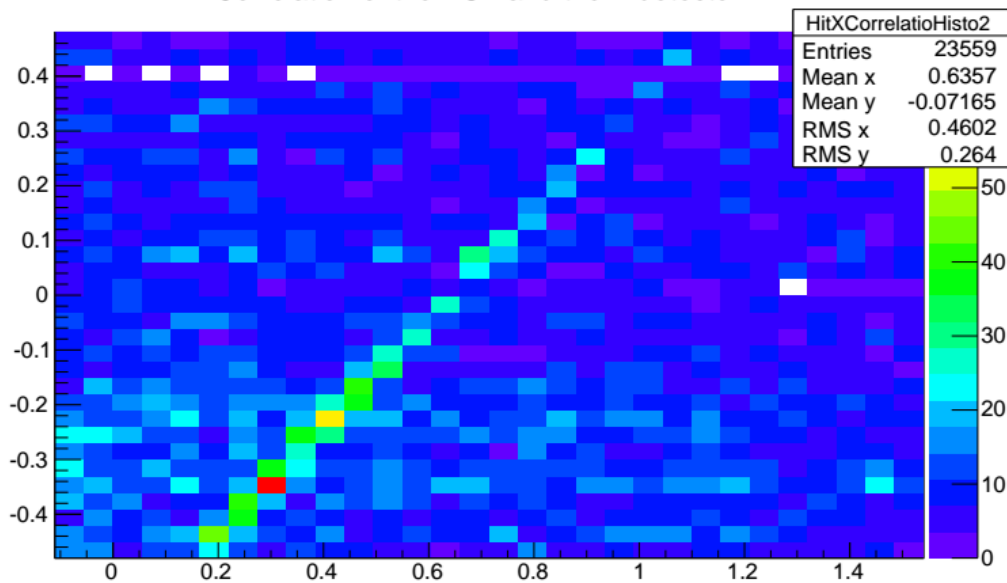
- Very first results show **spacial resolution** on the level of **6-7 μm** (pixel pitch 30 μm)
- Significant **improvement is expected**
 - No bad pixel rejection
 - No rotation correction
 - Preliminary results obtained for the whole matrix (different pixel architectures doesn't taken into account – **differences in gains not included**)



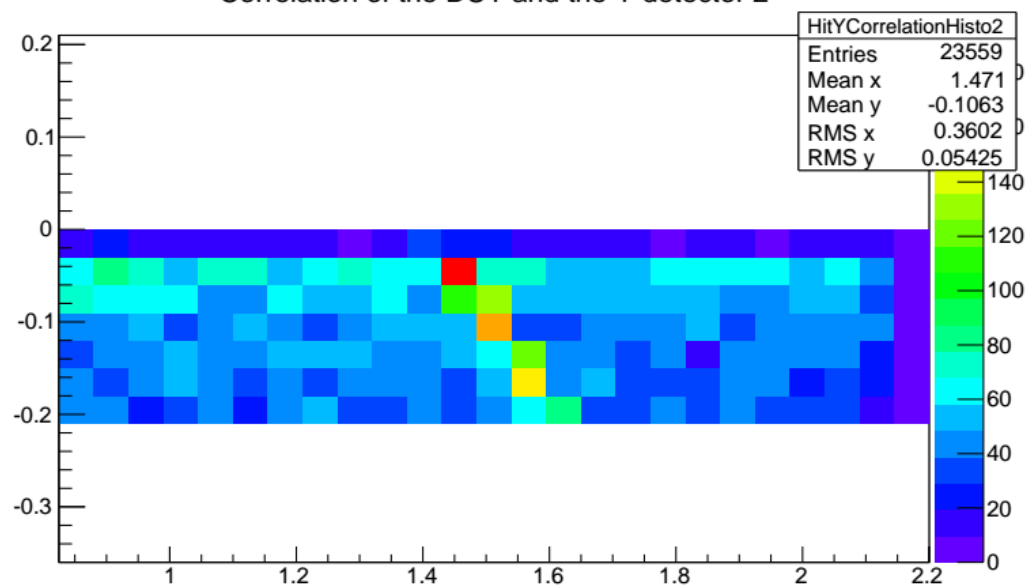
Results from June test beam – Marlin framework

- Finally the correlation between telescope and SOI tracks can be seen also **using the Marlin framework** !

Correlation of the DUT and the X detector 2



Correlation of the DUT and the Y detector 2



SOI DAQ upgrades

Firmware side:

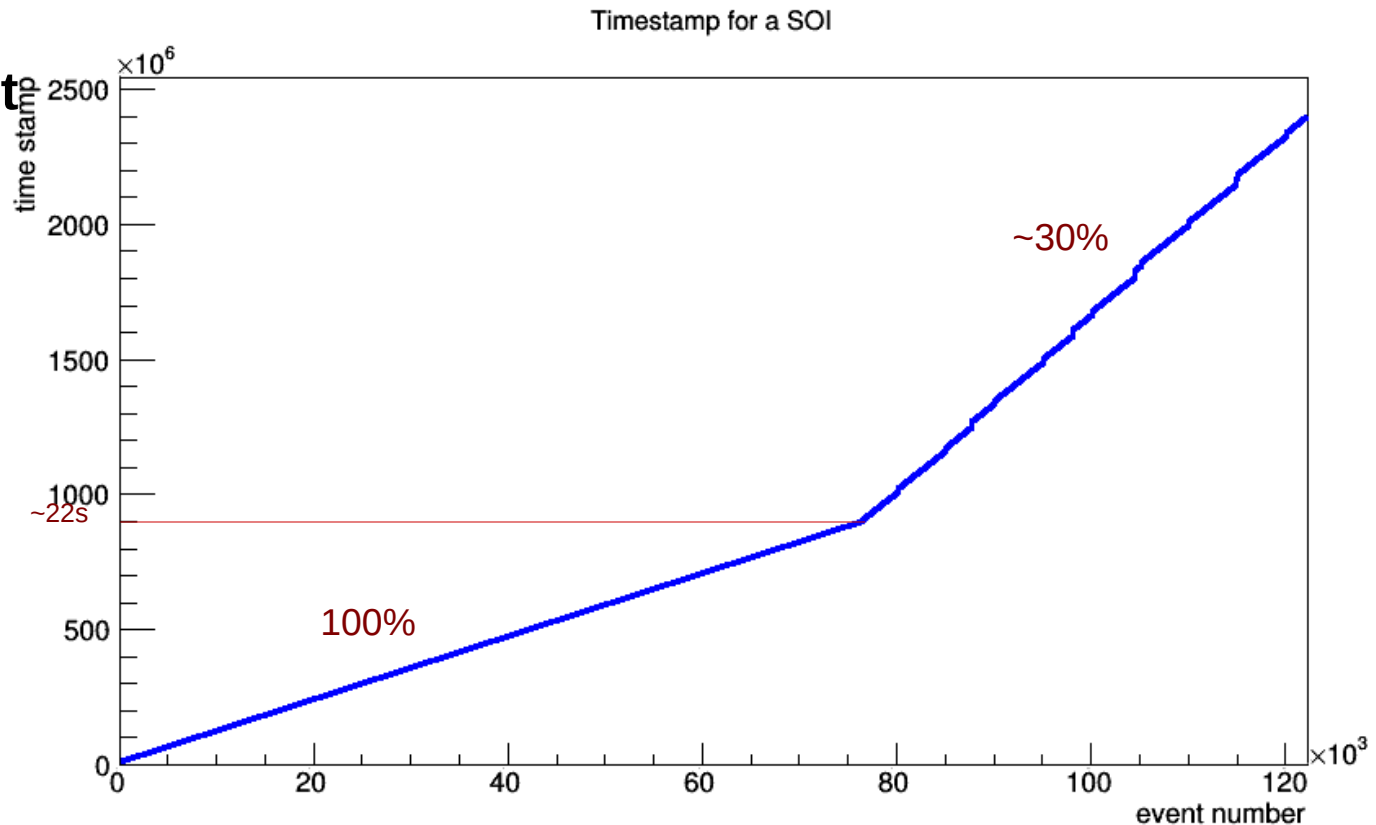
- Operating on the same **setup like in Cracow**
- **64 bit time-stamp** (instead of 32 bit)
- **Enlarged** internal FPGA event **buffer**
- “true” frame counter added (including missing frames)
- **Phase shift** between clocks added (matrix, ADC sampling, FPGA sampling)

Software side:

- **New frame structure** implemented
- **Phase shift control** added to GUI
- TCP sockets moved from `root::TSocket` to **boost::asio**
- **Multi-threading** implemented (GUI, telescope connection, DUT connection on separate threads)
- DAQ crush during automatic scans fixed
- Separate command for **DUT configuration** implemented
- T_0 misalignment seems to be fixed (beam is needed for final verification)

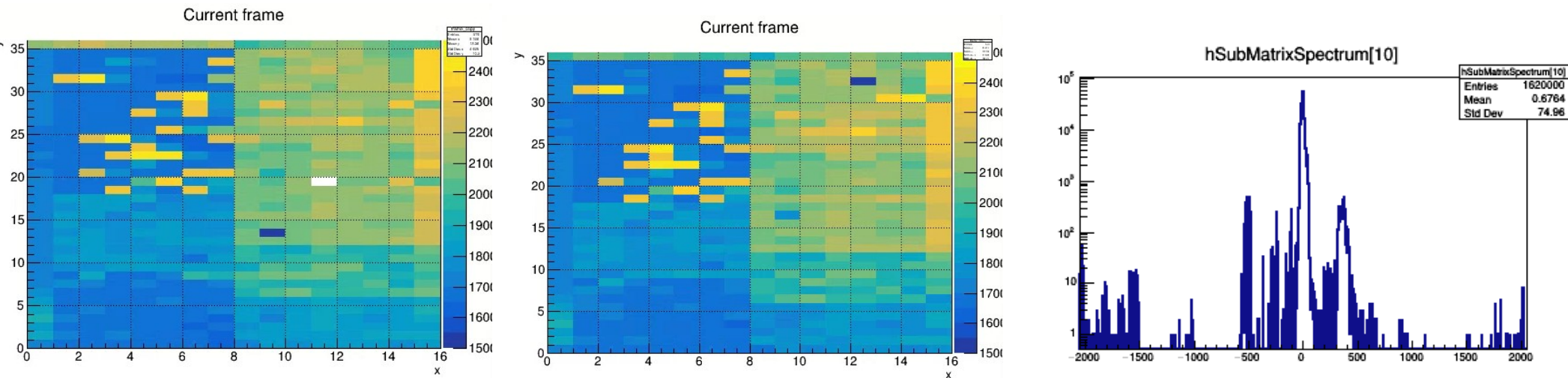
Enlarged FPGA buffer

- About **20 s of fully efficient** data taking
- After that we are able to store only about **30% of events**
- Worth to think about using external 'beam_present' signal
- No need for offline time-stamp recalculation



Issues that needs to be fixed/verified

- “**Blinking pixels**” issue still present after upgrading firmware to the newest version
- reported to Piotr, waiting for results from data taken with the Cracow setup



- New firmware version do not response on 'set_bias' command
- reported to Piotr - same thing observed in Cracow, **fixing ongoing**
- Operation exploiting external 'beam_present' signal needs to be checked

Plans for next two weeks

Before test beam

- **Fixing** reported **issues**
- **Check DAQ stability** during data taking with 'beam_present' signal

During test beam

- Mainly **focus on large statistics** (~50 spills per one setting)
- **HV bias scan** (0-150 V, 10V step)
- **3 sensors** wafers (FZN, CZN, DSOI)
- Optionally few different readout settings