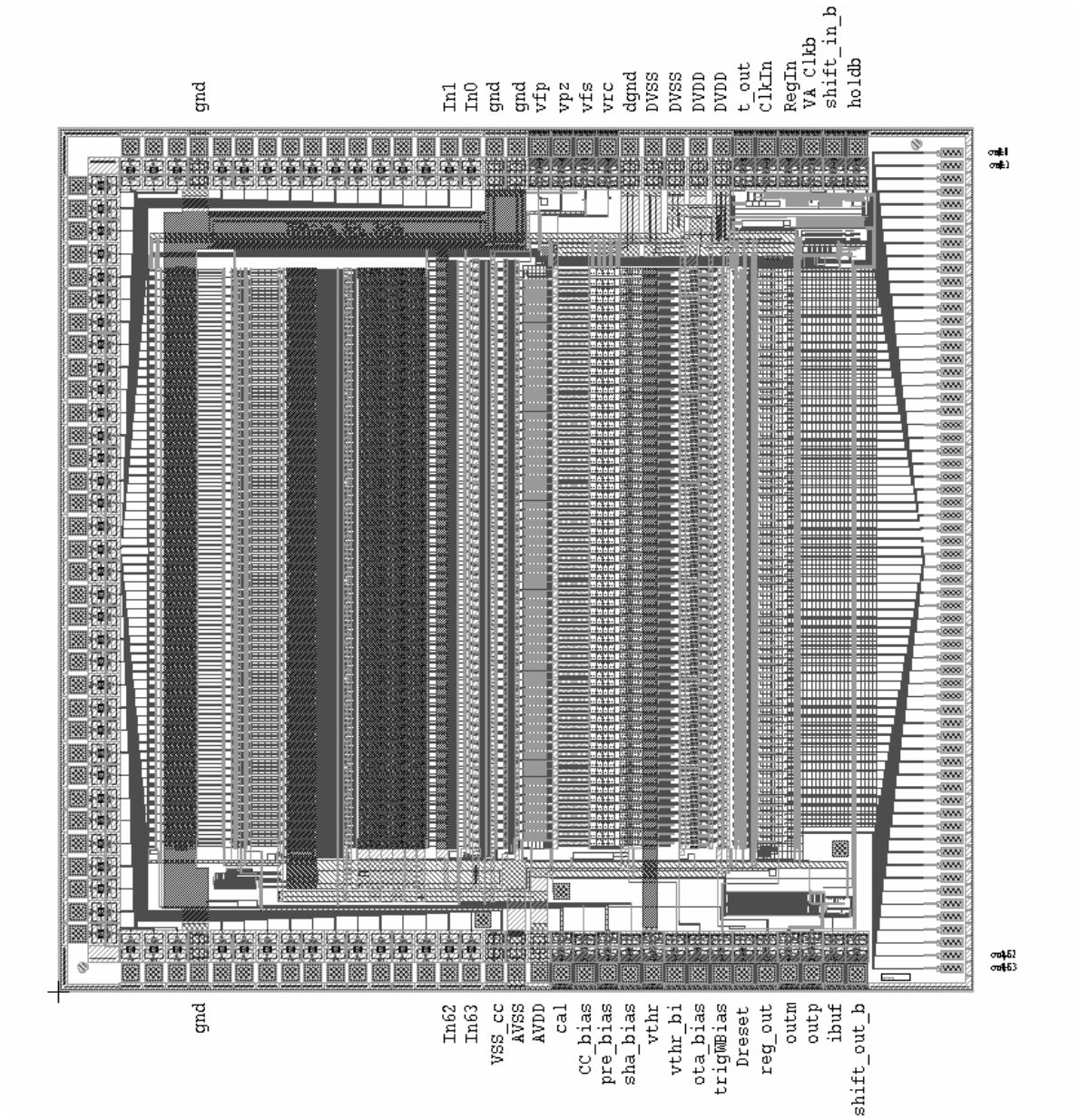
VA64TAP2.1

Documentation V0.7



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1. General

The Va64Tap2.1 is based on the Va64Tap2 design. It is a low-power, low noise ASIC optimised for moderate detector capacitances (~10pF). The gain-stage has been removed. A CR-RC fast shaper filters the output of the preamplifier. The peaking time is between 50-75ns. A Pole-Zero cancellation circuit has been implemented to minimize pile-up effects in the preamplifier and shaper. Each channel has a discriminator, with a 4-bit trim-DAC to reduce threshold spread. The ASIC has 64 parallel trigger outputs, one for each channel. The trigger is encoded as a current, and should be terminated with low impedance. An extra test channel is implemented. It can be connected to the cal-line in the same way as other channels. It can also be accessed through a direct input pad. The output of the shaping amplifiers of all channels can be connected to an analog output buffer. This read-out is controlled with an VA-style read-out engine, that also controls the enabling of the current output buffer. This feature allows for easier tuning of the pre-amp/shaper stages.

2. Physical

• Process:	0.35 µm N-well CMOS, double-poly, triple metal.	
• Die size:	5645 µm x 5330 µm Thickness: ~ 725 µm	
• Input bonding pads:	Single row on three sides. ESD protection diodes. Pad size: Pad pitch:	 90 µm x 90 µm 140µm
• Output pads:	Single row on one side. Pad size: Pad pitch:	 50 µm x 120 µm 80 µm
• Control and power pads:	Single row on upper and lower side. Full ESD protection. Pad size: Pad pitch:	 90 µm x 90 µm 140 µm

Table 1: Main physical parameters of VA64_TAP2.1.

3. Highlights of specifications

Specification	Value	Description
Peaking time	50 – 75ns	Tune biases for changing shaping time
Noise level, ENC	440e- 2400e-	Without input load and 50ns shaping time. At 50pF load and 50ns shaping time.
Lowest threshold	~2fC theoretical ~10fC in practice	Due to channel variations, the desire for stable operation and so on, 10fC is a practical lower level for the threshold. At high rates 10fC may not be optimal, due to return-to-baseline or baseline-shift related effects.
High rate performance	2.5MHz uniform rate will produce triggers for signals between 16 and ~160fC	
Signal polarity	Optimised for negative input charge	
Linear range:	-200 to +160fC	

Table 2: Highlight of specifications

4. Pad descriptions

The output, control and power pads are listed in the following table clockwise from the upper left. The 64 parallel inputs and outputs are omitted from the table. Positive current direction is into the chip. All voltages are listed assuming an ASIC powered with VDD and VSS as described in the table.

Pad name	Type	Description	Nominal value	Nominal voltage (for cur. biases)
Gnd (2)	P	Signal ground. (AGND)	0 V	
Vfp	ai	Control voltage to feedback resistance in pre-amplifier. Internally generated.	500mV	
Vpz	ai	Control voltage to feedback resistance in gain stage. No internal generation.	~800mV	
Vfs	ai	Control voltage to feedback resistance in shaper-amplifier. Internally generated.	700mV	
Vrc	ai	Control voltage for High-pass filter resistor (NMOS) in front of Discrim. Internally generated.	-1.0V	
Dgnd	p	Ground. Reference for signal input of discriminators. Typically connected to AGND.	0 V	
Dvss (2)	p	Digital Vss	-2 V	
Dvdd (2)	p	Digital Vdd	+1.5 V	
T_out	do	Common trigger output for all channels. Open drain current into the chip. Switchable with control bit.	Logical, current	
Clkin	di	Clock Input for register	Logical	
Regin	di	Input to the register	Logical	
Va_clkb	di	clock for test mode read-out register, see fig.3. Internal 10Kohm pull up to Dvdd.	Logical	
Shift_in_b	di	start pulse for read-out. Internal 10Kohm pull up to Dvdd.	Logical	
holdb	di	used to hold analogue data, see fig.3. Internal 10Kohm pull up to Dvdd.	Logical	
Shift_out_b		Do not connect		
Ibuf	ai	Bias current for current output buffer for the test channel.	+220 µA	450mV (If enabled)
Outp	ao	Current output for monitoring the test channel, positive phase.	Typical swing is ±350uA full scale	
Outm	do	Current output for monitoring the test channel, negative phase.		
Reg_out	do	Output of register	Logical	
Dreset	di	reset of test circuitry. Internal 10Kohm pull down to Dvss.	Logical	
TrigWBbias	ai	Bias adjust for trigger width. Internally generated.	-4 µA	440mV
Ota_bias	ai	Bias current to Discriminator. Internally	+120 µA	410mV

		generated.		
Vthr_bi	ai	Bias for trim-DACs. Internally generated.	+10µA	-1240mV
Vthr	ai	Discriminator threshold	-50mV (e.g)	
Sha_bias	ai	Bias current for shaper-amplifiers. Internally generated.	+90 µA	-1030mV
Pre_bias	ai	Bias current for pre-amplifiers. Internally generated.	+500 µA	-720mV
CC_bias	ai	Bias Leak-current compensation. Internally generated.	+2µA	615mV
Cal	ai	Test input signal	e.g. -20fC	
Avdd	p	Analogue Vdd	+1.5 V	
Avss	p	Analogue Vss (+ chip backplane)	-2 V	
VSS_CC	p	=AVSS filtered (~ no current)	-2V	

Table 3: Pad/Signal descriptions

In Table 3 the following applies:
p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out.

5. Functional description

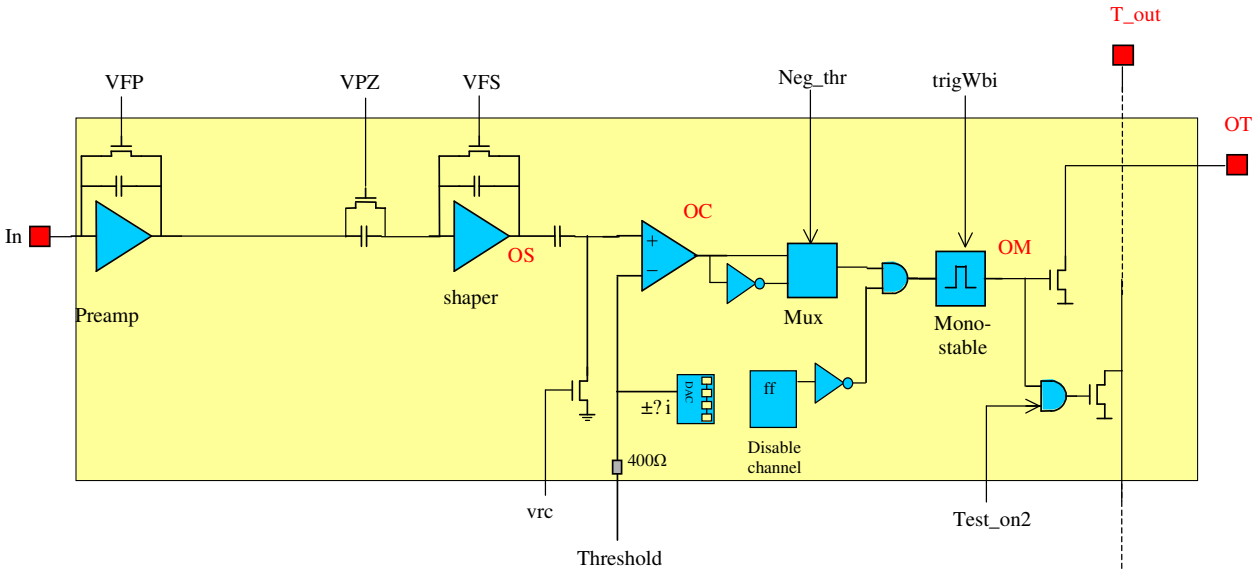


Figure 1: VA64Tap2.1 Channel Architecture.

The Va64Tap2.1 channel is shown in Figure 1. After the preamplifier, the signal is noise filtered by the shaper, that has a peaking time of ~70ns. Pole-Zero cancellation of the preamplifier can be adjusted with the *vpz* bias that controls a resistor connected in parallel with the coupling capacitor between the shaper and the preamplifier. A high pass filter is situated after the shaper to remove offsets on the input signal to the discriminator. The Discriminator offset is also reduced by a 4 bit trim-DAC. The trim-DAC adds or subtracts current through a resistor placed in series with the global on-chip threshold line. The DAC has 1 mV steps with nominal biases. When tuning the

DACs, optimal performance is obtained if the current from the trim-DACs in the various channels zeros out, meaning no net current is flowing out of the chip.

The discriminator output, *OC (see figure),* should be inverted by selecting the inverted output if the discriminator threshold is negative. This is the default mode for negative charges, and can done by setting the control bit *'neg_thr'*.

Setting the according channel bit to '1' in the disable register can disable any channel. If the channel is not disabled, a signal that triggers the discriminator will be made into a square pulse with a duration controlled by the '*trigWBias*'. The parallel trigger output, *OT,* is an open-drain current that should be terminated with a low impedance in order to avoid pick-up in other channels. It can be connected directly to the input of the LS64 ASIC.

ASIC Test mode

The test mode read-out circuitry is described in Figure 2. The output *a* of the shapers are connected to the inputs of a 64 channel multiplexer. The switches in the multiplexer are controlled by a bit-register, and can be used to read out all channels serially.

The output of the multiplexer goes directly out of the chip via the differential output buffer (*signal* = ***outp*** - ***outm***). Only one of the switches in the multiplexer can be ¨on ¨ simultaneously. Thus, only one channel can be seen at a time on the ASIC output. The bit in the register is clocked sequentially from the first to the last channel by clocking *VA_clkb*. The clock can be stopped at any point, which will leave the connection between the current channel and the output.

The timing diagram for a normal read-out sequence is shown in Figure 3. After the physics event, each channel will integrate and filter the charge for a time given by the peaking time Tp. At this point, the external *holdb* signal should be applied to sample all channels. The sequential read-out of the channels can be started by activating the output bit-register using overlapping *shift_in_b* and *ckb* signals. The analog data from channel 0 will appear on the output after the first negative flank of *ckb*. The analog output buffer will be tri-stated prior to the read-out, and will be activated simultaneously with the appearance of the data of channel 0. The settling time for the analog output might therefore be slightly worse than for the other channels. Typical maximum clock frequency is 10MHz, but this is only possible with a good external receiver and low load.

The serial read-out of the ASIC has been designed for daisy-chaining several ASICs on the same output bus. This is achieved by connecting the output signal of the first ASIC's shift register (*shift_out_b*) to the next ASIC's *shift_in_b* pad. The *shift_out_b* signal from the first ASIC will appear after the positive edge of *ckb* during the data output of the last channel. The next negative transition of *ckb* will enable the next ASIC's read-out circuitry.

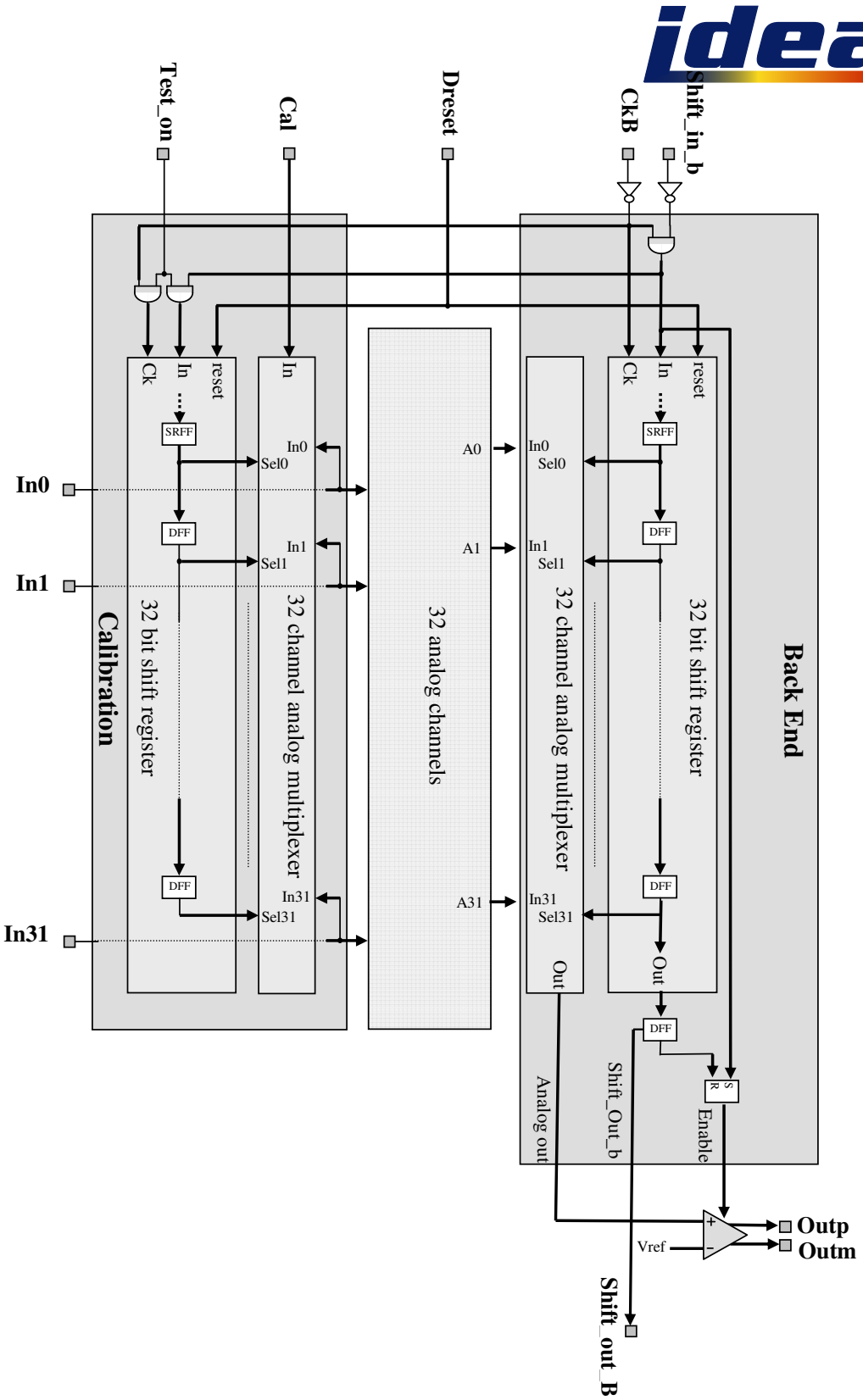


Figure 2: Overview of the ASIC Back End and Calibration circuitry. The calibration circuitry is described in section 0).

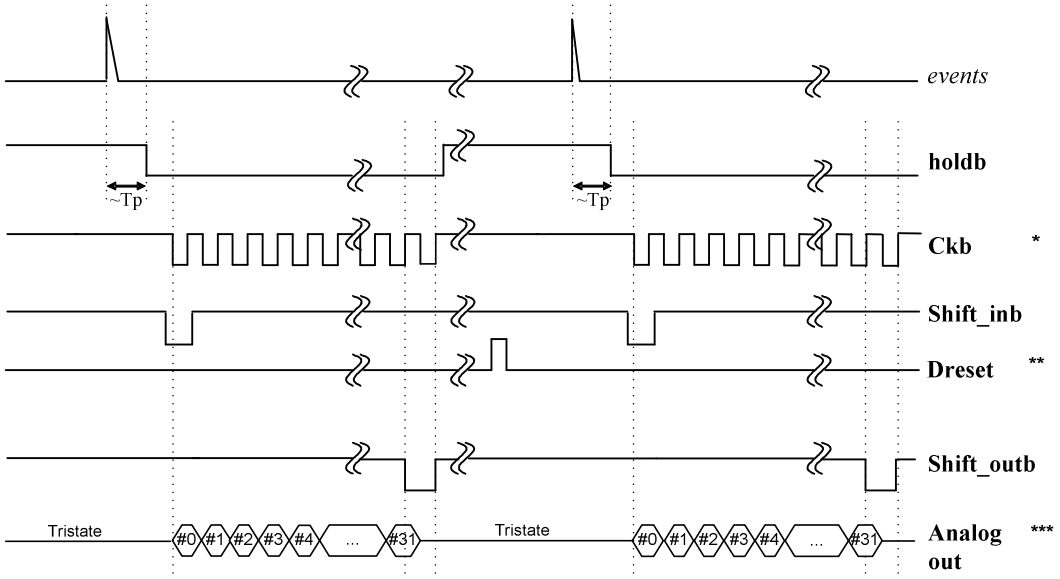


Figure 3: **Timing diagram for readout of the VA. After an event, holdb is applied, to sample and hold the shaper.**

Initialisation of the test mode

The ASIC will always be in an initialized state after *dreset* is applied, or after a normal read-out sequence without *dreset*.

Test and Calibration

Each channel can be tested individually without connecting the input. This can be done by enabling the calibration circuitry (described in Figure 2) with the *test_on* signal. This will enable another multiplexer/bit-register on the input to run in parallel with the output multiplexer used during normal serial read-out. This input multiplexer connects one of the preamplifier inputs to the *cal* signal. As for the read-out described in section 0, only one connection at a time is possible. This connection corresponds to the same channel that is connected to the output buffer.

When using the cal signal, place a capacitor very close to the ASIC to prevent pickup. Apply a voltage step to inject a calibration charge. A voltage step of 500 mV on a 47pF capacitor gives an input signal charge of 23.5 pC. Some additional noise due to routing and coupling of signals has to be taken into account when operating the ASIC with calibration pulses.

An additional feature is implemented in the channel to facilitate testing. If the global control register bit '*test_on2'* is set, an additional trigger output '*t_out'* is enabled. The *'t_out'* is available through an external pad. This node is connected to all channels in parallel, to form a wired-OR, meaning that a trigger on any channel will be possible to monitor on this line.

A 65th channel is implemented for test purposes. This channel is identical to the 64 normal channels, but has no parallel trigger output. The output of the shaper in this channel is available on the '*outm'* and '*outp'* outputs of the differential-current test buffer. Setting the *'ero'* control bit high turns the buffer on. The channel is accessible through the '*Cal*' and the '*InTEST*' pad.

6. Adjusting the return to baseline

The most important parameters for adjusting the return to baseline for the system, is the peaking time, the high pass filter before the discriminator and the pulse width of the trigger.

Adjusting the peaking time

The shaping time can be adjusted externally by the two bias-pads '*Vfs'* and '*Sha_bias'*. Adjusting one will influence the effect of the other.

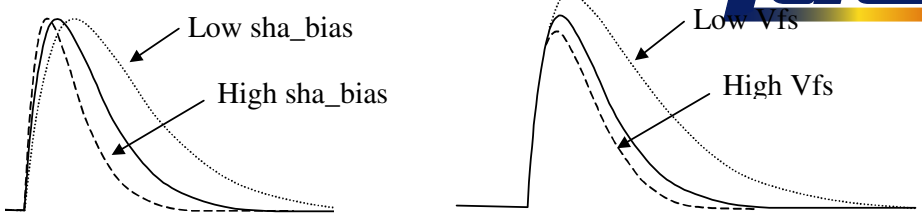
Changing the *'Sha_bias'* will change the dc-level of the input (since the Vgs of the input PMOS transistor has to increase/decrease as response to the change in current). This dc-level represents the source-voltage of the feedback NMOS transistor, and with an unchanged '*Vfs'*, the Vgs of this transistor will consequently change. Therefore, to maintain the same resistance value, '*Vfs'* must change correspondingly to the change in the input dc-level caused by a change in '*Sha_bias'*.

This will consequently affect the shaper output signal in two ways:

1. The change in feedback resistance will cause a change in the time-constant of discharding the feedback capacitor meaning that the differentiation time, or fall-time, will change. Reduced resistance (increase of *'Sha_bias'*) will cause a shorter fall-time and vice versa.
2. Changing *'Sha_bias'* will also affect the rise-time of the shape because the transconductance of the input transistor will change. Increase of *'Sha_bias'* will cause faster rise-time and vice versa. Consequently, combining this with the previous point, an increase of '*Sha_bias'* will increase the rise-time and decrease the fall-time which will reduce the peaking-time.

Only changing the '*Vfs'* (keeping '*Sha_bias'* constant) will affect only the fall-time but the effect will be stronger.

A good shape depends on the requirements. Nominally, the shape should be an ideal semi-gaussian CR-RC shape, but it is not necessarily so. Generally, it is advantageous to minimize the "tail" of the signal (fall-time) since this part conserves the DC component of the signal and hence a long tail will make the amplifier more sensitive to the parallel noise (detector leakage-current noise and biasing-resistor noise).



Only adjusting sha_bias Only adjusting Vfs

Figure 4: Effect of adjusting Vfs and Sha_bias

Clearly, the desired shape will most often be found by adjusting both parameters.

Adjusting the preamplifier return to baseline and the Pole-Zero

Ideal noise performance is normally obtained with a large feedback resistor in the preamplifier. However, at high rates, this may not any longer be ideal due to baseline shift of the preamplifier output. In extreme cases, this will saturate the preamplifier when the frequency becomes too large. When reducing the preamplifier feedback resistance by changing '*vfp'*, an undershoot may occur in the shaper. This can be compensated by tuning the *'vpz'* bias, which controls the resistance of a resistor connected in parallel to the coupling capacitor between the preamplifier and the shaper.

Adjusting the high pass filter

The high-pass filter in front of the discriminator should be optimised in order to make sure that it does not affect the return to base line. The time constant of the filter should be as low as possible without introducing damping of the signal. The resistance of the filter is implemented with a NMOS connected to DGND. The resistance can be tuned through the '*Vrc'* bias pad. To reduce the resistance, increase the voltage.

Adjusting the trigger pulse width

The pulse width of the ASIC output signal should be made short enough to not introduce any ambiguity to which cycle it belongs. The default pulse width is 50ns. The pulse width is inversed proportional with the '*trigWBbias'* bias. Thus, increasing the bias will give a shorter duration of the output pulse.

7. Control register

Clocking in a serial bit pattern, using Clkin and Regin pins, sets the ASIC control register.

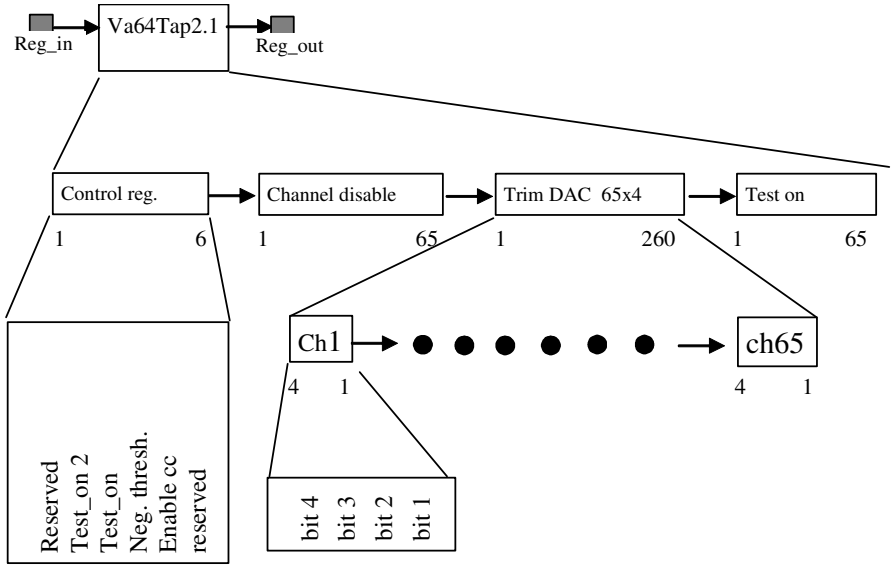


Figure 5: Bit ordering in the control register.

Thus the first bit clocked in on reg_in is Test_on ch#65 (the test channel), then subsequent bits comes in accordance with the figure above.

Control register details

'Test_on_2' is used for parallel testing and *'Test_on'* is for single channel testing.

See details on these 2 control bits in section 6.

'*Neg. thresh.'* relate to the threshold voltage polarity, see Table 4.

Input signal	Positive	Negative
Neg. Thresh.	0	1
Threshold polarity	Positive	Negative

Table 4: Relation between input signal polarity and *'Neg_thr'* setting.

'Enable cc' enables current compensation. *'Reserved'* is always set to '0'.

Trim DAC bits

Trim Value	Bit1	Bit2	Bit3	Bit4	Offset change (mV)
0	0	0	0	0	None
-1	0	0	0	1	- 1
-2	0	0	1	0	- 2
-3	0	0	1	1	- 3
-4	0	1	0	0	-4
-5	0	1	0	1	-5
-6	0	1	1	0	-6
-7	0	1	1	1	-7
0	1	0	0	0	None
1	1	0	0	1	+ 1
2	1	0	1	0	+ 2
3	1	0	1	1	+ 3
4	1	1	0	0	+4
5	1	1	0	1	+5
6	1	1	1	0	+6
7	1	1	1	1	+7

Table 5: Effect on channel threshold by adjusting 4-bit trim-DAC.

It is advised to set trim DAC settings such that the sum of all ‘trim values’ (see Table 5) are zero.

Clocking of control register

The control register is a serial register of positive D-flip-flops. Data are clocked into the register on the positive edge of ‘Clkin’. Allow 10ns setup time between setting a value (‘0’ or ‘1’) on ‘Regin’ pin and the positive clock edge of ‘Clkin’. Clock frequencies up to 1MHz is supported for the VA64_TAP2.1. Regsiter information is static, i.e. register data is retained unless ASIC is powered down or register is altered by clocking ‘Regin’.

All control register pins, ‘Regin’, ‘Clkin’ and ‘Regout’ are referred to the ASIC supplies DVDD and DVSS. These supplies are nominally +2V amd -2V. This means that logic ‘1’ is a voltage close to +2V and logic ‘0’ is a voltage close to -2V. Since ‘Regin’ and ‘Clkin’ are normal CMOS inputs, normal CMOS switching characteristics apply, meaning that voltages in the range 30%-70% between the supplies are regarded as undefined. For a +1.5/-2V supplies this means 0.45V to 1.5V is to be regarded as logic ‘1’ and -0.95V to -2V is to be regarded as logic ‘0’. In practice one will experience that probably voltages above 0.7V will be regarded as ‘1’ whereas below -0.7V wil be regarded as ‘0’.

8. ASIC pad position description

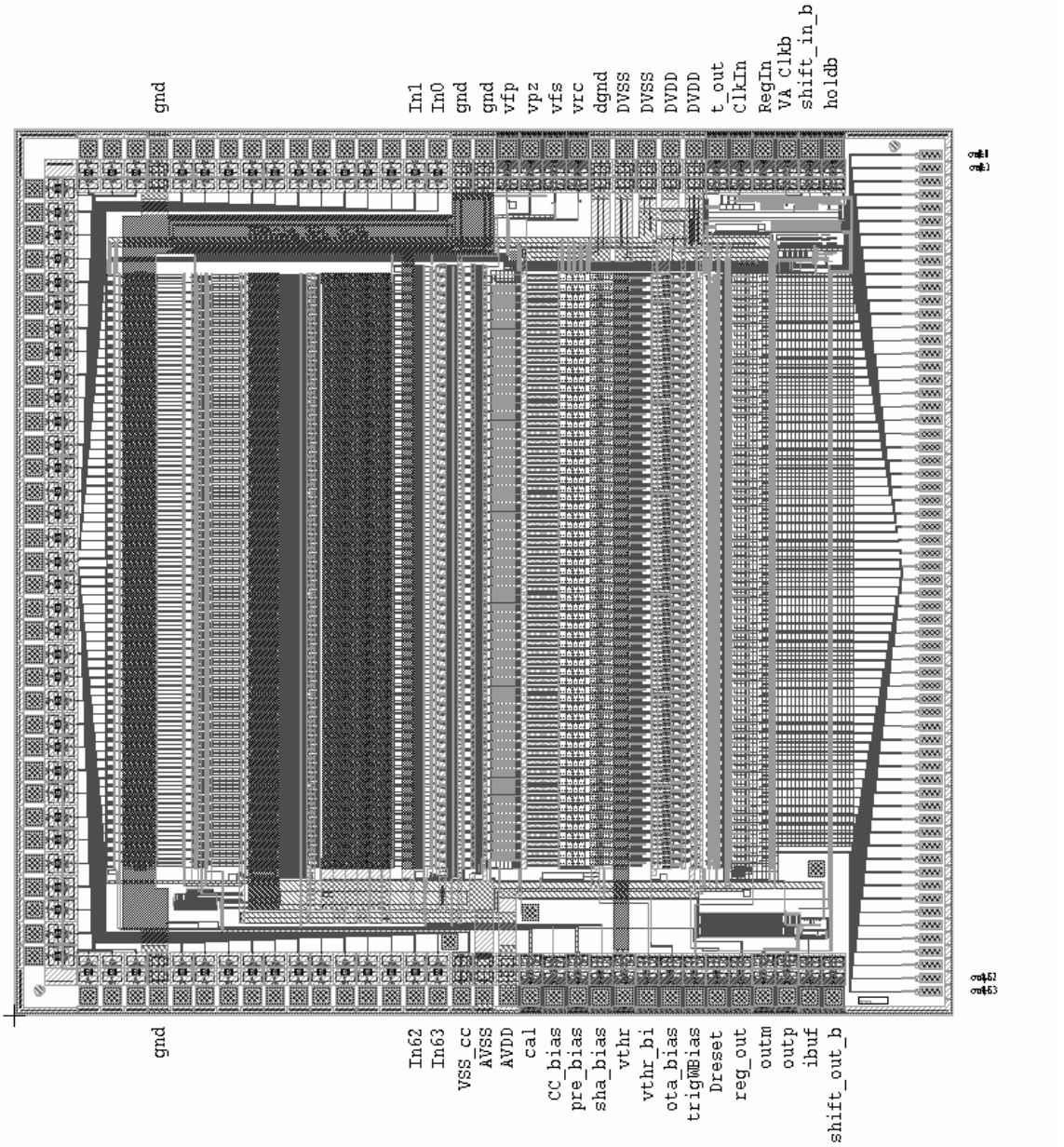


Figure 6: Chip plot of VA64_TAP2.1.

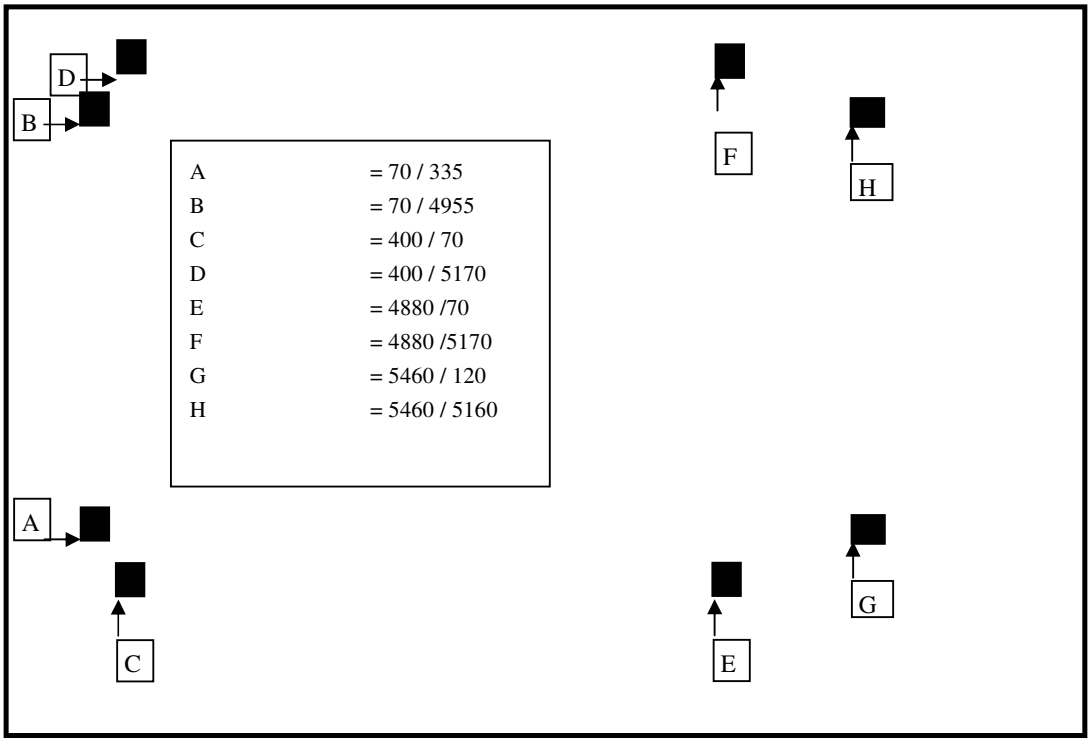


Figure 7: Chip geometry & pad placement. Total die size: 5605 µm x 5380 µm

Figure 7 is not to scale. All dimensions are in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50-100 µm on each side for scribe/cutting tolerances).