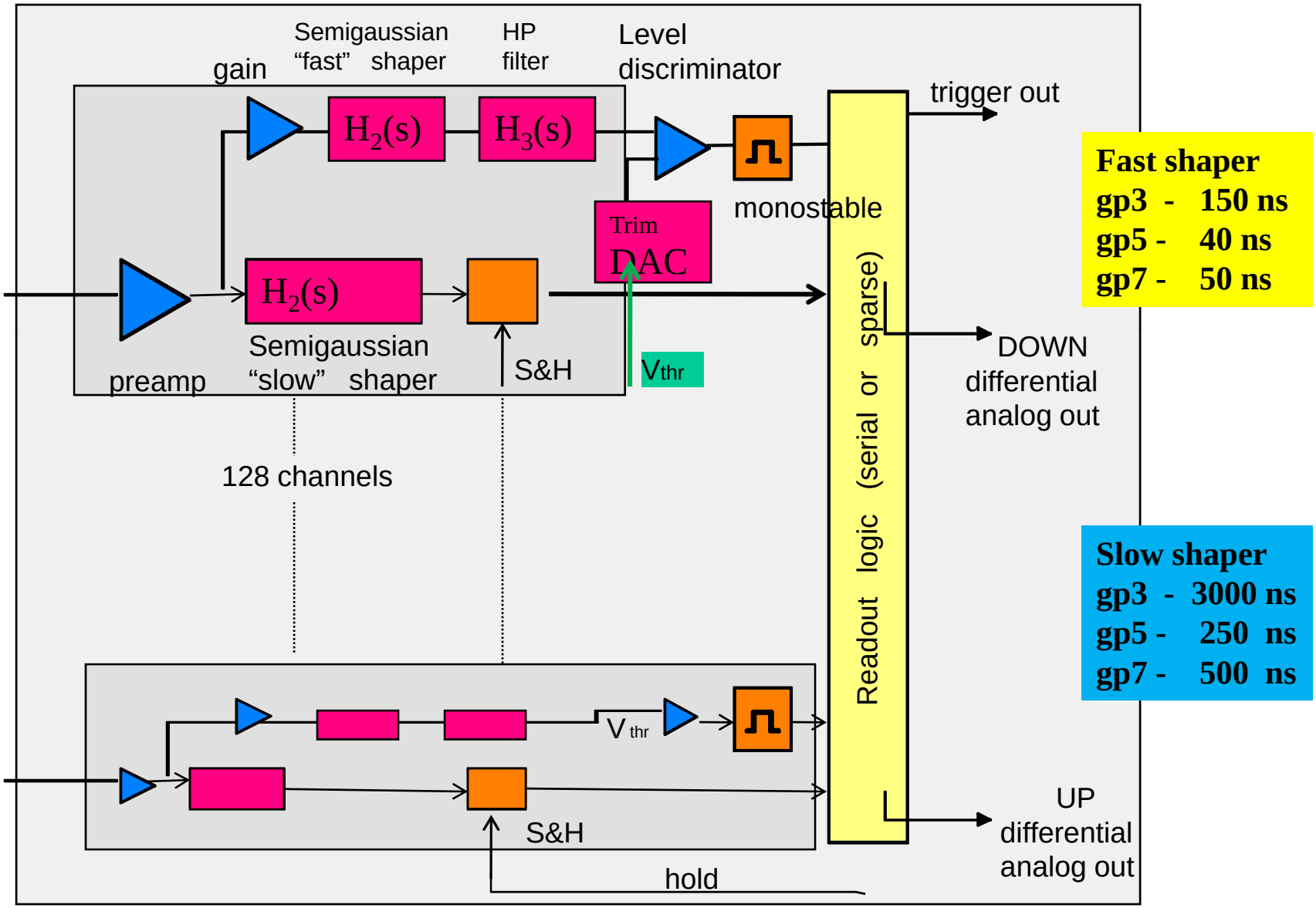
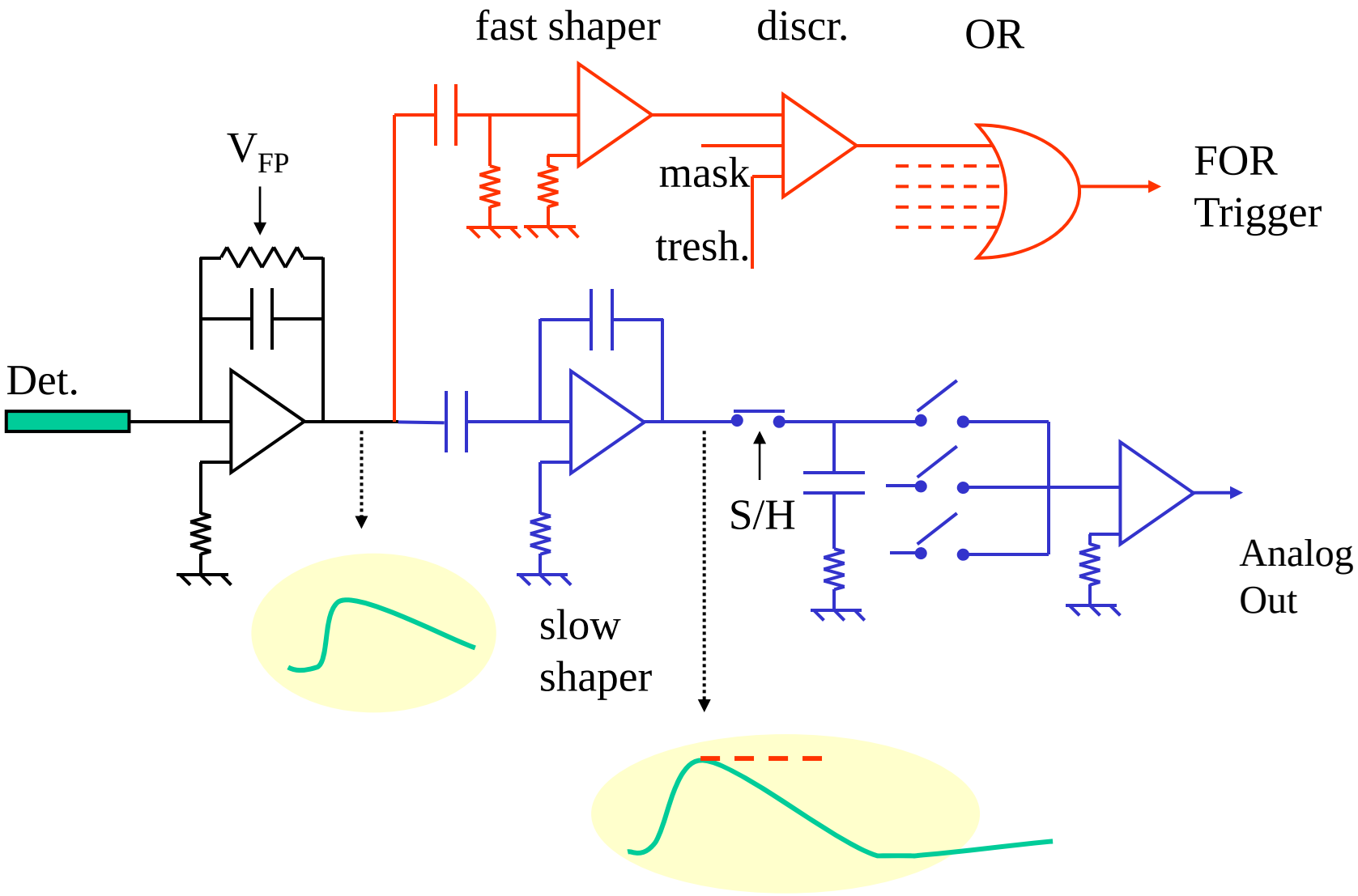
This presentation about how we used some IDEAS chips.

1. Information about IDEAS chips can be found on www.ideas.no . Also files with description about principles of those chips, tables with chips produced ....
2. Here only about some readout principles that can be important for creating “Scalable and Portable Readout Systems”.
3. Also about some small DAQs that we used and we ready to share all experience with those DAQs that can be useful.

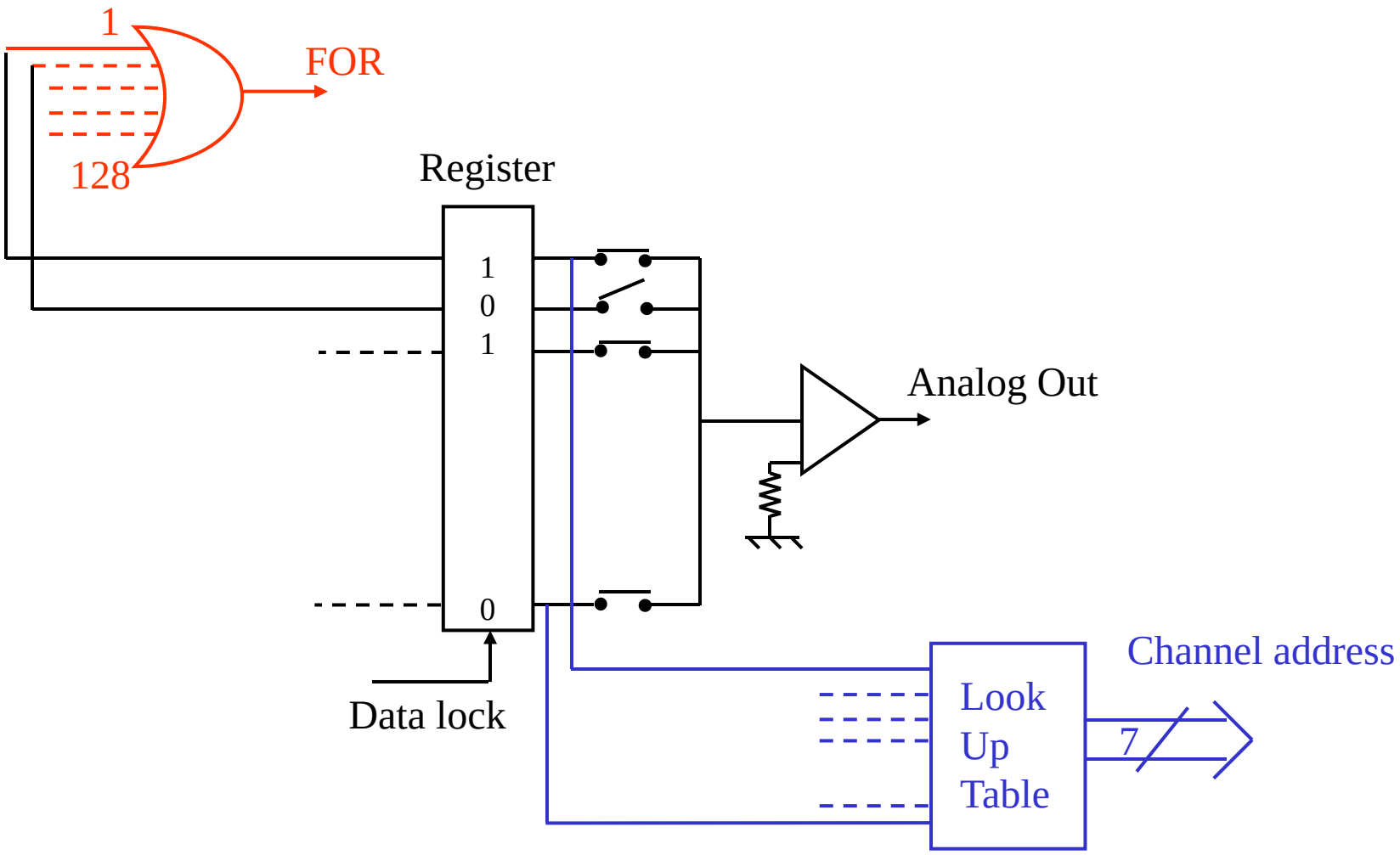
VATA-GP3 -5- 7 block diagram



VATA-GP 3-5-7 Principle of serial readout



VATA-GP5 Principle of sparse readout



„Trigger family“ chips, produced by IDEAS.

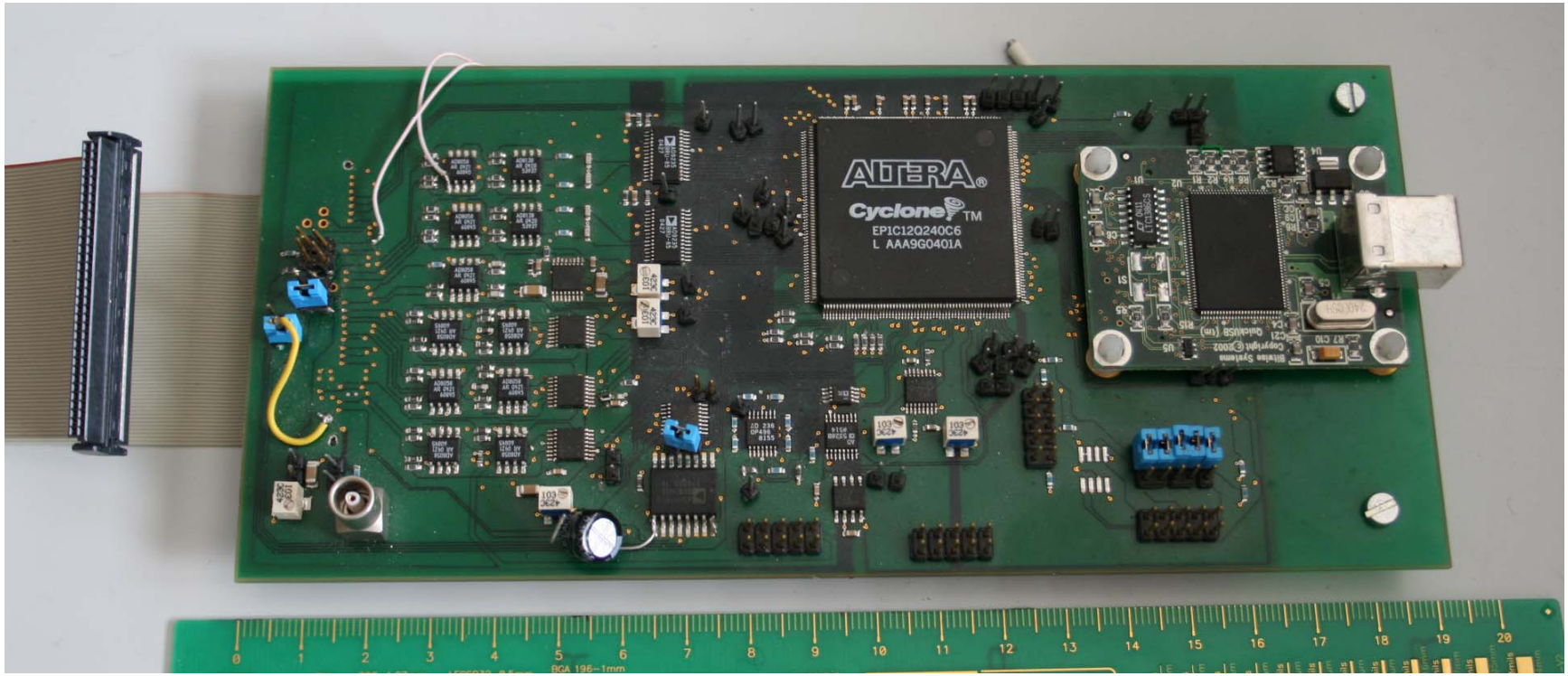
Trigger Family

Chip	Feature	Detector load (pF)	Readout	Dynamic Range (fC)	#Ch	Gain (µA/fC)	Noise (rms, e-)	Tp [1] (CR-RC)	Process	Input cap.	Feedback cap. (pF)	fu	Measured	External biases	Ex
TA1	VA-type CSA with Wired-Or Trigger Output	Medium	Serial Analogue Readout; Trigger Output	36	128	20	162 + 6.1pF	2µs	1.5u amsw						
Ta1	VA-type CSA with Wired-Or Trigger Output. Low power.	20-100	Serial Analogue Readout; Trigger Output	36	128	18		2µs	0.6u amsw+		0.2			No	C
TAN	Part of the VAN-TAN chip-set; Energy Window Discriminator		Digital Address Output; Trigger Output. Use with VA32_75/500		32				1.5u amsw						
TA32C	Part of the VA-TA chip-set [3]		Trigger Output		32			75ns	1.5u amsw						
Ta32cg	Fast shaper and discriminator				32			75ns-150ns	1.5u amsw						
Ta32cg2	Fast shaper and discriminator		Use with 32ch VA-chips		32			75ns-150ns	0.6u amsw+						
Va1Ta	VA1 with trigger functionality		SEU proof		128	10		0.6µs	0.35u mixed						
Va2_Ta (VA2TA)	One Dic VA2 + TA [3]	Medium	Serial Analogue Readout; Trigger Output		128				1.5u amsw						
Va32Ta	Similar to VA32c+TA32		SEU proof		32			2µs	0.35u mixed						
Va32Ta2	VA-type CSA with Wired-Or Trigger Output (close to HDR2)	~6	Serial Analogue Readout; Trigger Output	1000	32	0.8	800 + 3fpF	2µs	0.6u amsw+		0.5			Yes	(
Va32Ta2.2	VA-type CSA with Wired-Or Trigger Output (close to HDR2)	~6	Serial Analogue Readout; Trigger Output	1000	32	0.8	710 + 3fpF	2µs	0.6u amsw+		0.5			Yes	(
VA32Ta3.2					32				0.6u amsw+						
Ma32	Counter ASIC		Use with VA32_75/500		32				0.6u amsw+						
Va64Tap	VA-type Amplifier with Parallel Trigger Output. High gain (HPDs)	~10	Parallel Trigger Outputs (LS64 convert par. outputs to TTL)		64		500 + 50fpF	75ns	0.6u amsw+		0.15			Yes	(5
Va64Tap2	VA-type Amplifier with Parallel Trigger Output. Low gain (PMTs)	~10	Parallel Trigger Outputs (LS64 convert par. outputs to TTL)		64		500 + 50fpF	75ns	0.6u amsw+		0.15			Yes	(5
Vatagp			GP spares readout family		128			3µs	0.6u amsw+						
Vatagp2	Obsolete, use ver 2_2		GP spares readout family		128	44		3µs	0.6u amsw+						
Vatagp2_2			GP spares readout family		128	44		3µs	0.6u amsw+						
Vatagp3			GP spares readout family		128				0.6u amsw+						
Va_Tdcs			Spares readout possibility		128				1.5u amsw						
TA2_75	VA-type CSA with Wired-Or Trigger Output	Medium	Trigger Output		128			75ns	1.5u amsw						
CA2 CA2_2	VA-type Amplifier with Parallel Trigger Output	Medium	Parallel Trigger Outputs	72	128		500 + 50fpF	100ns	1.5u amsw						
Vatest					8x4			50ns	1.5u amsw						
SA3	Part of the VA-TA chip-set [3]; Use with VA32_75, VA32_500		Trigger Output; Serial Timing Output					75ns	1.5u amsw						
Tat2					32				0.6u amsw+						
Tat3					31(incl. 1 test chan.)			75ns	0.6u amsw+						
Ta645am					128			6µs	0.6u amsw+						
Tap64_jv	Use with VA064				64				0.6u amsw+						
Angie 31x32_2					31x32 (992+1test)			0.5µs	0.6u amsw+						
Angie 31x32_3					31x32 (992+1test)			0.5µs	0.6u amsw+						
Va_ta10x10			10x10 pixel chip		10x10 array			0.3µs	0.35u mixed						

[1] Tp: Nominal peaking time. DTp approximately ±50% of the nominal value.

[2] Voltage output. Value given in mV/fC.

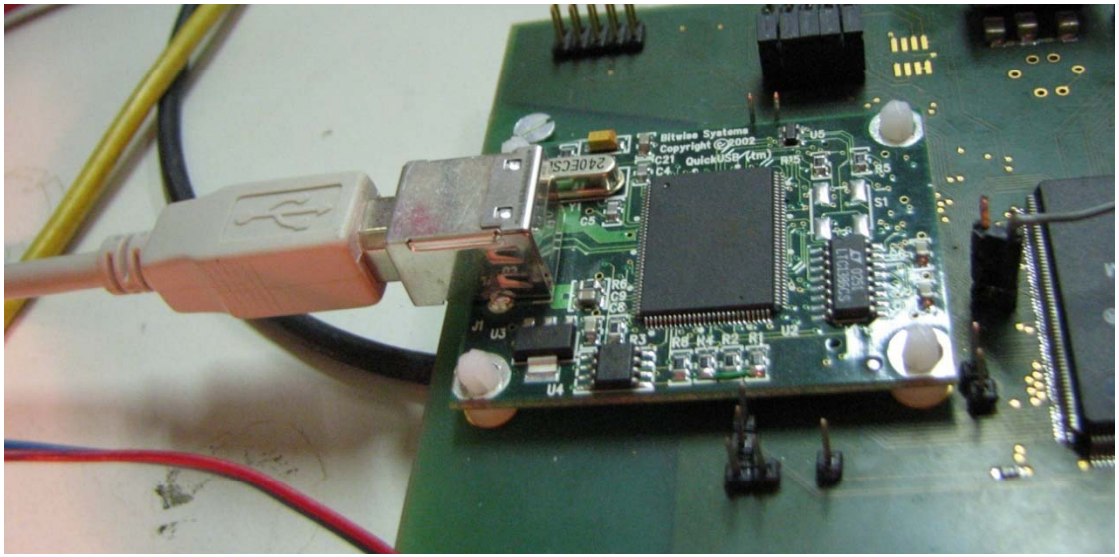
VATAGP_testDAQ



VATAGP_testDAQ :

- up to 16 GP chips , connected in daisy chain.
- readout in “serial” or “sparse” or “sparse with neighbors” modes.
- two 12 bits ADCs (for DOWN and UP analog outputs).

QuikUSB module.



www.quickusb.com :

- 150 USD,
- USB-2, up to 30 MB/sec .
- drivers and libraries for Windows (XP and Vista) and Linux.
- 16 bits HS data bus. + Three 8 bits ports
- downloading FPGA : Altera and Xilinx

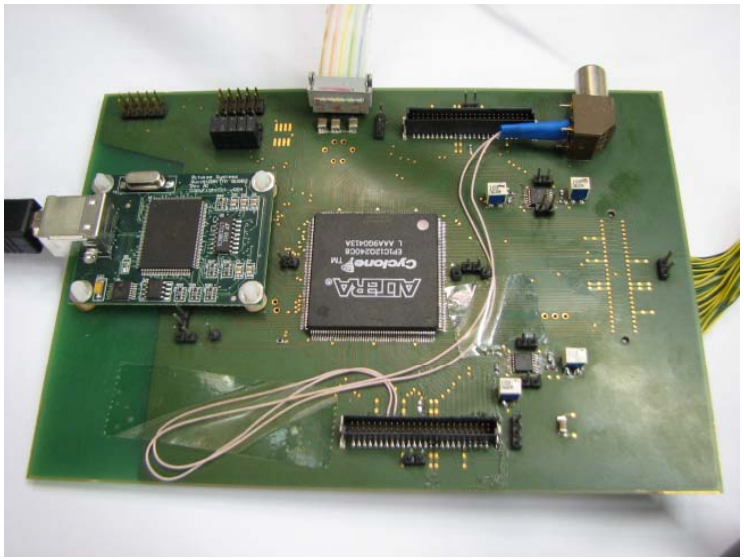
Readout Electronics for MPGDs

Developed for Readout of DPGP Front-end Electronics

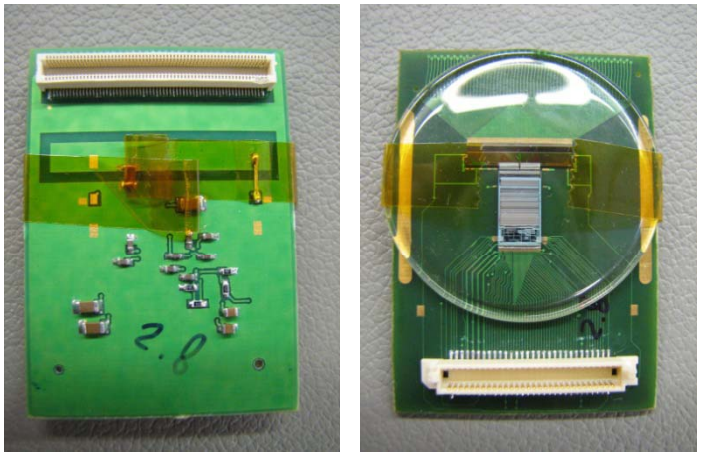
David Watts
Nail Malakhov

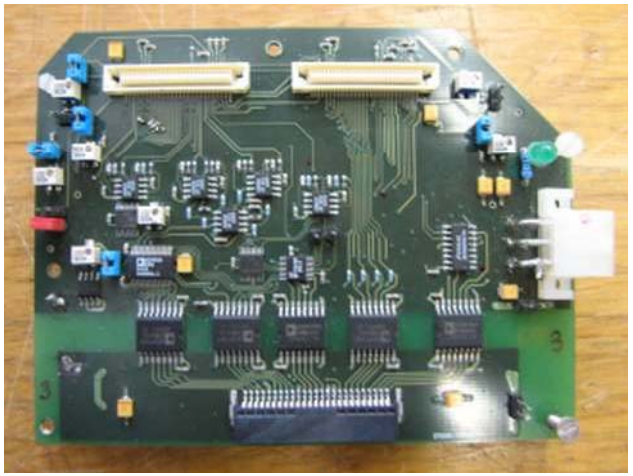
DPGP Electronics

3DAQ

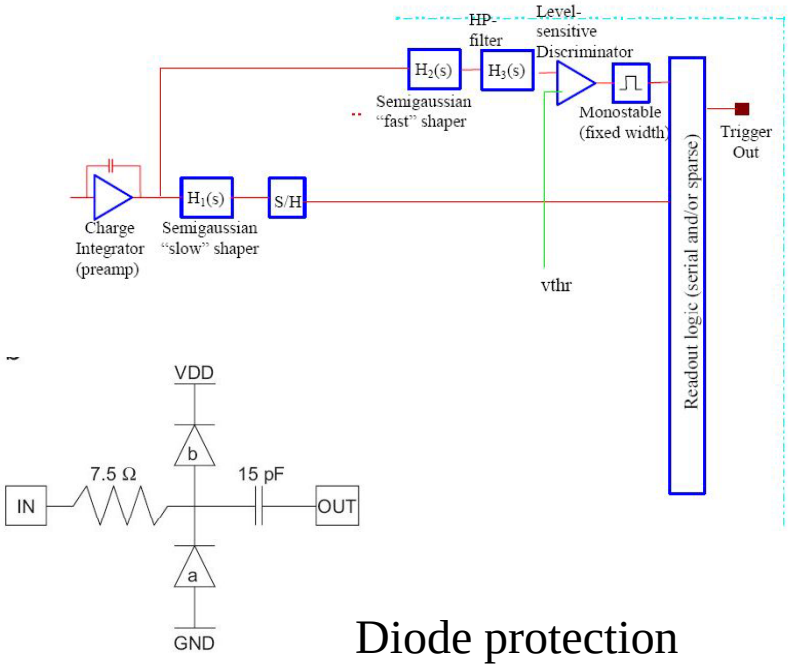


DPGP5 Hybrids





MDAQ

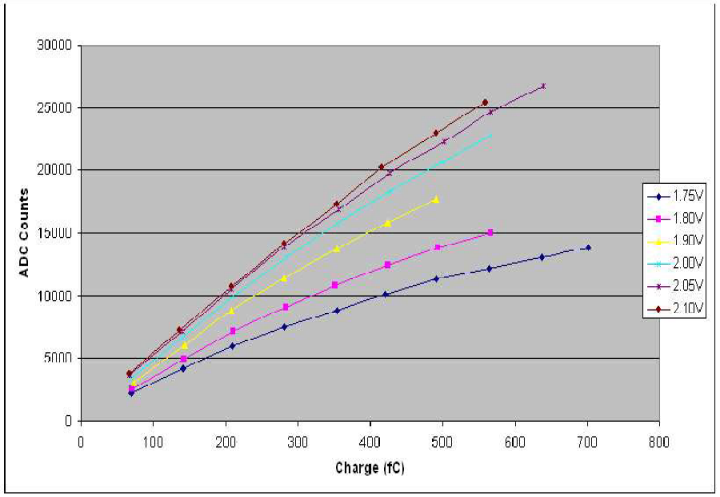


Diode protection

DPGP Electronics

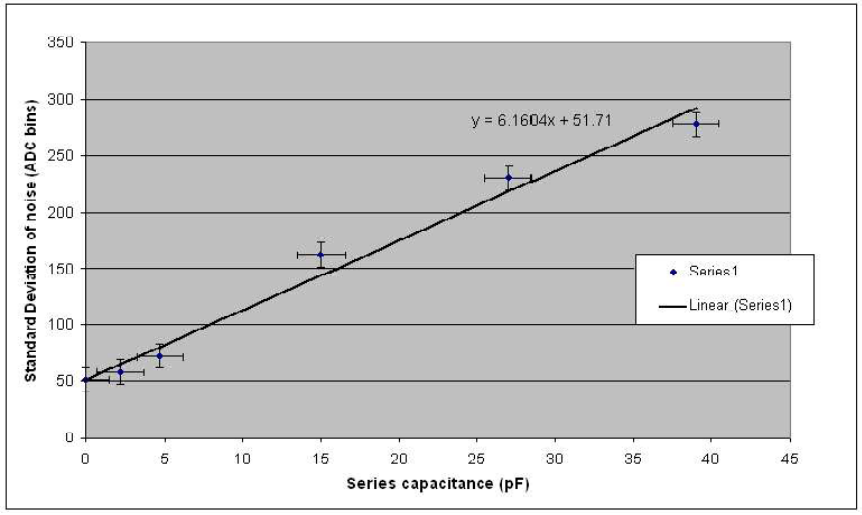
Electronics Characterization

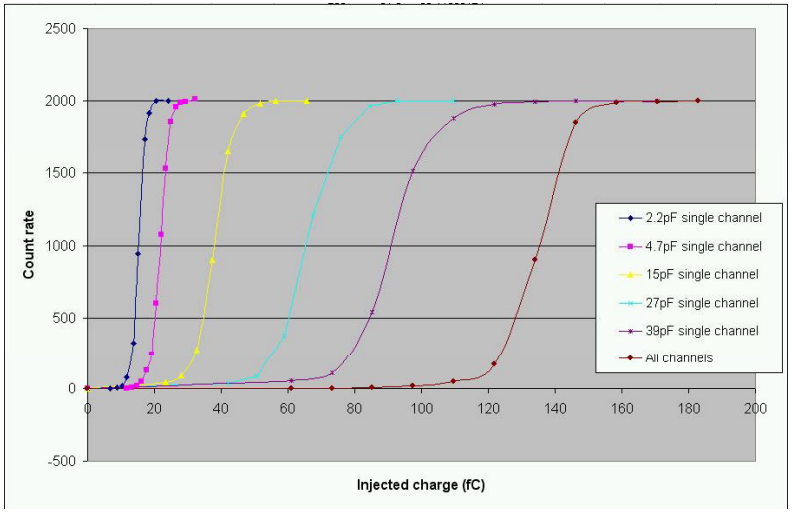
DPGP Hybrids + 3DAQ QuickUSB Readout



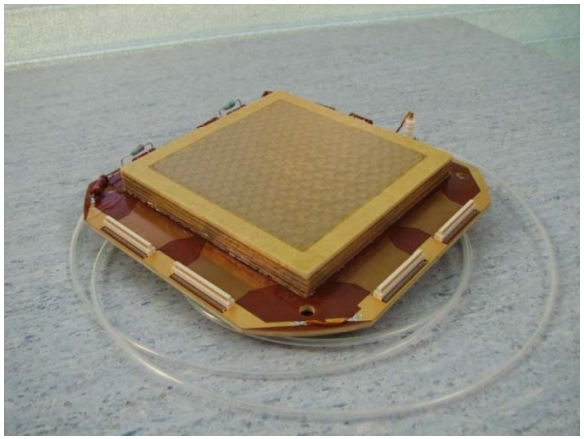
Dynamic range : up to 1pC
Lowest threshold:
- 140fC all channels trigger
- 15fC single channel trigger

Analogue Noise:
- 0.8fC + 0.25fC/pF or 5100e +1500e/pF

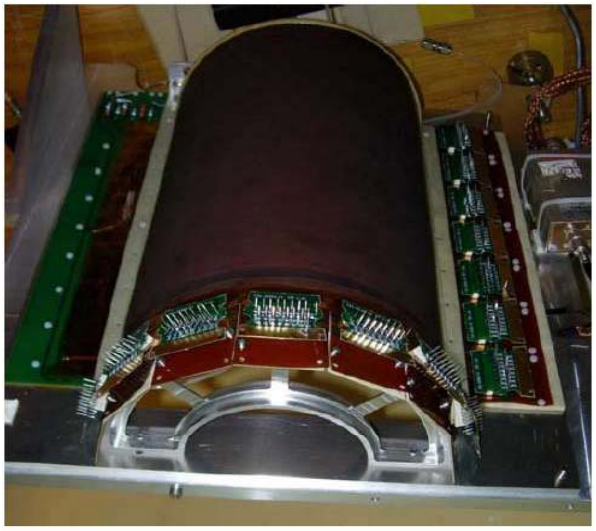




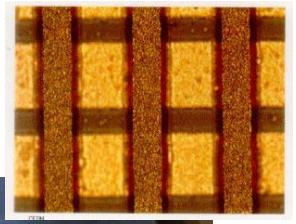
Compatible GEM Designs

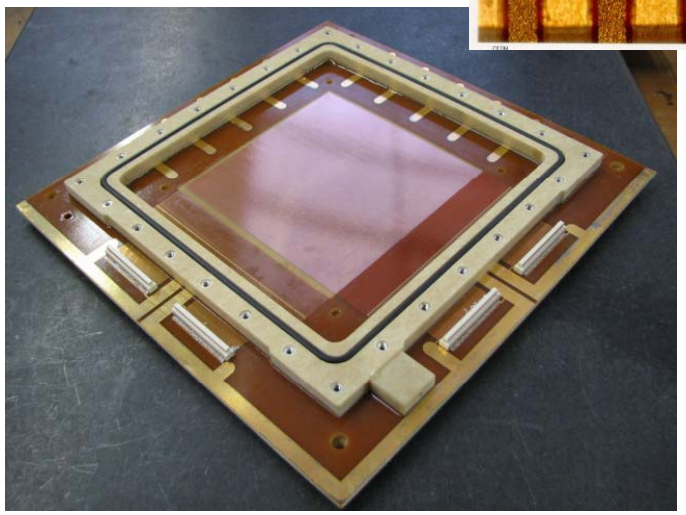


10x10-130-SEALED TGEM

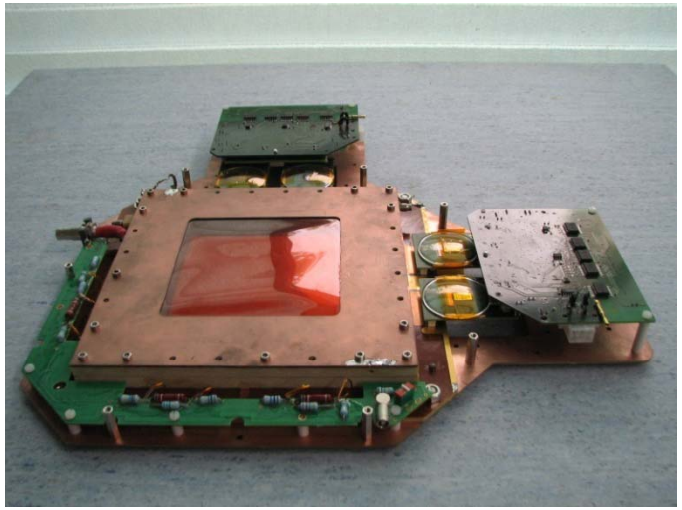


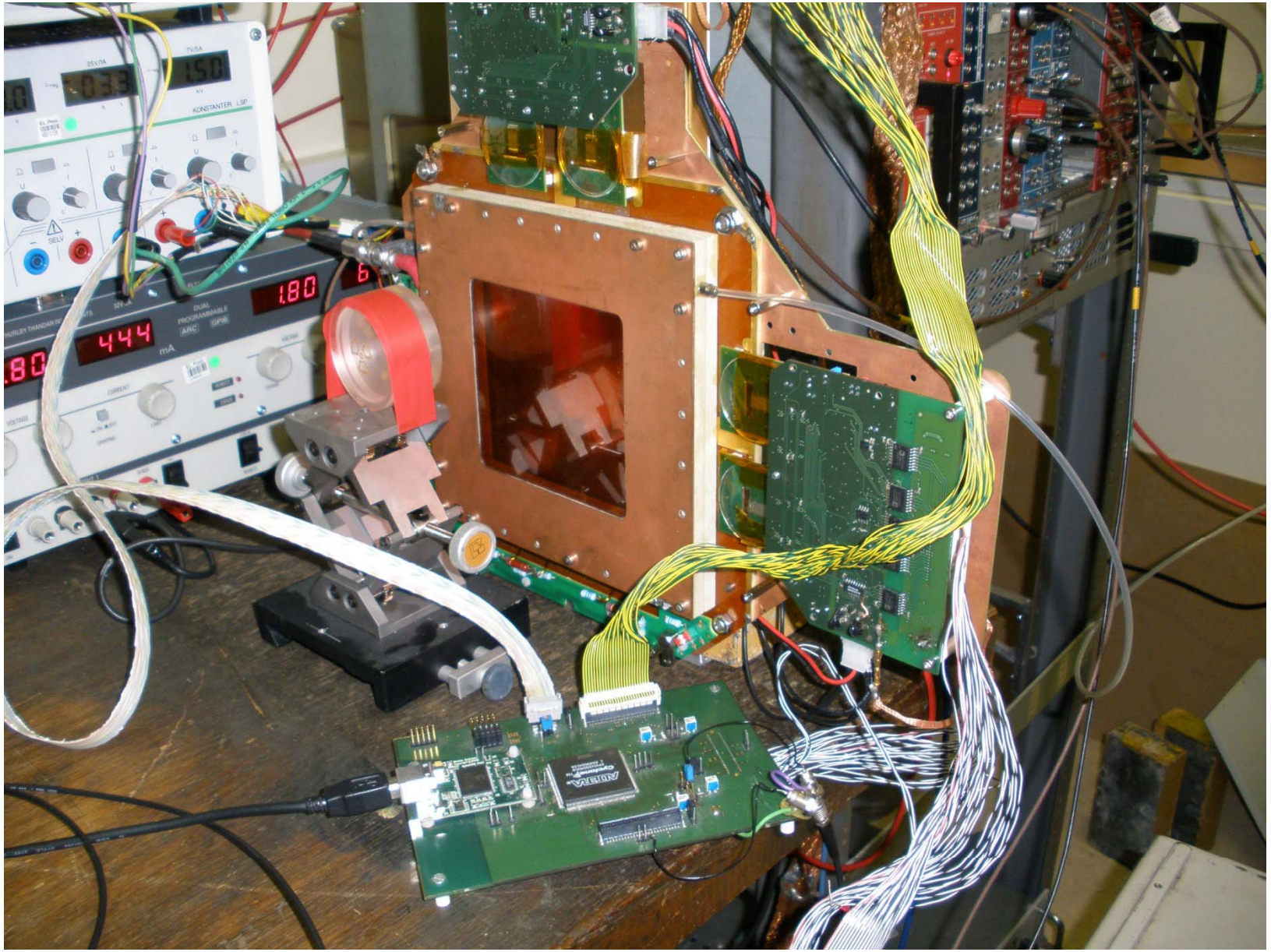
Cylindrical GEM





10x10-130 TGEM (unmountable)



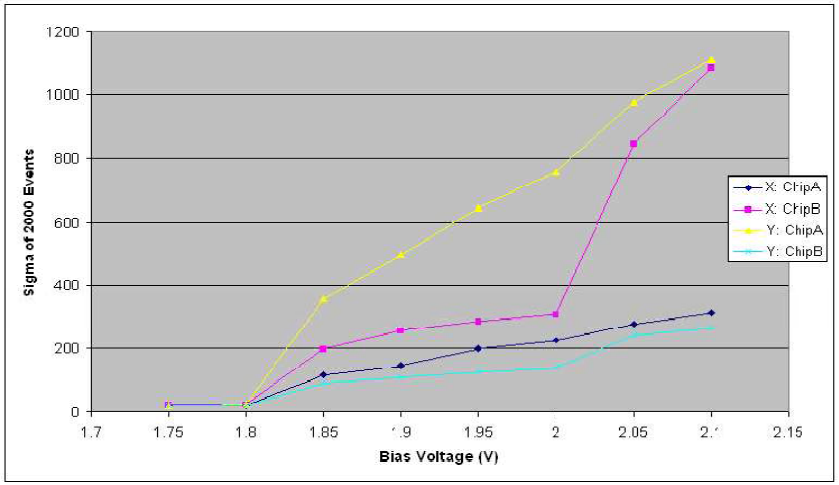

KONSTANTER LSP
DUAL
PROGRAMMABLE
ARC
GPIB
444
mA
1.80
ALTERA

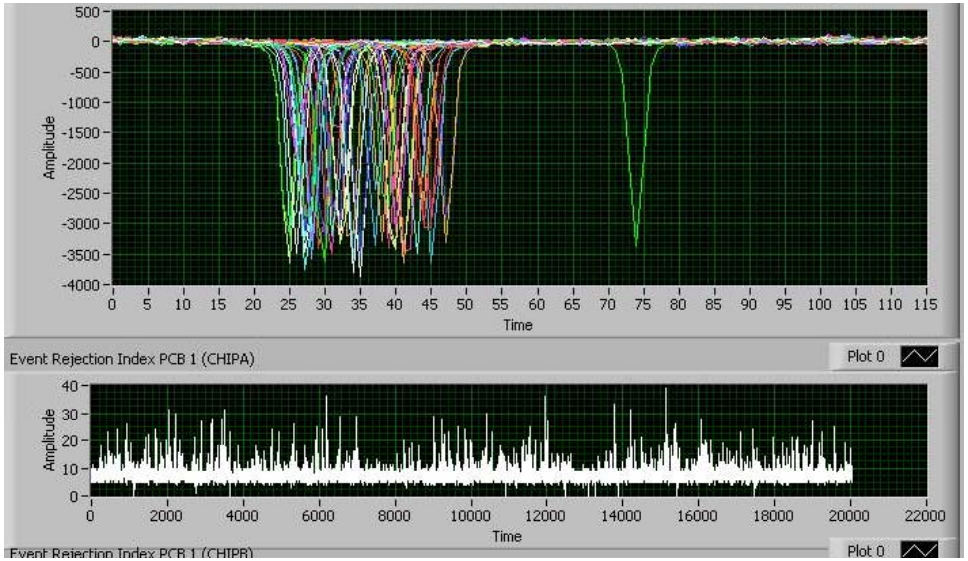
DPGP Readout with TGEM

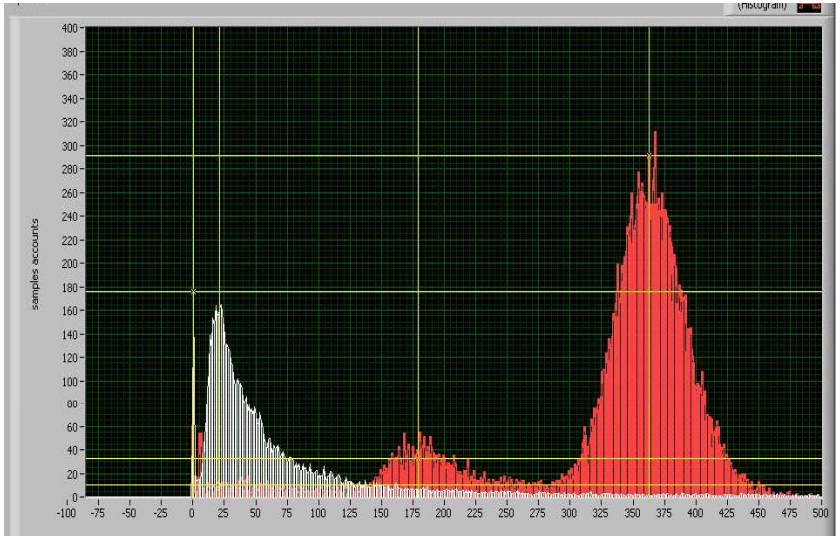
18% FWHM energy resolution at 5.9keV

Serial mode readout :	up to 50ksps
Sparse readout :	up to 1Msps
Sparse-w-neighbors:	up to 3Msps
Purely digital :	up to 8Msps

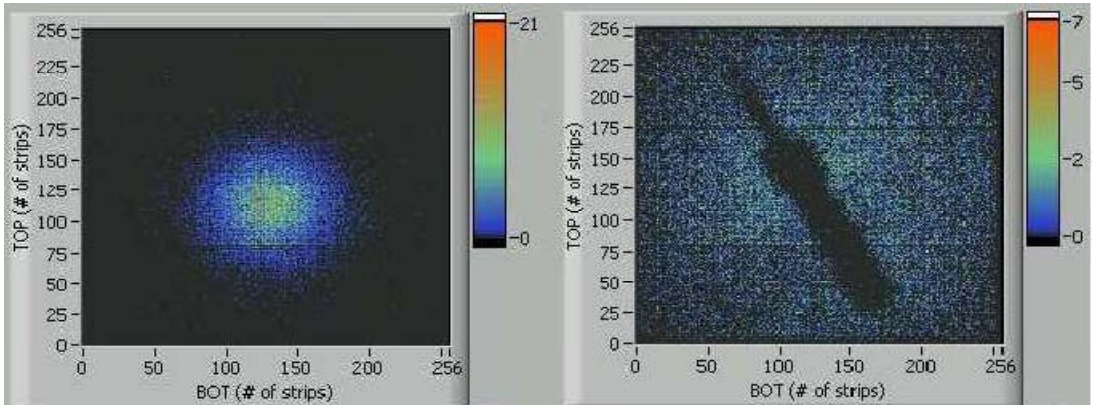
Labview software for analysis and acquisition





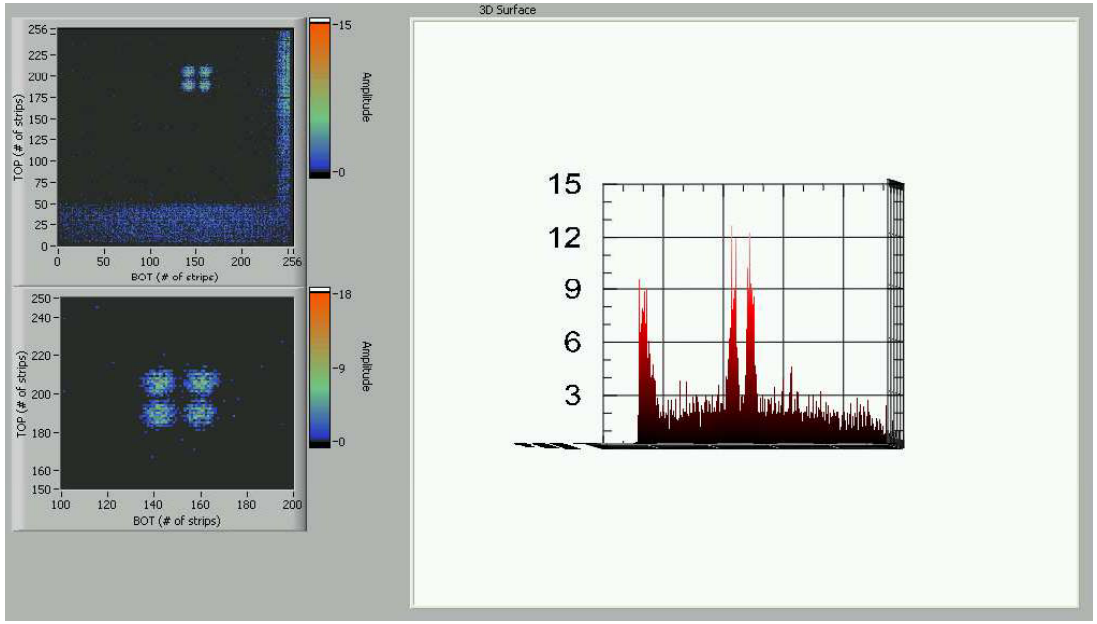


DPGP Readout with TGEM



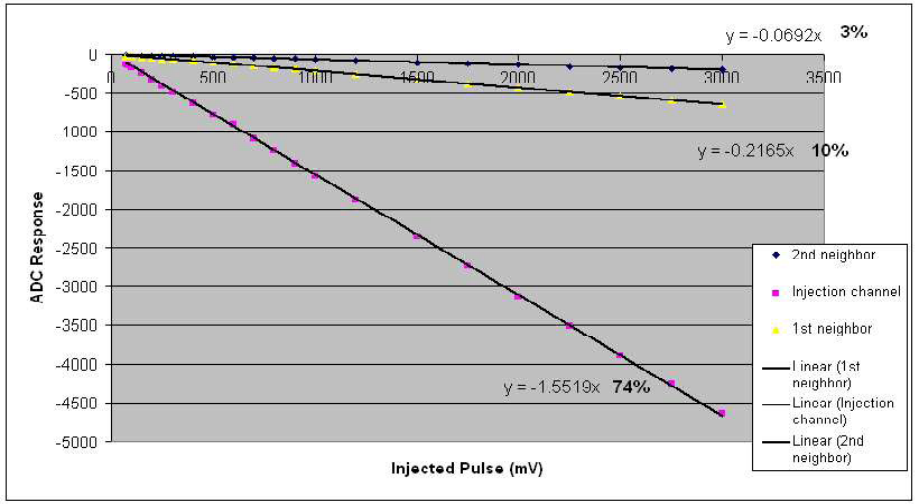
Fe55 source and a
Banana plug

Aluminum mask
with 2mm holes



DPGP Readout with TGEM

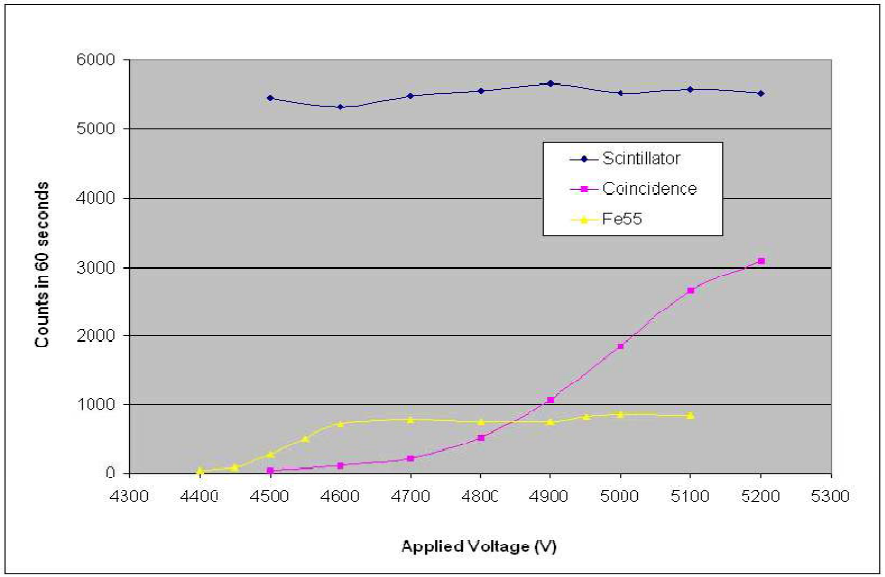
Crosstalk and MIP Efficiency



26% of charge “lost” in neighboring channels

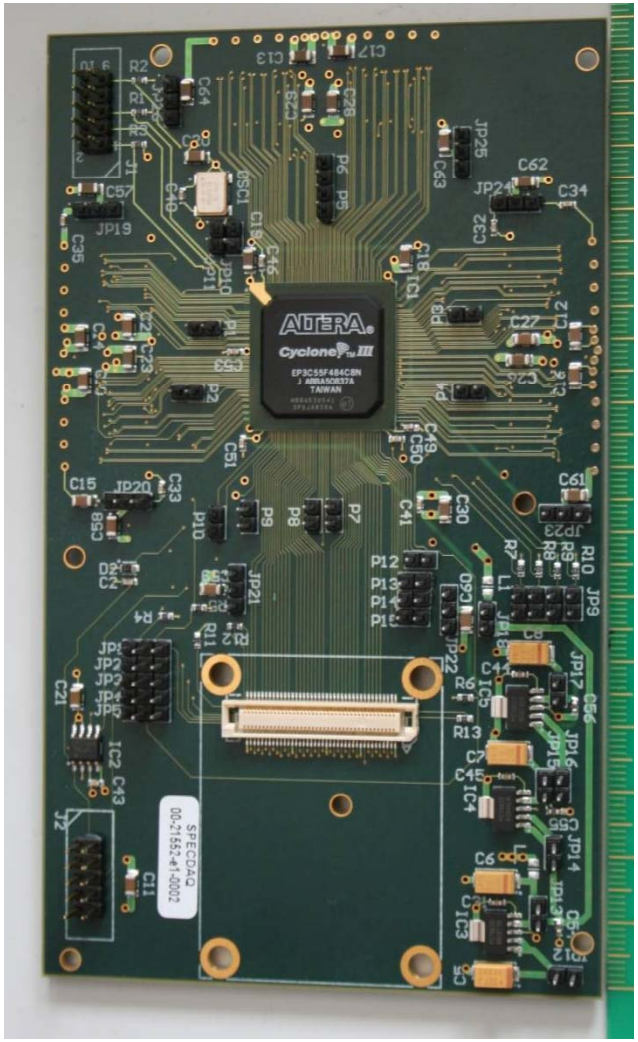
Efficient for 6keV but NOT for MIPs
→need trim-DAC threshold adjustment

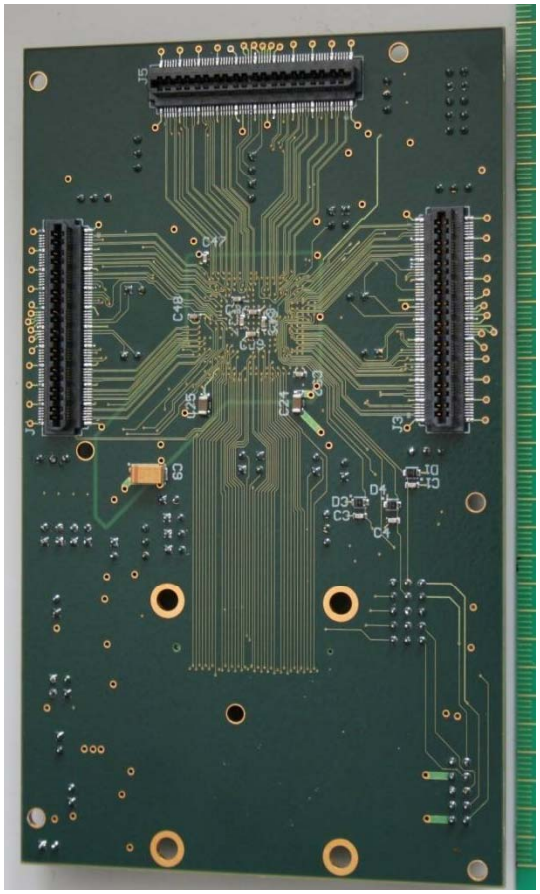
→Or to use coincidence with other axes and/or chambers (external triggers).



Main DAQ.

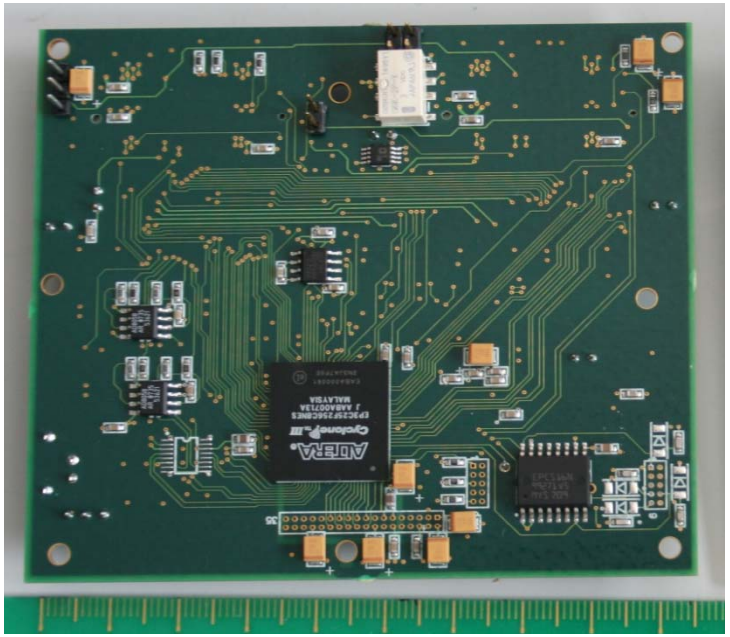
new version

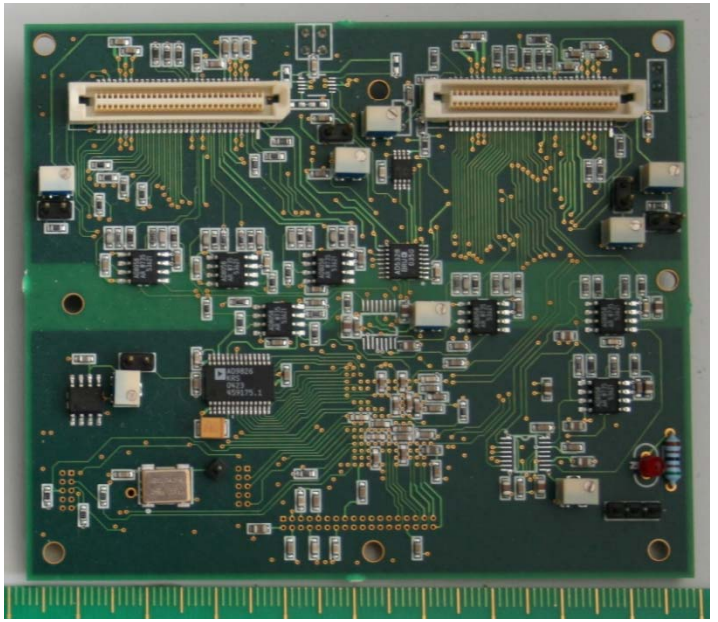




- *Altera Cyclone III.*
- *three 100 pins HF connectors .*
- *designed for LVDS connection*

new version of Readout Board for VATAGP...



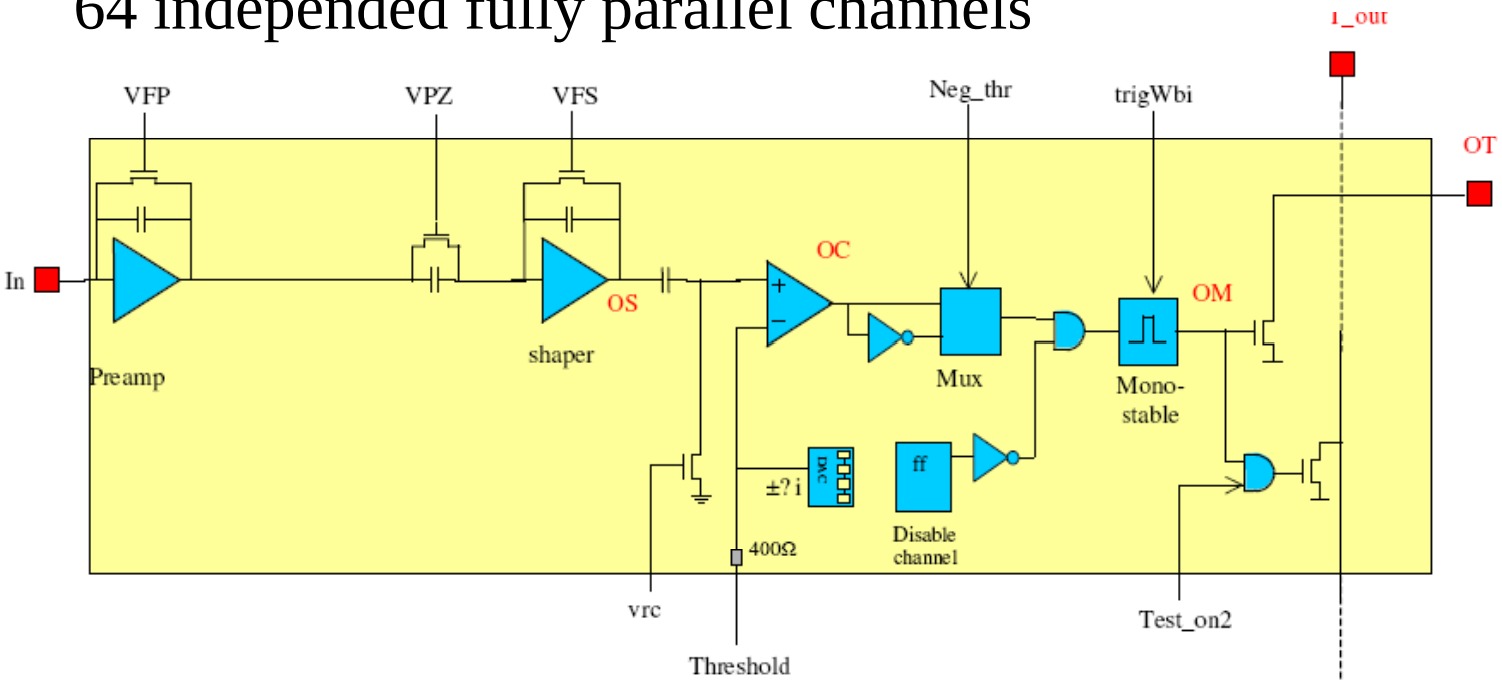


- with Altera Cyclone III for full parameters control and readout. And serial LVDS interface to central unit.

VA64TAP.... (few different types – different gain : for Si, PM...)

block diagram.

64 independed fully parallel channels



The parallel trigger output, *OT, is an open-drain* current that should be terminated with a low impedance in order to avoid pick-up in other channels.
It can be connected directly to the input of the **LS64 ASIC**.

VA64TAP2 test board.