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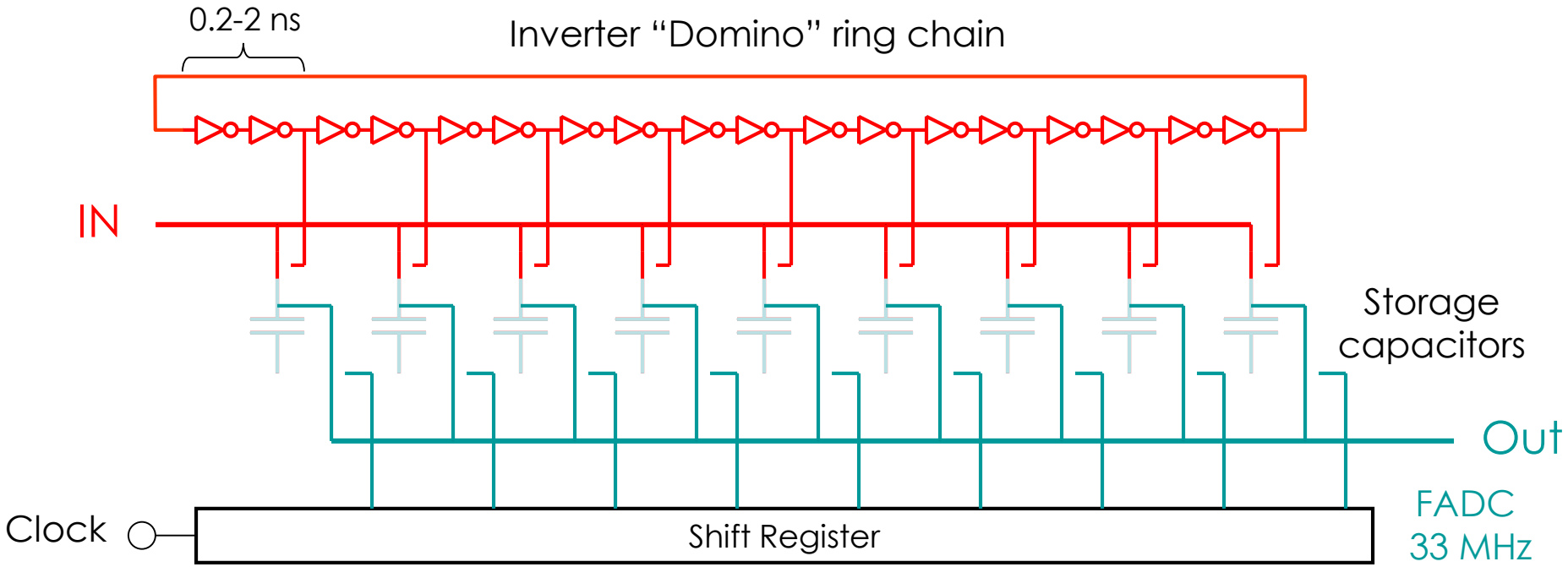
Stefan Ritt :: Muon Physics :: Paul Scherrer Institute

The WaveDAQ system: Picosecond measurements with 10'000 channels

Workshop on pico-second photon sensors, Kansas City, Sept. 2016

DRS4 Chip



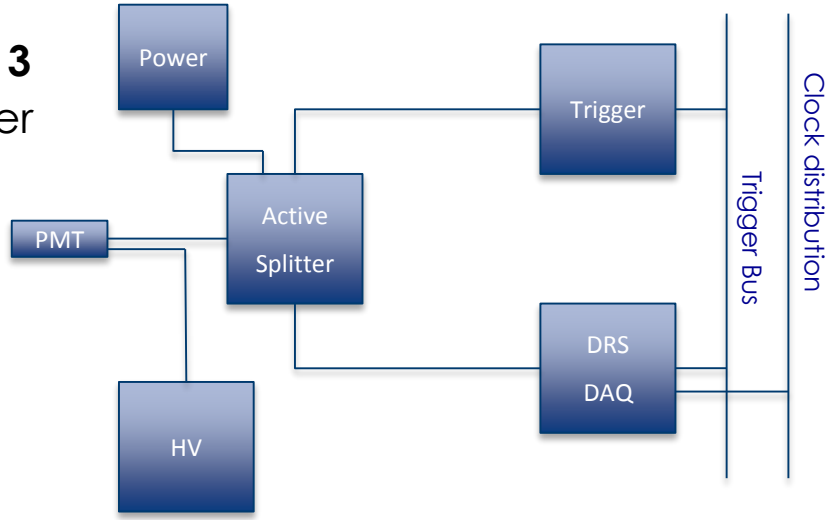
-Switched Capacitor Array (Analog Memory) developed at PSI
-5 GSPS / 11.5 bits SNR, 9 channels on 5 mm x 5 mm chip, 40 mW / chn.
-Used at ~200 locations worldwide
-2011, 2014 Clermont-Ferrand: "DRS4 Chip, Timing Calibration"

-Pile-up rejection	O(~10 ns)
-Time measurement	O(10 ps)
-Charge measurement	O(0.1%)

MEG & MEG II

MEG Experiment 1999-2013

- Separated DAQ & Trigger
- 3000 Channels DRS4 (0.8 GSPS / 1.6 GSPS)
- 1000 Channels Trigger (100 MSPS)
- 5 Racks



MEG II Experiment 2014-

- 9000 Channels
- Same rack space
  - Avoid dead space between boards
  - Combine DAQ & Trigger
  - Integrate high voltage
- Timing requirement
  - O(10 ps) between any two channels

?

Crate Options

Feature	VME	ATCA	???
Transfer speed O(100 MB/s)	✓	✓	✓
Dual-Star Topology with Gbit links	✗	✓	✓
Shelf management	✗	✓	✓
Fast trigger distribution	✗	✗	✓
Low-jitter precision clock O(ps)	✗	✗	✓
200 V SiPM biasing	✗	✗	✓
< 2000 US$per crate including power	✗	✗	✓

Custom Design

- Standard 19" crate + custom backplane
- Idea: Not only a solution for MEG II,

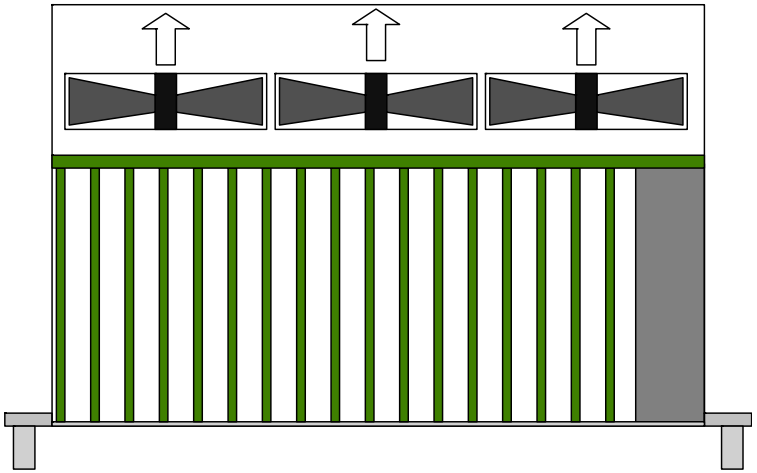
  but more general "crate standard"
- Take the best ideas on the market and combine them
  - Single 24 V backplane power
  - Serial gigabit links
  - Serial bus for configuration
  - Hot-swap functionality
  - Shelf management (but simpler!) with Ethernet interface
    - Power, Temperature, Fans control, board management

New Ideas

- Power supply on the side
- Cooling from back to front

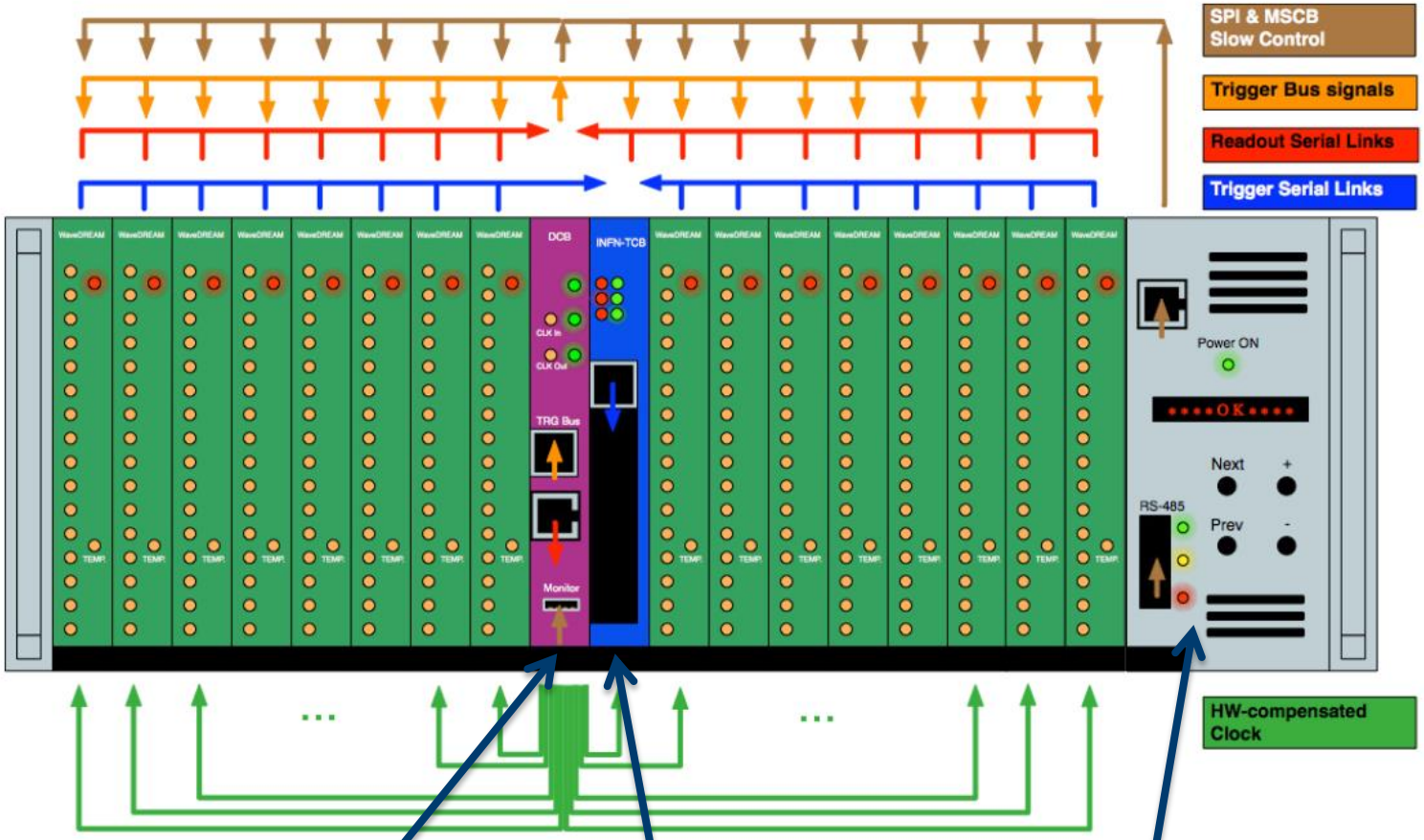
} no “dead” space on top and bottom

- Trigger / busy logic through backplane (→ next slide)
- Dual star topology for trigger & DAQ in parallel
- **Low skew clock (few ps) for high precision timing**
- Firmware download through backplane via shelf management
- High voltage power supply through backplane (200 V)



Traditional trigger & clock distribution

WaveDAQ System

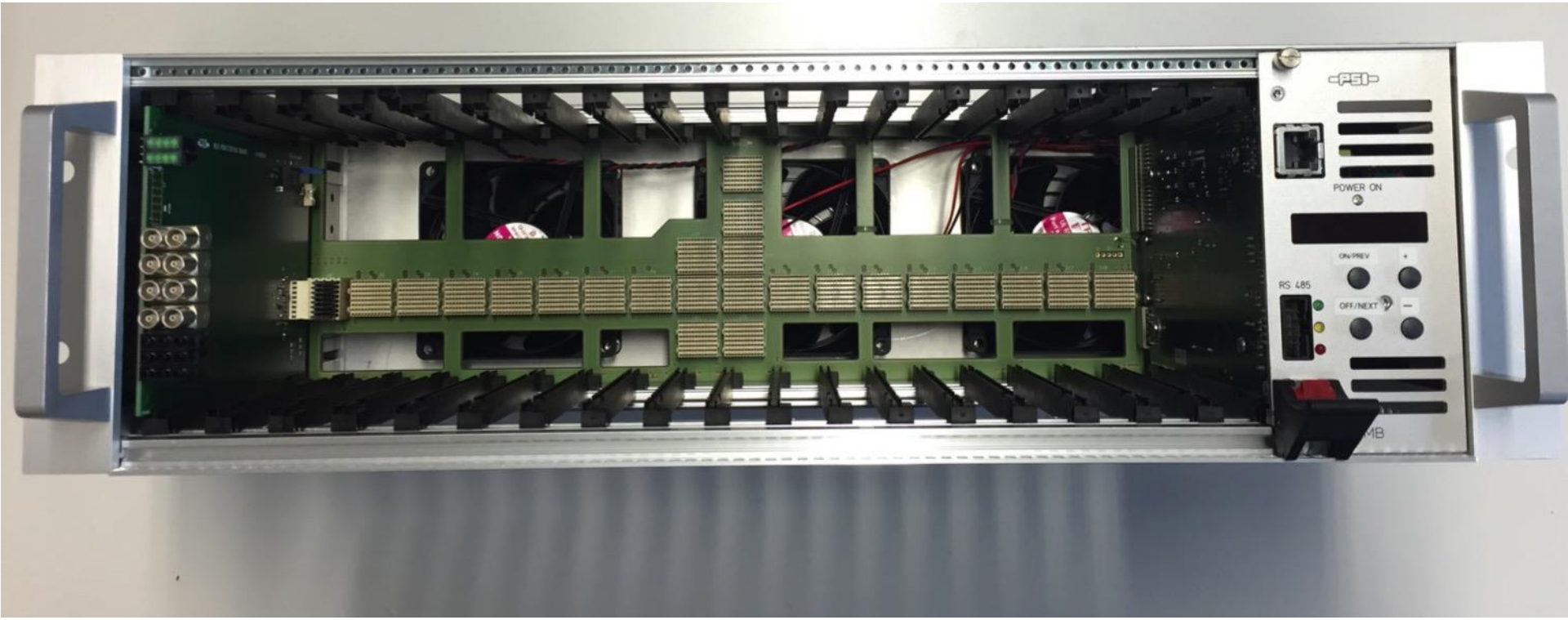


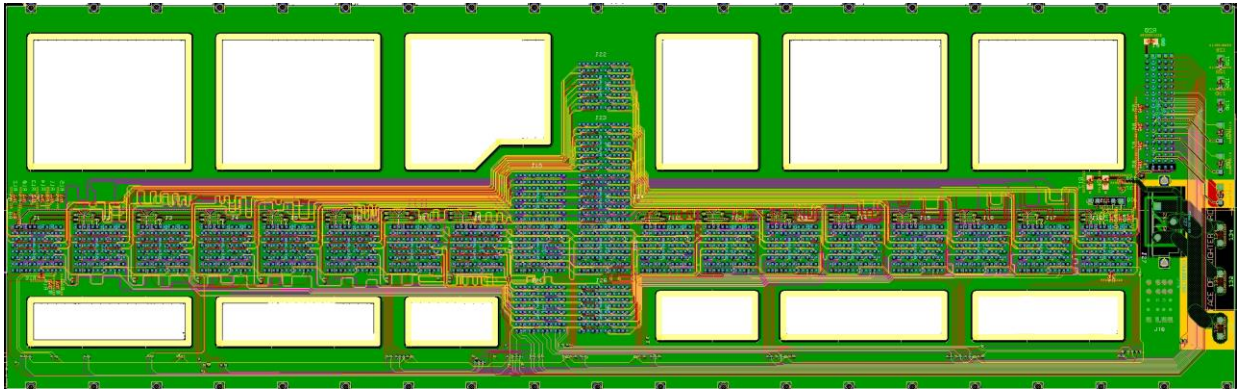
Data Concentrator Board (DCB)

Trigger Concentrator Board (TCB)

Crate **M**anagement **B**oard
- Power supply 24V / 300W
- Fan / Temp. control
- Power cycle each slot
- FPGA Firmware upload
- Local control via buttons
- Ethernet remote control

Half Height Backplane





Pin Assignment

Data Concentrator Board (DCB)

	A	B	C	D	E	F	G	H	I	J	K	L	
C2													
8	GND	LSK0_CLK_P	LSK0_CLK_N	GND	SD0_D1_P	SD0_D1_N	GND	SD15_D1_P	SD15_D1_N	GND	LSK15_CLK_P	LSK15_CLK_N	LSK_CLK 0/15
7	LSK1_CLK_P	LSK1_CLK_N	GND	SD1_D1_P	SD1_D1_N	GND	SD14_D1_P	SD14_D1_N	GND	LSK14_CLK_P	LSK14_CLK_N	GND	LSK_CLK 1/14
6	GND	LSK2_CLK_P	LSK2_CLK_N	GND	SD2_D1_P	SD2_D1_N	GND	SD13_D1_P	SD13_D1_N	GND	LSK13_CLK_P	LSK13_CLK_N	LSK_CLK 2/13
5	LSK3_CLK_P	LSK3_CLK_N	GND	SD3_D1_P	SD3_D1_N	GND	SD12_D1_P	SD12_D1_N	GND	LSK12_CLK_P	LSK12_CLK_N	GND	LSK_CLK 3/12
4	GND	LSK4_CLK_P	LSK4_CLK_N	GND	SD4_D1_P	SD4_D1_N	GND	SD11_D1_P	SD11_D1_N	GND	LSK11_CLK_P	LSK11_CLK_N	LSK_CLK 4/11
3	LSK5_CLK_P	LSK5_CLK_N	GND	SD5_D1_P	SD5_D1_N	GND	SD10_D1_P	SD10_D1_N	GND	LSK10_CLK_P	LSK10_CLK_N	GND	LSK_CLK 5/10
2	GND	LSK6_CLK_P	LSK6_CLK_N	GND	SD6_D1_P	SD6_D1_N	GND	SD9_D1_P	SD9_D1_N	GND	LSK9_CLK_P	LSK9_CLK_N	LSK_CLK 6/9
1	LSK7_CLK_P	LSK7_CLK_N	GND	SD7_D1_P	SD7_D1_N	GND	SD8_D1_P	SD8_D1_N	GND	LSK8_CLK_P	LSK8_CLK_N	GND	LSK_CLK 7/8
C3	A	B	C	D	E	F	G	H	I	J	K	L	
8	24V	don't connect	don't connect	24V	don't connect	don't connect	3.3V	don't connect	don't connect	3.3V	don't connect	don't connect	POWER
7	TRIGGER_P	TRIGGER_N	GND			GND	TR_BUSY_P	TR_BUSY_N	GND	TR_SYNC_P	TR_SYNC_N	GND	TRIGGER
6	GND	SPI_CLK_P	SPI_CLK_N	GND	SPI_MOSI_P	SPI_MOSI_N	GND	SPI_MISO_P	SPI_MISO_N	GND	MSCB_P	MSCB_N	SPI/MSCB
5	SD6_D0_P	SD6_D0_N	GND	SD6_CLK_P	SD6_CLK_N	GND	SD9_D0_P	SD9_D0_N	GND	SD9_CLK_P	SD9_CLK_N	GND	SERDES WD6/9
4	GND	SD7_D0_P	SD7_D0_N	GND	SD7_CLK_P	SD7_CLK_N	GND	SD8_D0_P	SD8_D0_N	GND	SD8_CLK_P	SD8_CLK_N	SERDES WD7/8
3	SELECT_TCB		GND	LSK_TCB_CLK_P	LSK_TCB_CLK_N	GND			GND			GND	SELECT/LSK TCB
2	24V	SD_RX_D_P	SD_RX_D_N	24V	SD_RX_CLK_P	SD_RX_CLK_N	24V	SD_TX_D_P	SD_TX_D_N	24V	SD_TX_CLK_P	SD_TX_CLK_N	SEDES TCB
1	POWER_ON	/INIT	GND/SENSE	/BOARD_SELECT	/FLASH_SELECT	CLK_P	CLK_N	CLK_P	CLK_N	GND	/SYNC	/ATTENTION	GND	CONTROL
C4	A	B	C	D	E	F	G	H	I	J	K	L	
8	GND	SD5_D0_P	SD5_D0_N	GND	SD5_CLK_P	SD5_CLK_N	GND	SD10_D0_P	SD10_D0_N	GND	SD10_CLK_P	SD10_CLK_N	SERDES WD5/10
7	SD4_D0_P	SD4_D0_N	GND	SD4_CLK_P	SD4_CLK_N	GND	SD11_D0_P	SD11_D0_N	GND	SD11_CLK_P	SD11_CLK_N	GND	SERDES WD4/11
6	GND	SD3_D0_P	SD3_D0_N	GND	SD3_CLK_P	SD3_CLK_N	GND	SD12_D0_P	SD12_D0_N	GND	SD12_CLK_P	SD12_CLK_N	SERDES WD3/12
5	SD2_D0_P	SD2_D0_N	GND	SD2_CLK_P	SD2_CLK_N	GND	SD13_D0_P	SD13_D0_N	GND	SD13_CLK_P	SD13_CLK_N	GND	SERDES WD2/13
4	GND	SD1_D0_P	SD1_D0_N	GND	SD1_CLK_P	SD1_CLK_N	GND	SD14_D0_P	SD14_D0_N	GND	SD14_CLK_P	SD14_CLK_N	SERDES WD1/14
3	SD0_D0_P	SD0_D0_N	GND	SD0_CLK_P	SD0_CLK_N	GND	SD15_D0_P	SD15_D0_N	GND	SD15_CLK_P	SD15_CLK_N	GND	SERDES WD0/15
2	GND	/SELECT 1	GND	/SELECT 2	/SELECT 3	GND	/SELECT 12	/SELECT 13	GND	/SELECT 14	/SELECT 15	GND	SELECT
1	/SELECT 4	/SELECT 5	GND	/SELECT 6	/SELECT 7	GND	/SELECT 8	/SELECT 9	GND	/SELECT 10	/SELECT 11	GND	SELECT

	A	B	C	D	E	F	G	H	I	J	K	L	
C3													
8	24V	HV0	HV1	24V	HV2	HV3	3.3V	spare	spare	3V	spare	spare	POWER
7	TRIGGER_P	TRIGGER_N	GND	LSK_CLK_P	LSK_CLK_N	GND	TR_BUSY_P	TR_BUSY_N	GND	TR_SYNC_P	TR_SYNC_N	GND	TRIGGER/CLK
6	GND	SPI_CLK_P	SPI_CLK_N	GND	SPI_MOSI_P	SPI_MOSI_N	GND	SPI_MISO_P	SPI_MISO_N	GND	MSCB_P	MSCB_N	SPI/MSCB
5	SDx_D4_P	SDx_D4_N	GND	SDx_DS_P	SDx_DS_N	GND	SDx_D6_P	SDx_D6_N	GND	SDx_CLK_P	SDx_CLK_N	GND	to TCB
4	GND	SDx_D0_P	SDx_D0_N	GND	SDx_D1_P	SDx_D1_N	GND	SDx_D2_P	SDx_D2_N	GND	SDx_D3_P	SDx_D3_N	to TCB
3	SDx_D6_P	SDx_D4_N	GND	SDx_DS_P	SDx_DS_N	GND	SDx_D6_P	SDx_D6_N	GND	SDx_CLK_P	SDx_CLK_N	GND	to DCB
2	24V	SDx_D0_P	SDx_D0_N	24V	SDx_D1_P	SDx_D1_N	GND	SDx_D2_P	SDx_D2_N	24V	SDx_D3_P	SDx_D3_N	to DCB
1	POWER_ON	/INIT	GND/SENSE	/BOARD_SELECT	/FLASH_SELECT	CLK_P	CLK_N	CLK_P	CLK_N	GND	/SYNC	/ATTENTION	GND	CONTROL

GND
POWER
LVDS
LVDS unconnected at backplane
LVTTL
SERDES
SERDES_2-7 not connected at backplane, possible use in future extensions

Trigger Concentrator Board (TCB)

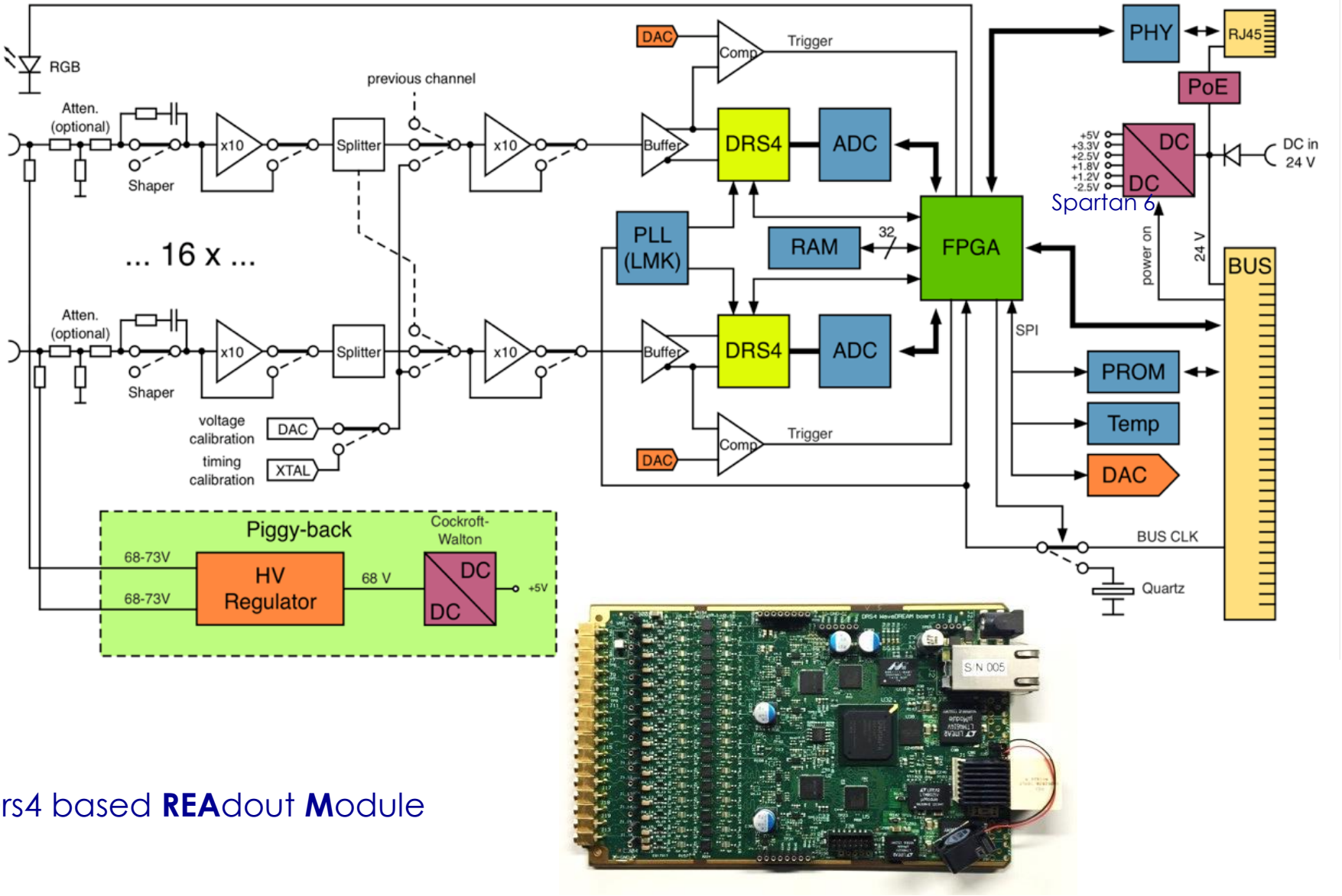
8 SERDES connections to each WaveDREAM board

	A	B	C	D	E	F	G	H	I	J	K	L	
C0													
8	GND	SD0_DS_P	SD0_DS_N	GND	SD0_D6_P	SD0_D6_N	GND	SD15_DS_P	SD15_DS_N	GND	SD15_D6_P	SD15_D6_N	SERDES WD0/15
7	SD0_CLK_P	SD0_CLK_N	GND	SD0_D4_P	SD0_D4_N	GND	SD15_CLK_P	SD15_CLK_N	GND	SD15_D4_P	SD15_D4_N	GND	SERDES WD0/15
6	GND	SD0_D1_P	SD0_D1_N	GND	SD0_D2_P	SD0_D2_N	GND	SD15_D1_P	SD15_D1_N	GND	SD15_D2_P	SD15_D2_N	SERDES WD0/15
5	SD0_D3_P	SD0_D3_N	GND	SD0_D0_P	SD0_D0_N	GND	SD15_D3_P	SD15_D3_N	GND	SD15_D0_P	SD15_D0_N	GND	SERDES WD0/15
4	GND	SD1_D5_P	SD1_DS_N	GND	SD1_D6_P	SD1_D6_N	GND	SD14_DS_P	SD14_DS_N	GND	SD14_D6_P	SD14_D6_N	SERDES WD1/14
3	SD1_CLK_P	SD1_CLK_N	GND	SD1_D4_P	SD1_D4_N	GND	SD14_CLK_P	SD14_CLK_N	GND	SD14_D4_P	SD14_D4_N	GND	SERDES WD1/14
2	GND	SD1_D5_P	SD1_D3_N	GND	SD1_D2_P	SD1_D2_N	GND	SD14_D1_P	SD14_D1_N	GND	SD14_D2_P	SD14_D2_P	SERDES WD1/14
1	SD1_D3_P	SD1_D3_N	GND	SD1_D0_P	SD1_D0_N	GND	SD14_D3_P	SD14_D3_N	GND	SD14_D0_P	SD14_D0_N	GND	SERDES WD1/14
C1	A	B	C	D	E	F	G	H	I	J	K	L	
8	GND	SD2_DS_P	SD2_DS_N	GND	SD2_D6_P	SD2_D6_N	GND	SD13_DS_P	SD13_DS_N	GND	SD13_D6_P	SD13_D6_N	SERDES WD2/13
7	SD2_CLK_P	SD2_CLK_N	GND	SD2_D4_P	SD2_D4_N	GND	SD13_CLK_P	SD13_CLK_N	GND	SD13_D4_P	SD13_D4_N	GND	SERDES WD2/13
6	GND	SD2_D1_P	SD2_D1_N	GND	SD2_D2_P	SD2_D2_N	GND	SD13_D1_P	SD13_D1_N	GND	SD13_D2_P	SD13_D2_N	SERDES WD2/13
5	SD2_D3_P	SD2_D3_N	GND	SD2_D0_P	SD2_D0_N	GND	SD13_D3_P	SD13_D3_N	GND	SD13_D0_P	SD13_D0_N	GND	SERDES WD2/13
4	GND	SD3_DS_P	SD3_DS_N	GND	SD3_D6_P	SD3_D6_N	GND	SD12_DS_P	SD12_DS_N	GND	SD12_D6_P	SD12_D6_N	SERDES WD3/12
3	SD3_CLK_P	SD3_CLK_N	GND	SD3_D4_P	SD3_D4_N	GND	SD12_CLK_P	SD12_CLK_N	GND	SD12_D4_P	SD12_D4_N	GND	SERDES WD3/12
2	GND	SD3_D1_P	SD3_D1_N	GND	SD3_D2_P	SD3_D2_N	GND	SD12_D1_P	SD12_D1_N	GND	SD12_D2_P	SD12_D2_N	SERDES WD3/12
1	SD3_D3_P	SD3_D3_N	GND	SD3_D0_P	SD3_D0_N	GND	SD12_D3_P	SD12_D3_N	GND	SD12_D0_P	SD12_D0_N	GND	SERDES WD3/12
C2	A	B	C	D	E	F	G	H	I	J	K	L	
8	GND	SD4_DS_P	SD4_DS_N	GND	SD4_D6_P	SD4_D6_N	GND	SD11_DS_P	SD11_DS_N	GND	SD11_D6_P	SD11_D6_N	SERDES WD4/11
7	SD4_CLK_P	SD4_CLK_N	GND	SD4_D4_P	SD4_D4_N	GND	SD11_CLK_P	SD11_CLK_N	GND	SD11_D4_P	SD11_D4_N	GND	SERDES WD4/11
6	GND	SD4_D1_P	SD4_D1_N	GND	SD4_D2_P	SD4_D2_N	GND	SD11_D1_P	SD11_D1_N	GND	SD11_D2_P	SD11_D2_N	SERDES WD4/11
5	SD4_D3_P	SD4_D3_N	GND	SD4_D0_P	SD4_D0_N	GND	SD11_D3_P	SD11_D3_N	GND	SD11_D0_P	SD11_D0_N	GND	SERDES WD4/11
4	GND	SD5_DS_P	SD5_DS_N	GND	SD5_D6_P	SD5_D6_N	GND	SD10_DS_P	SD10_DS_N	GND	SD10_D6_P	SD10_D6_N	SERDES WD5/10
3	SD5_CLK_P	SD5_CLK_N	GND	SD5_D4_P	SD5_D4_N	GND	SD10_CLK_P	SD10_CLK_N	GND	SD10_D4_P	SD10_D4_N	GND	SERDES WD5/10
2	GND	SD5_D1_P	SD5_D1_N	GND	SD5_D2_P	SD5_D2_N	GND	SD10_D1_P	SD10_D1_N	GND	SD10_D2_P	SD10_D2_N	SERDES WD5/10
1	SD5_D3_P	SD5_D3_N	GND	SD5_D0_P	SD5_D0_N	GND	SD10_D3_P	SD10_D3_N	GND	SD10_D0_P	SD10_D0_N	GND	SERDES WD5/10
C3	A	B	C	D	E	F	G	H	I	J	K	L	
8	24V	don't connect	don't connect	24V	don't connect	don't connect	3.3V	don't connect	don't connect	3.3V	don't connect	don't connect	POWER
7	TRIGGER_P	TRIGGER_N	GND	LSK_TCB_CLK_P	LSK_TCB_CLK_N	GND	TR_BUSY_P	TR_BUSY_N	GND	TR_SYNC_P	TR_SYNC_N	GND	TRIGGER/CLK
6	GND	SPI_CLK_P	SPI_CLK_N	GND	SPI_MOSI_P	SPI_MOSI_N	GND	SPI_MISO_P	SPI_MISO_N	GND	MSCB_P	MSCB_N	SPI/MSCB
5			GND			GND			GND			GND	
4	GND			GND			GND			GND			
3			GND			GND			GND			GND	
2	24V	SD_TX_D_P	SD_TX_D_N	24V	SD_TX_CLK_P	SD_TX_CLK_N	24V	SD_RX_D_P	SD_RX_D_N	24V	SD_RX_CLK_P	SD_RX_CLK_N	SERDES DCB
1	POWER_ON	/INIT	GND/SENSE	/BOARD_SELECT	/FLASH_SELECT	CLK_P	CLK_N	CLK_P	CLK_N	GND	/SYNC	/ATTENTION	GND	CONTROL
C4	A	B	C	D	E	F	G	H	I	J	K	L	
8	GND	SD7_DS_P	SD7_DS_N	GND	SD7_D6_P	SD7_D6_N	GND	SD8_DS_P	SD8_DS_N	GND	SD8_D6_P	SD8_D6_N	SERDES WD7/8
7	SD7_CLK_P	SD7_CLK_N	GND	SD7_D4_P	SD7_D4_N	GND	SD8_CLK_P	SD8_CLK_N	GND	SD8_D4_P	SD8_D4_N	GND	SERDES WD7/8
6	GND	SD7_D1_P	SD7_D1_N	GND	SD7_D2_P	SD7_D2_N	GND	SD8_D1_P	SD8_D1_N	GND	SD8_D2_P	SD8_D2_N	SERDES WD7/8
5	SD7_D3_P	SD7_D3_N	GND	SD7_D0_P	SD7_D0_N	GND	SD8_D3_P	SD8_D3_N	GND	SD8_D0_P	SD8_D0_N	GND	SERDES WD7/8
4	GND	SD6_DS_P	SD6_DS_N	GND	SD6_D6_P	SD6_D6_N	GND	SD9_DS_P	SD9_DS_N	GND	SD9_D6_P	SD9_D6_N	SERDES WD6/9
3	SD6_CLK_P	SD6_CLK_N	GND	SD6_D4_P	SD6_D4_N	GND	SD9_CLK_P	SD9_CLK_N	GND	SD9_D4_P	SD9_D4_N	GND	SERDES WD6/9
2	GND	SD6_D1_P	SD6_D1_N	GND	SD6_D2_P	SD6_D2_N	GND	SD9_D1_P	SD9_D1_N	GND	SD9_D2_P	SD9_D2_N	SERDES WD6/9
1	SD6_D3_P	SD6_D3_N	GND	SD6_D0_P	SD6_D0_N	GND	SD9_D3_P	SD9_D3_N	GND	SD9_D0_P	SD9_D0_N	GND	SERDES WD6/9

Crate Management Board (CMB)

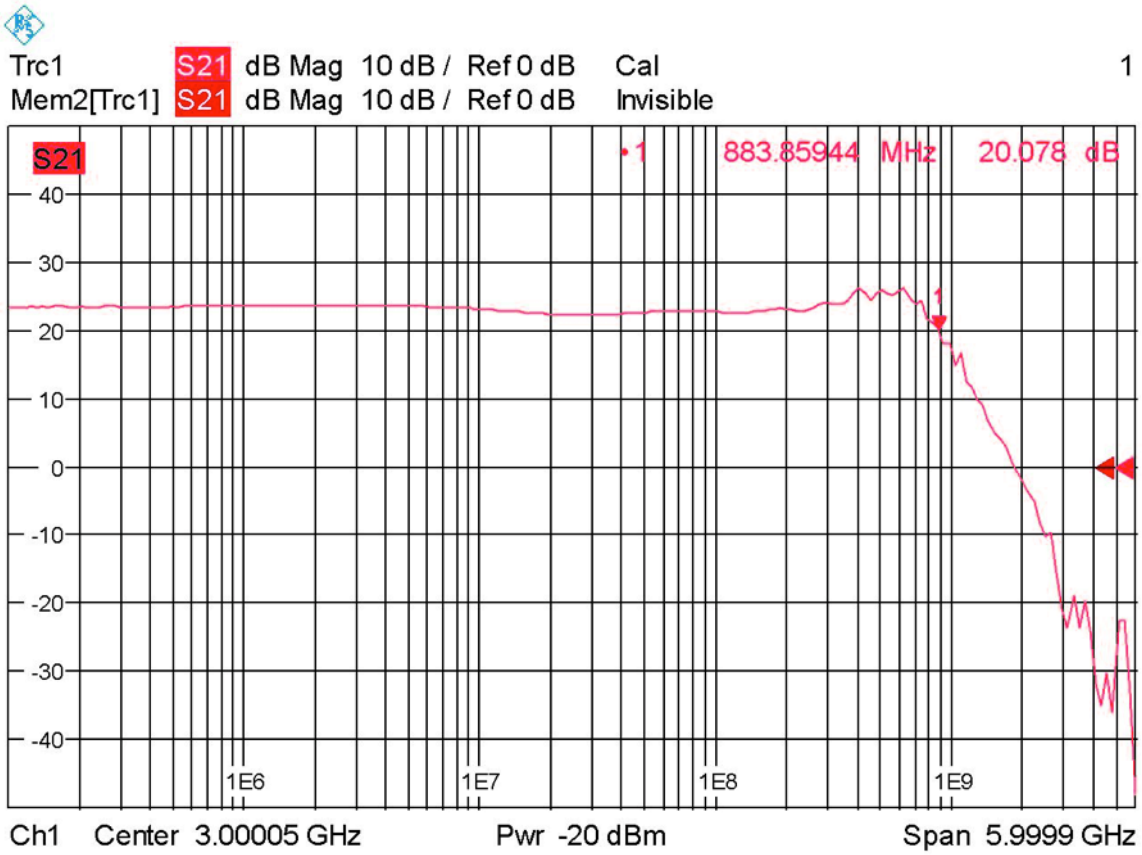
C1	A	B	C	D	E
1	3.3V	FAN_1	POWER_ON_S2	POWER_ON_S1	POWER_ON_S0
2	spare	FAN_1	POWER_ON_S5	POWER_ON_S4	POWER_ON_S3
3	spare	FAN_1	POWER_ON_DCB	POWER_ON_S7	POWER_ON_S6
4	spare	FAN_2	POWER_ON_S9	POWER_ON_S8	POWER_ON_TCB
5	spare	FAN_2	POWER_ON_S12	POWER_ON_S11	POWER_ON_S10
6	/INIT	FAN_2	POWER_ON_S15	POWER_ON_S14	POWER_ON_S13
7	/FLASH_SELECT	FAN_3	/SELECT 2	/SELECT 1	/SELECT 0
8	GND	FAN_3	/SELECT 5	/SELECT 4	/SELECT 3
9	SPI_CLK_P	FAN_3	/SELECT DCB	/SELECT 7	/SELECT 6
10	SPI_CLK_N	5V	/SELECT 9	/SELECT 8	/SELECT TCB
11	GND	TEMP_SENSE_1	/SELECT 12	/SELECT 11	/SELECT 10
12	SPI_MOSI_P	GND	/SELECT 15	/SELECT 14	/SELECT 13
13	SPI_MOSI_N	5V	PLUGIN S2	PLUGIN S1	PLUGIN S0
14	GND	TEMP_SENSE_2	PLUGIN S5	PLUGIN S4	PLUGIN S3
15	SPI_MISO_P	GND	PLUGIN DCB	PLUGIN S7	PLUGIN S6
16	SPI_MISO_N	5V	PLUGIN S9	PLUGIN S8	PLUGIN TCB
17	GND	TEMP_SENSE_3	PLUGIN S12	PLUGIN S11	PLUGIN S10
18	MSCB_P	GND	PLUGIN S15	PLUGIN S14	PLUGIN S13
19	MSCB_N	HV3	HV2	HV1	HV0

WaveDREAM Board (WDB)



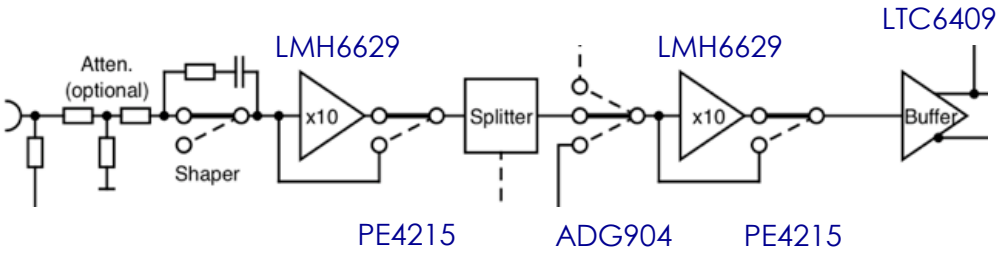
Drs4 based **REA**dout **M**odule

Preamp



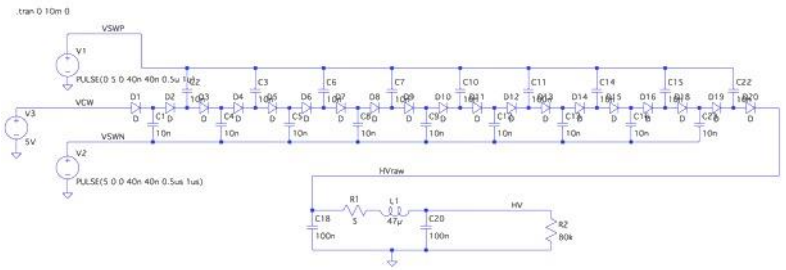
Gain	BW_{3db} (MHz)	Noise (mV)
1	940	0.37
10	880	0.40
100	300	1.2
100	500	1.7
100	800	3.3

Different compensations

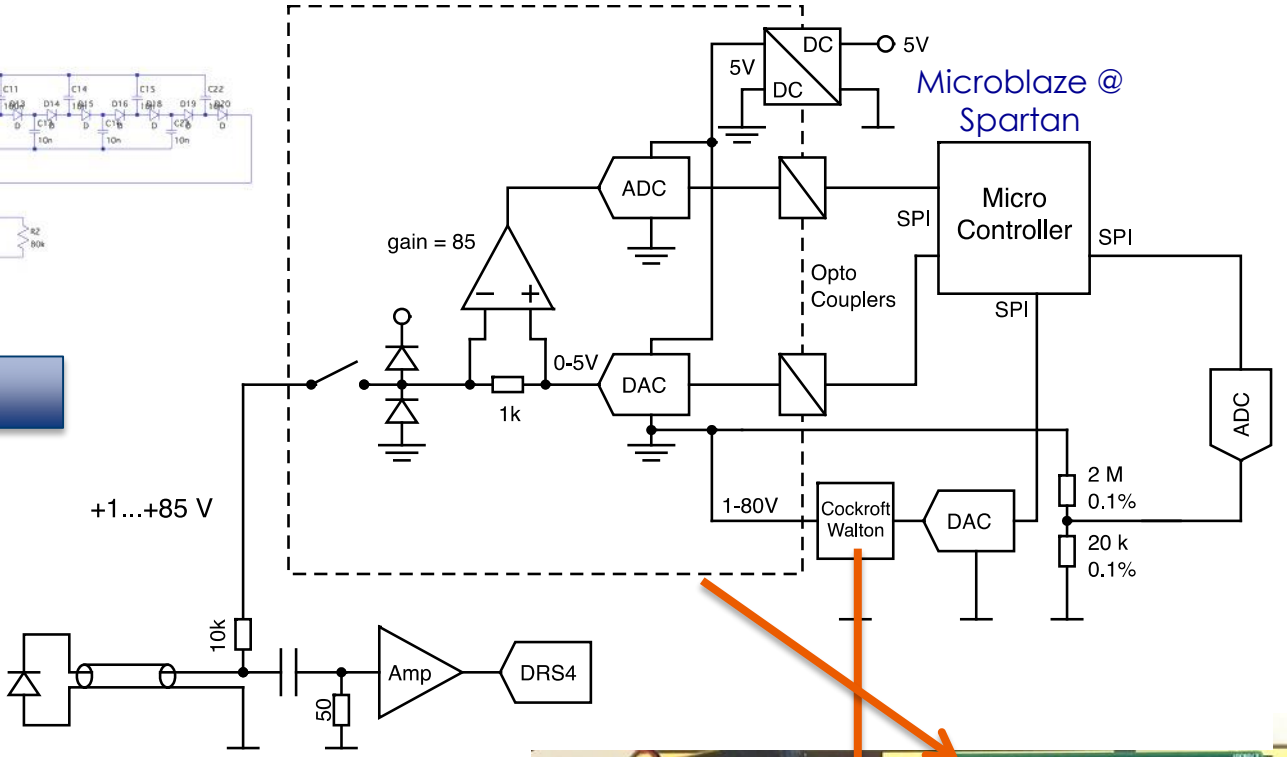


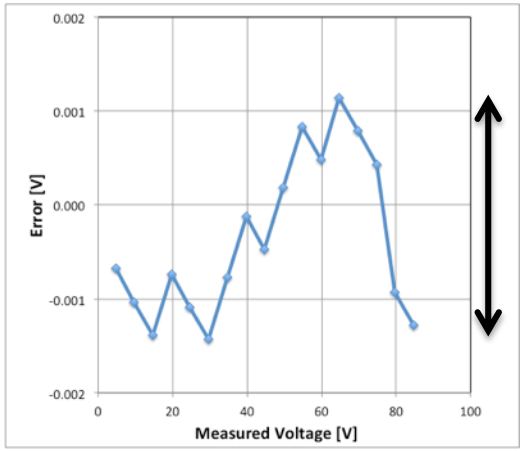
3.3 mV at output =
33 µV at input

WaveDREAM2 HV



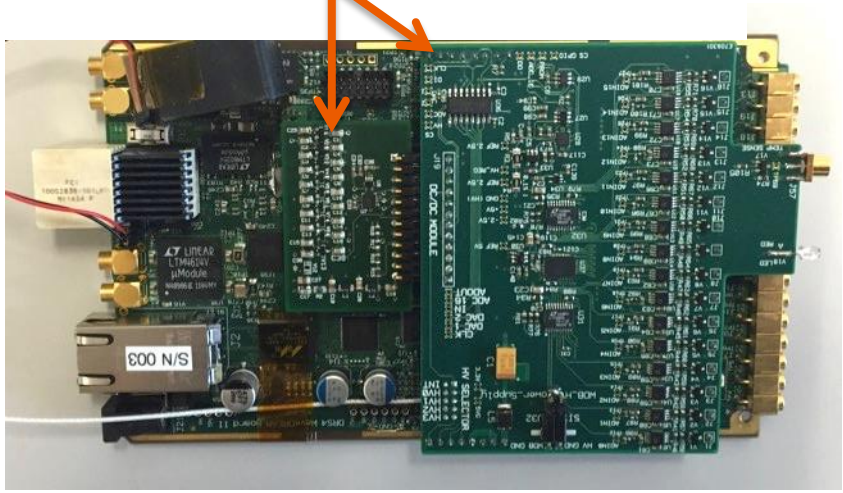
~ 20 US$ / channel





+/- 1mV

Ripple < 10 μV



Temperature Sensor Extension

maxim integrated™

DS18B20
Programmable Resolution
1-Wire Digital Thermometer

DESCRIPTION

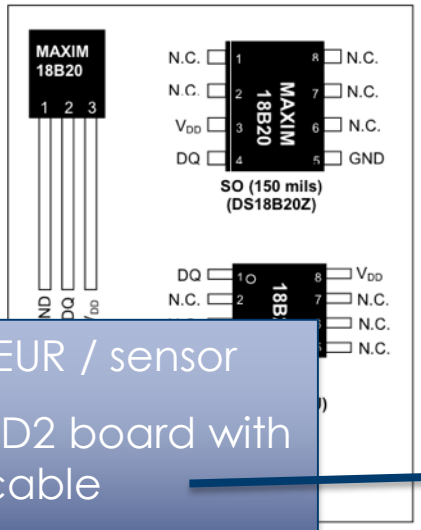
The DS18B20 digital thermometer provides 9-bit to 12-bit Celsius temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18B20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of -55°C to +125°C and is accurate to ±0.5°C over the range of -10°C to +85°C. In addition, the DS18B20 can derive power directly from the data line ("parasite power"), eliminating the need for an external power supply.

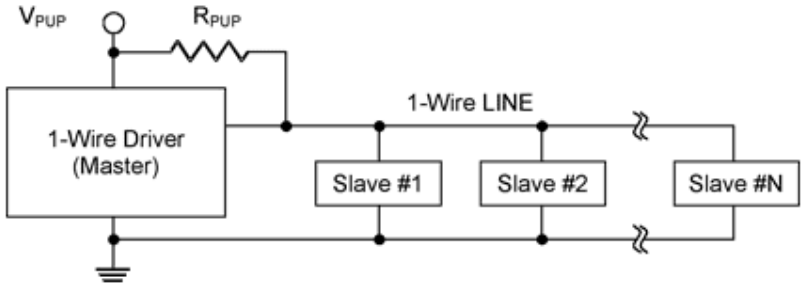
Each DS18B20 has a unique 64-bit serial code, which allows multiple DS18B20s to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many DS18B20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, or machinery, and process monitoring and control systems.

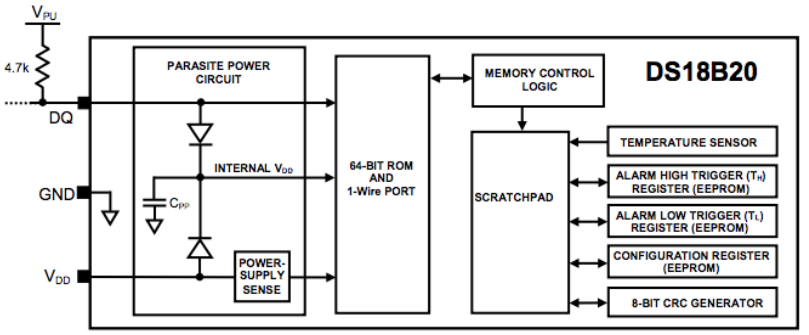
FEATURES

- Unique 1-Wire® Interface Requires Only One Port Pin for Communication
- Each Device has a Unique 64-Bit Serial Code
- User-Definable Nonvolatile (NV) Alarm Settings
- Alarm Search Command Identifies and Addresses Devices Whose Temperature is Outside Programmed Limits (Temperature Alarm Condition)
- Available in 8-Pin SO (150 mils), 8-Pin µSOP, and 3-Pin TO-92 Packages
- Software Compatible with the DS1822
- Applications Include Thermostatic Controls, Industrial Systems, Consumer Products, Thermometers, or Any Thermally Sensitive System

PIN CONFIGURATIONS

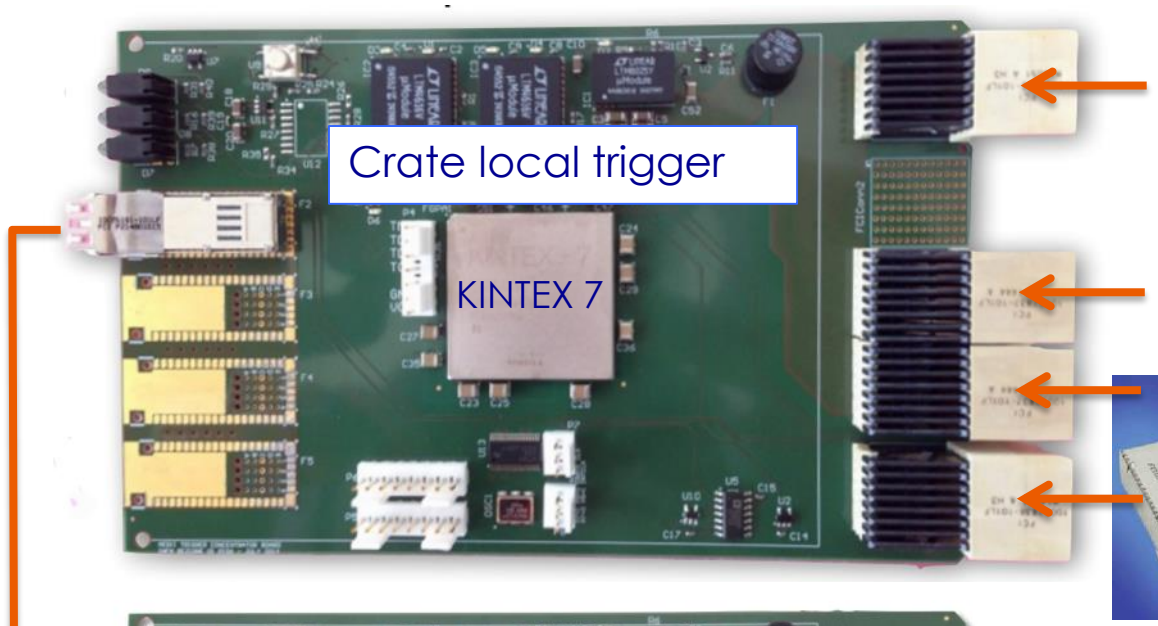


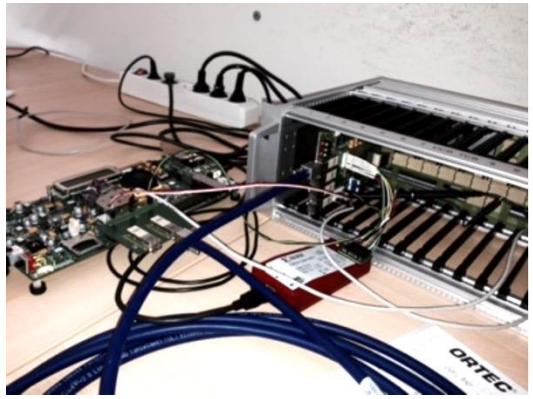


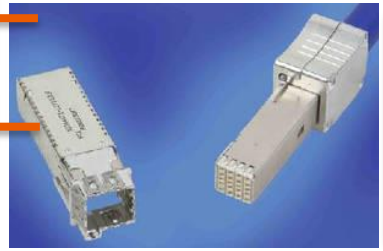


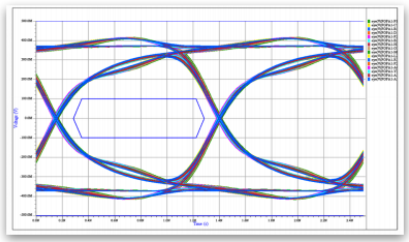
- accuracy ±0.5°, 3 EUR / sensor
- 1-16 sensors per WD2 board with only one coaxial cable
- Automatic HV adjustments with temperature changes

Trigger Concentrator Board (TCB)





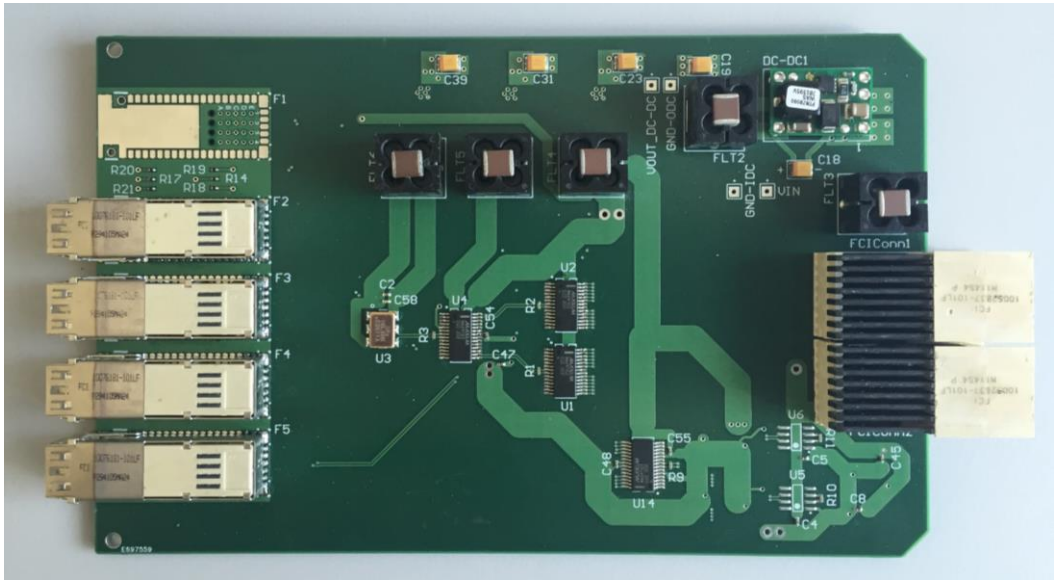


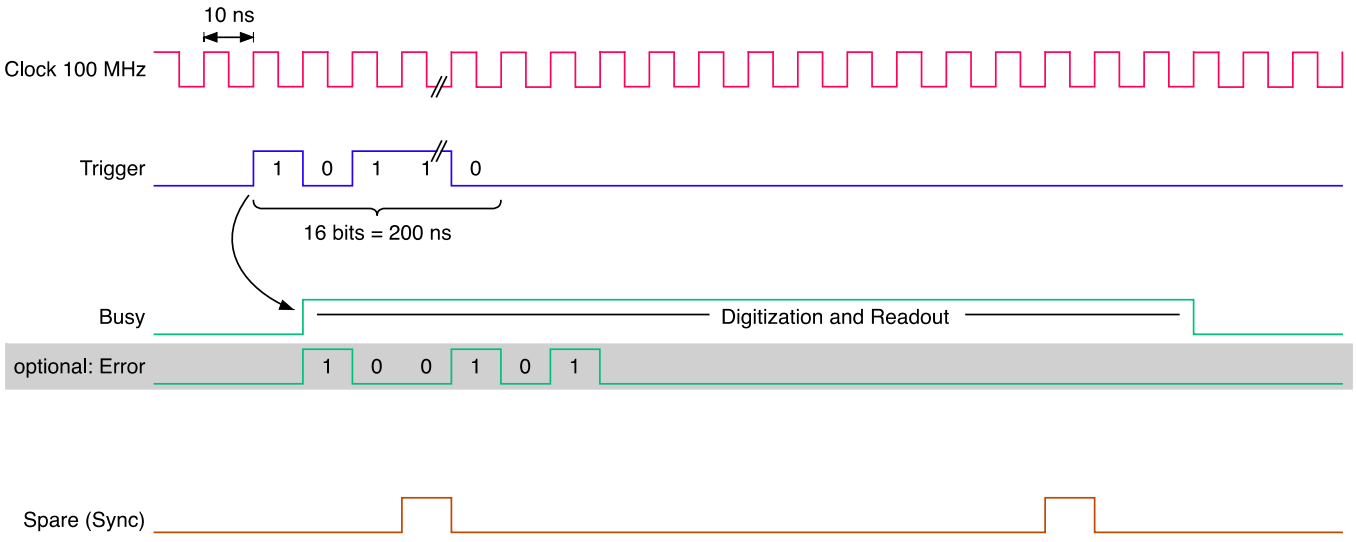


- Receives serial links (SERDES) from WD boards
- Computes crate local trigger
- Send trigger via serial links to global trigger in dedicated crate
- FCI Densishield cables

Ancillary system

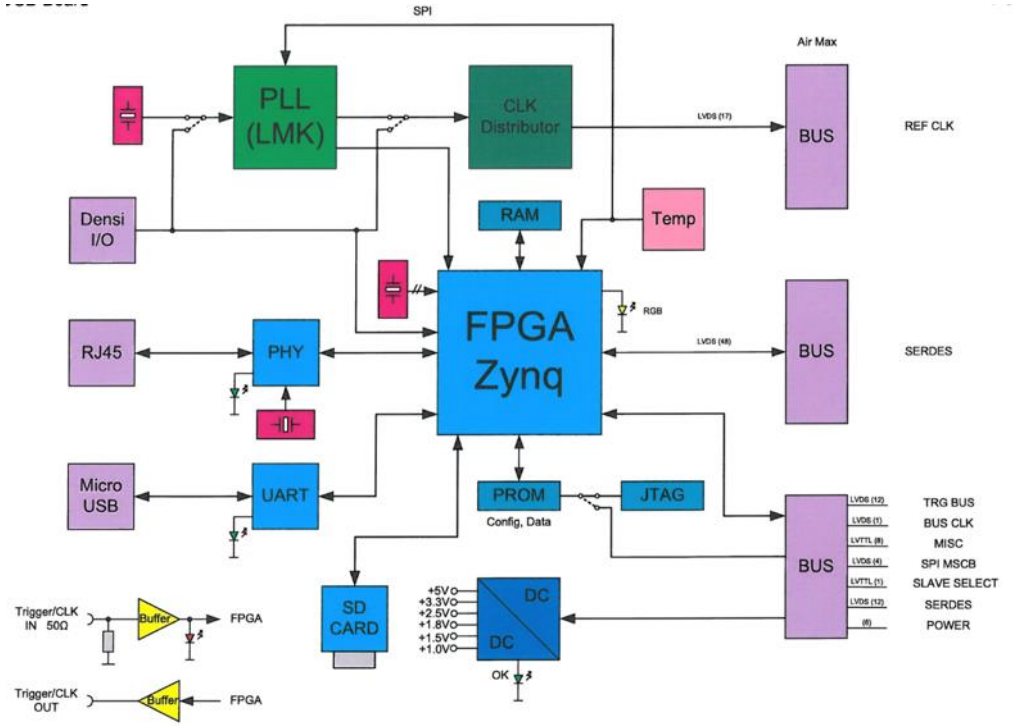
- Contains master clock
- Distribute clock
  (jitter < 12 ps measured)
- Distribute trigger
- 4 diff. pairs for
  - Clock
  - Trigger
  - Busy
  - (Sync)

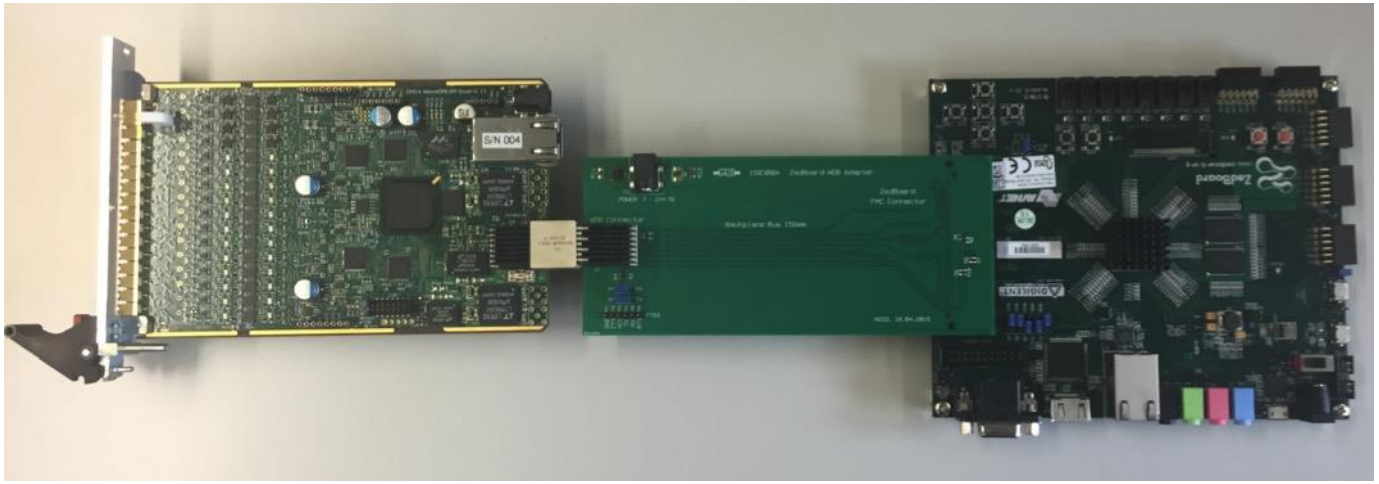




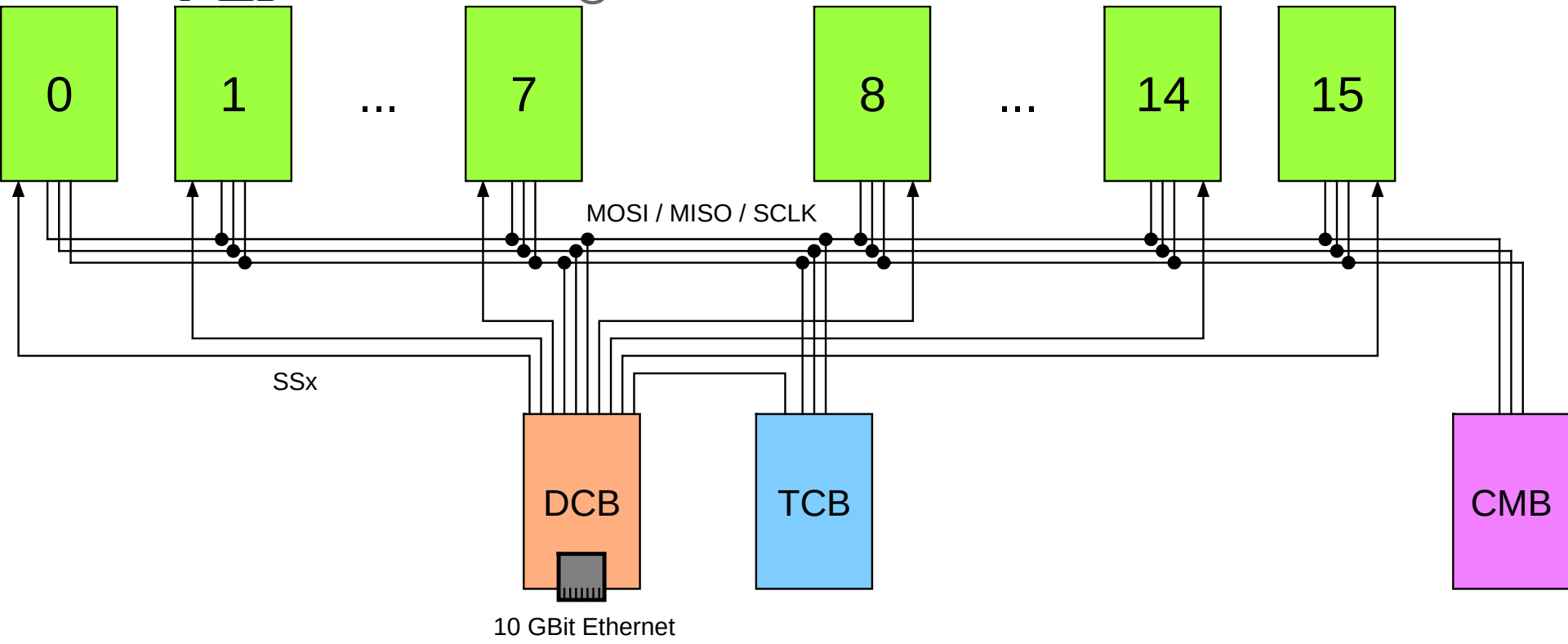
DAQ Concentrator Board (DCB)

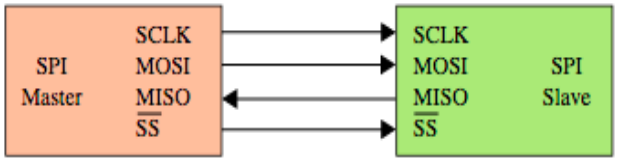
- Receive Gbit links from WDB
- Use SERDES instead GTX (lower latency)
- Waveform preprocessing in Zynq CPU
- Output via Gbit Ethernet (10 Gbit optional)
- Board under design
- Tests with Zed-Board and "Backplane Simulator"

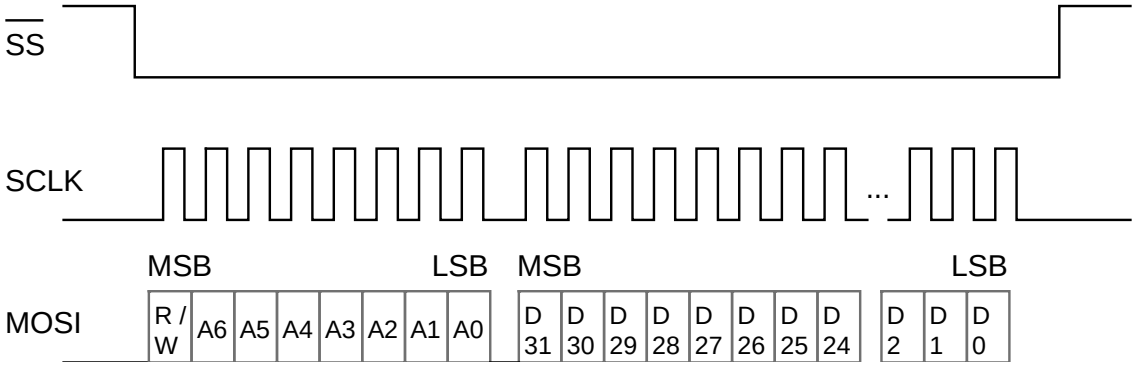




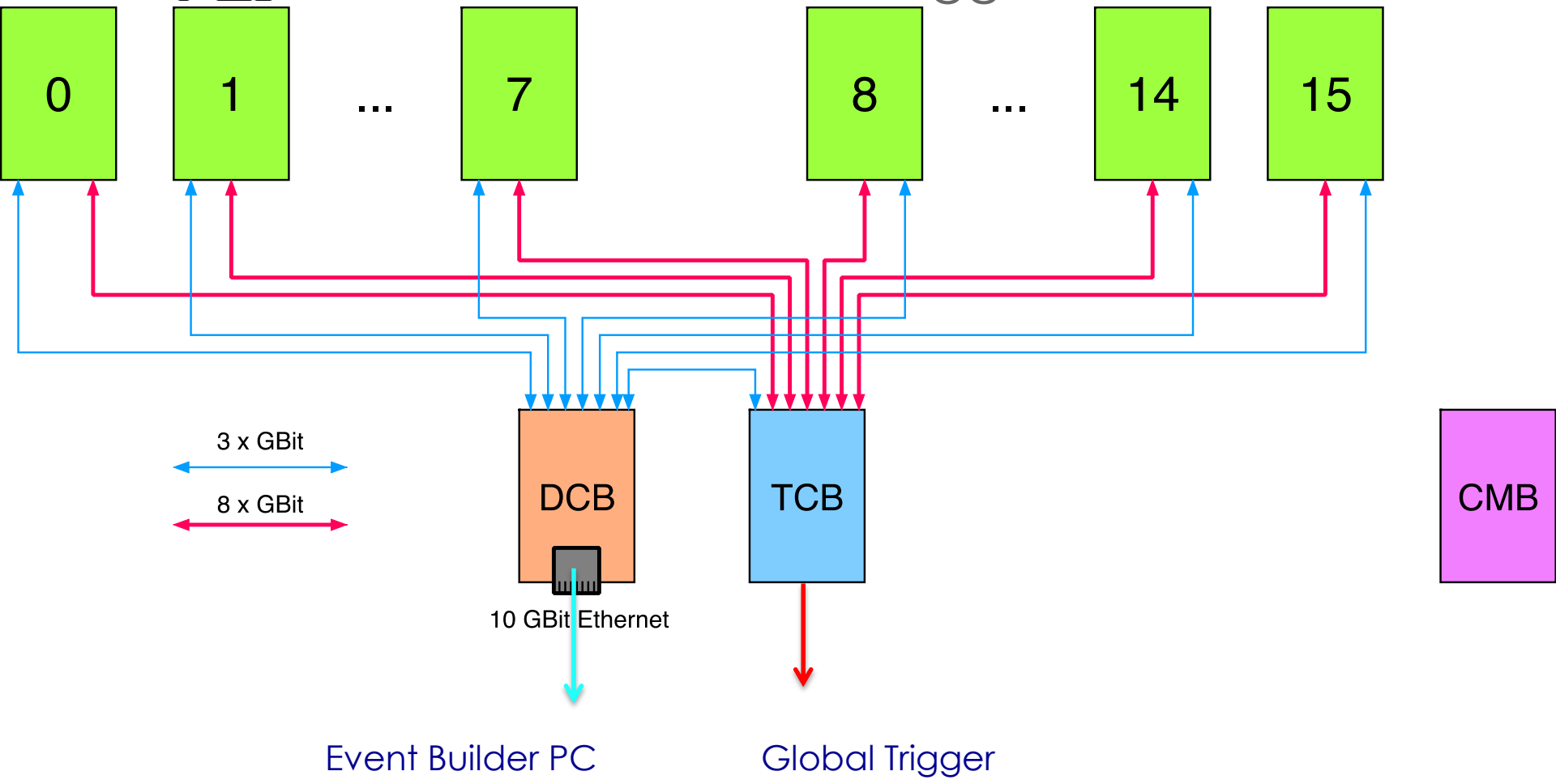
SPI configuration



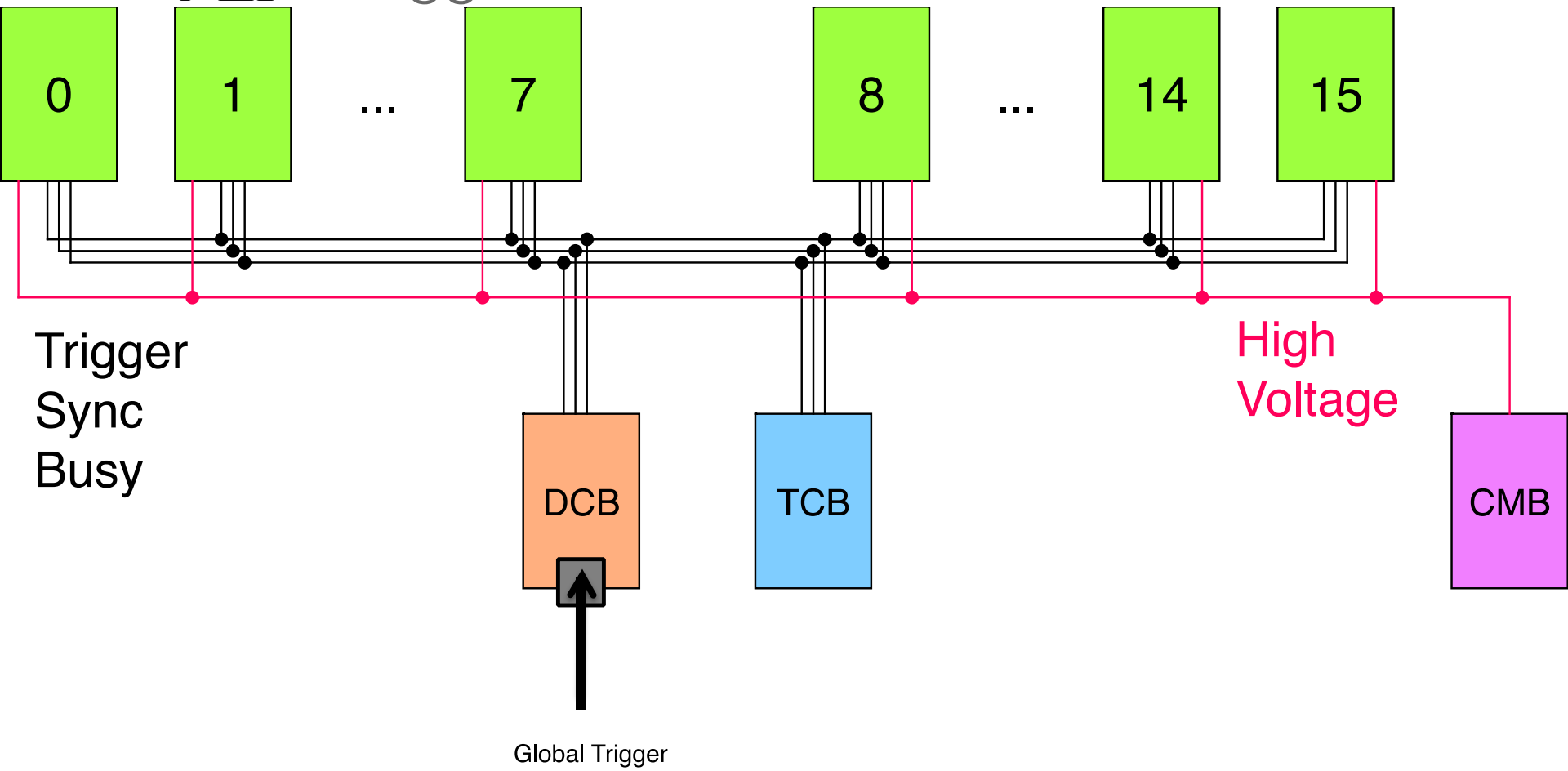




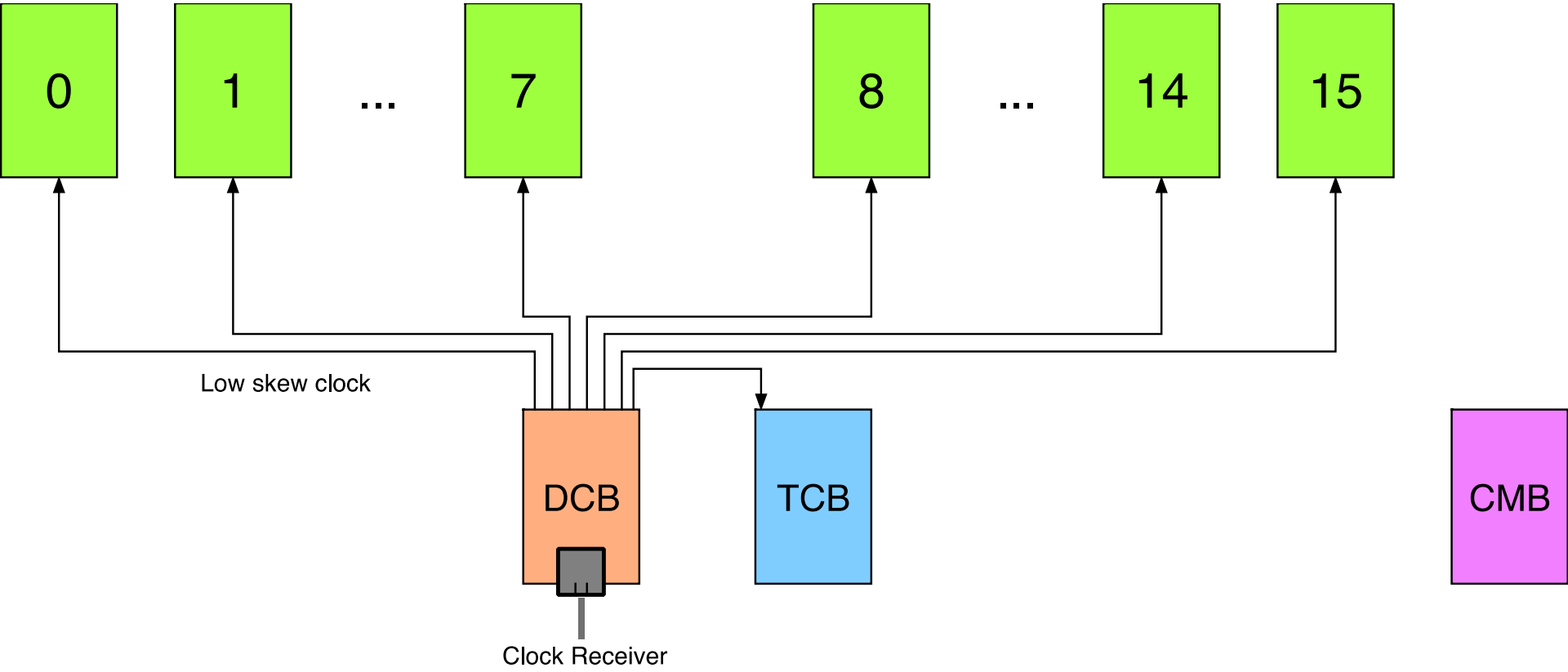
Gbit links for DAQ & Trigger



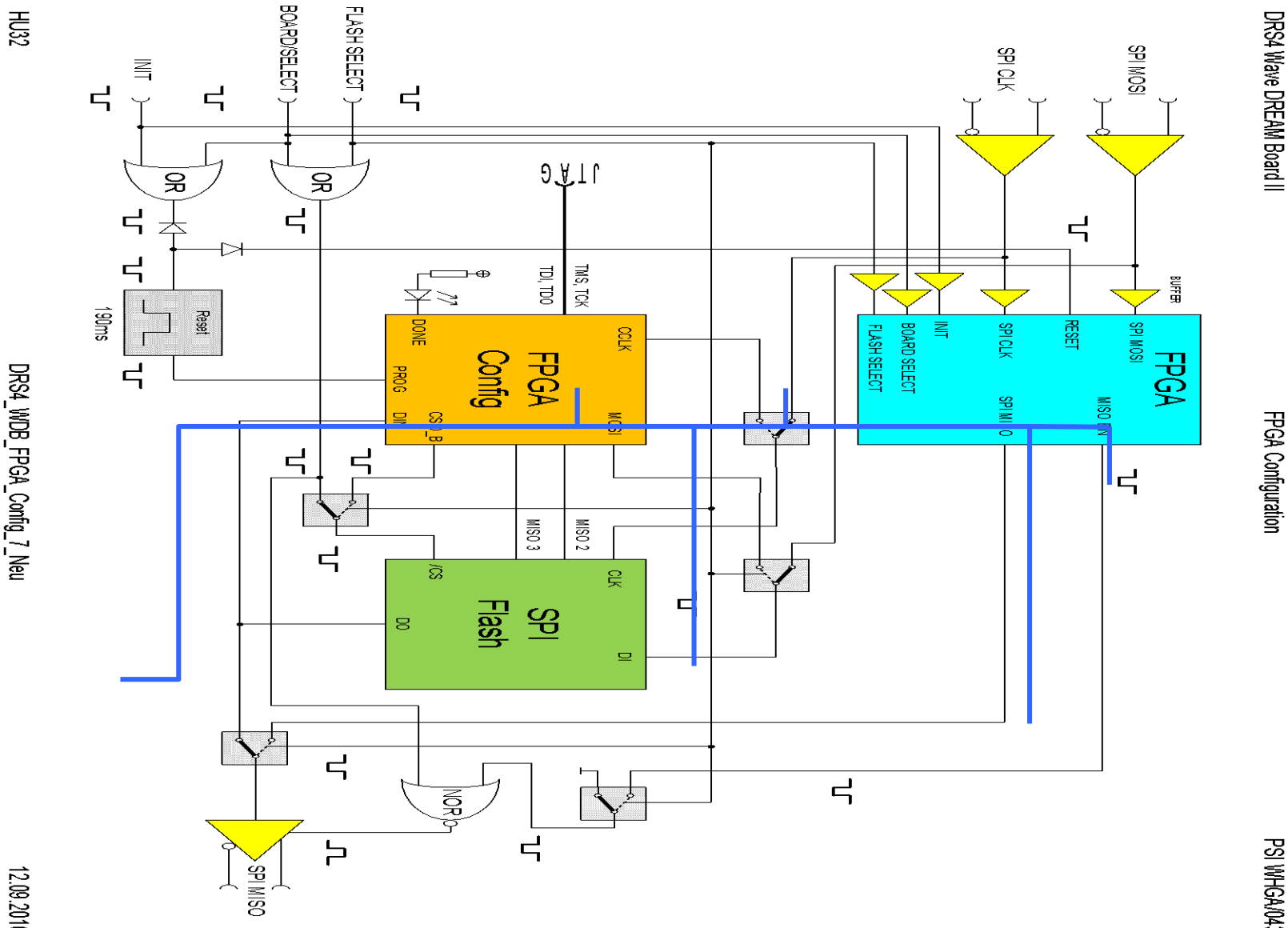
Trigger Bus & HV



Clock Distribution



SPI Flash Access Select



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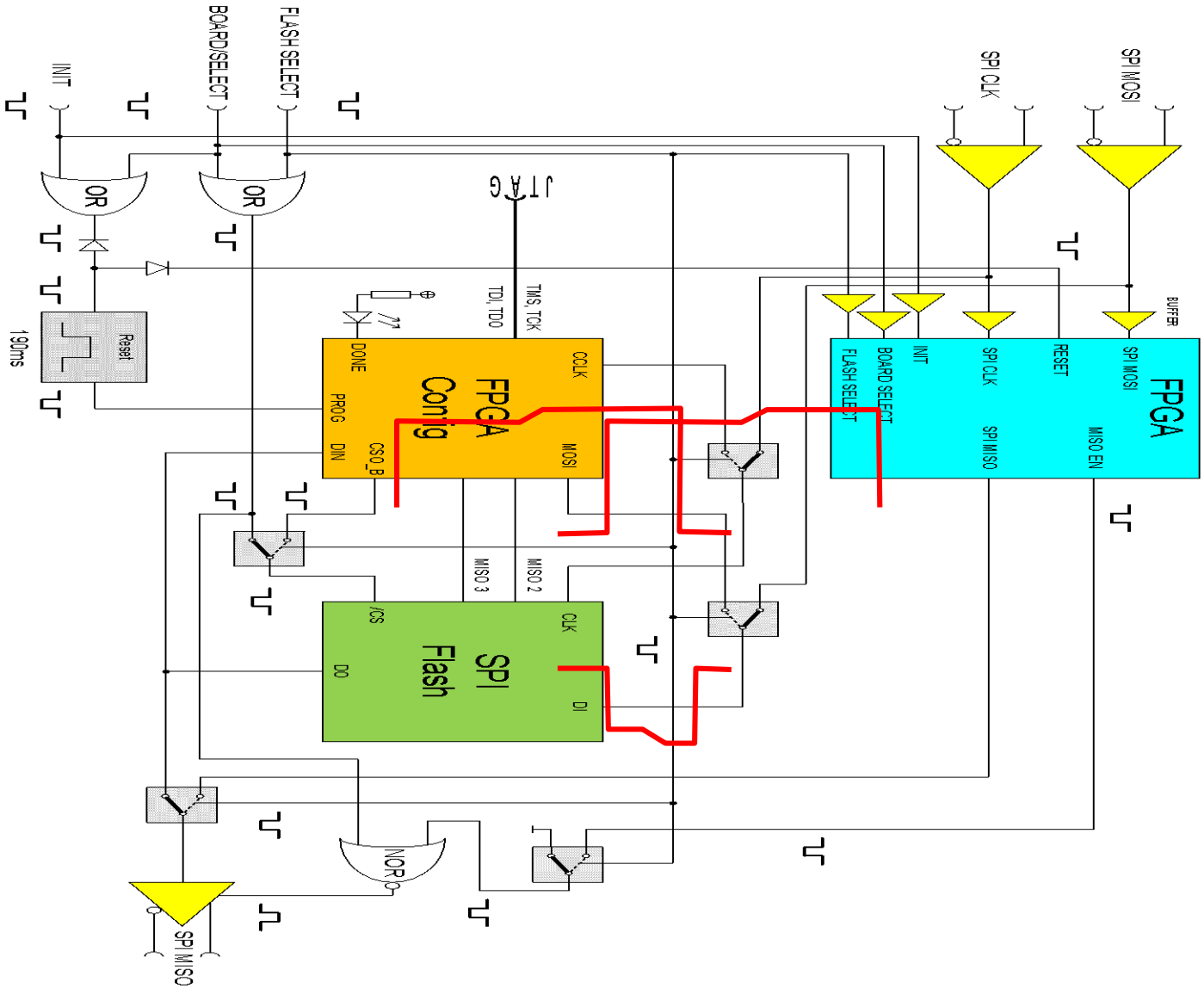
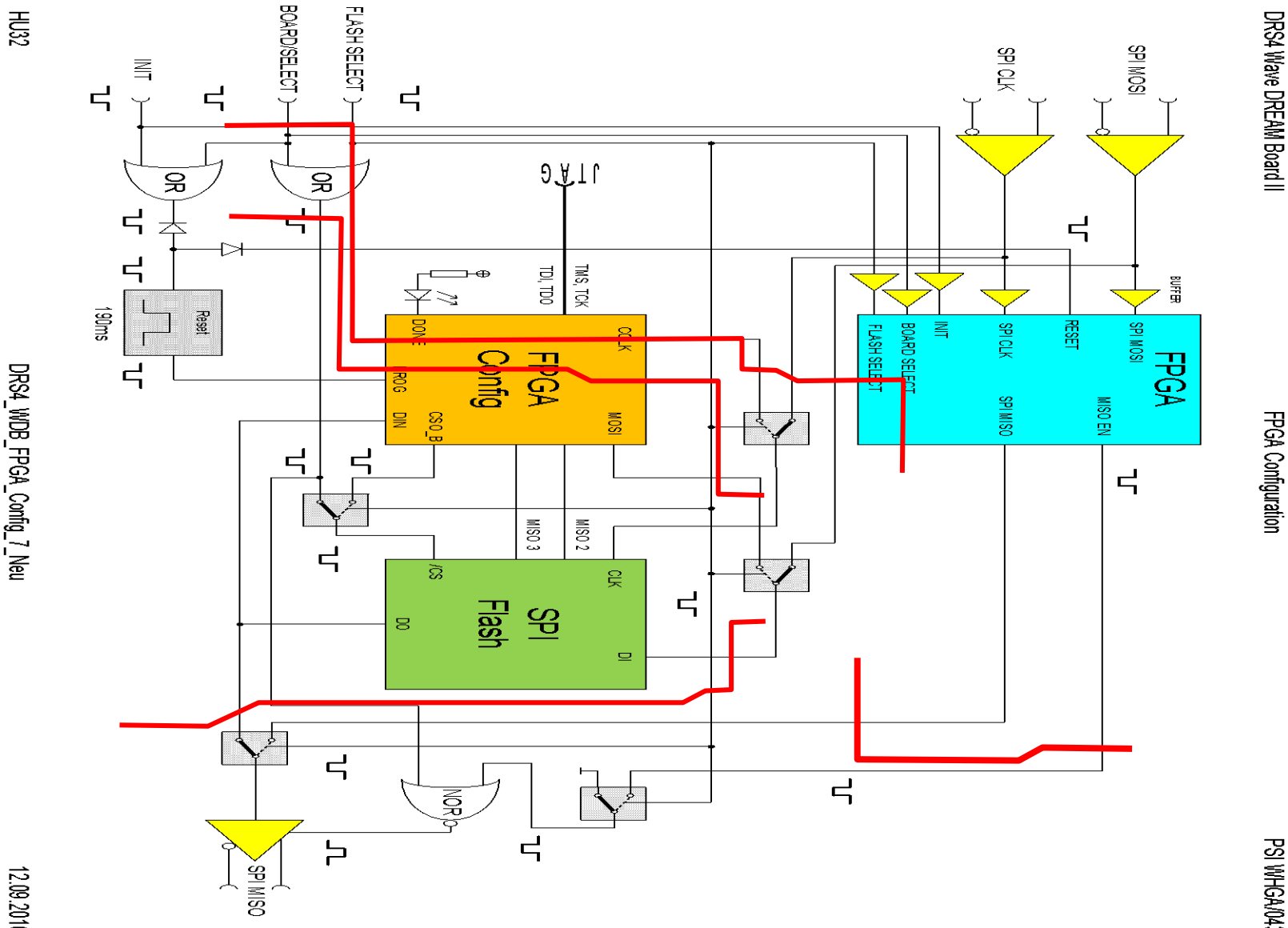
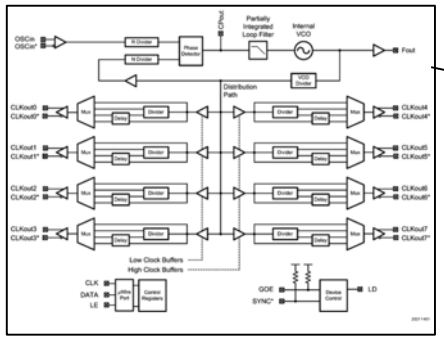
SPI Flash connected to FPGA



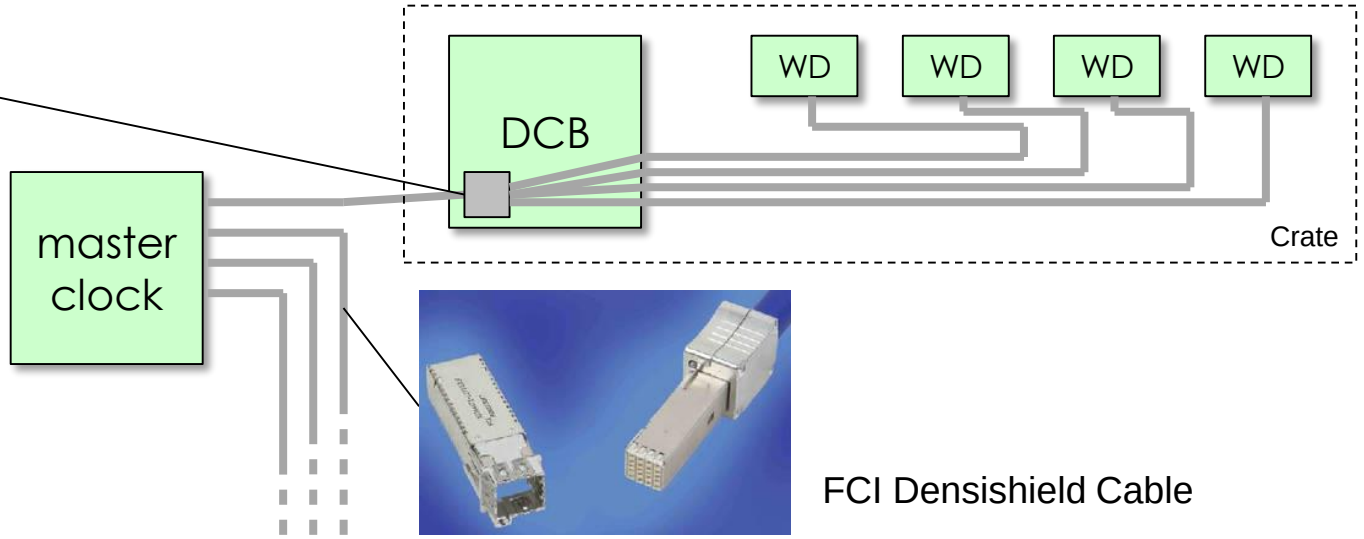
SPI Flash connected to backplane



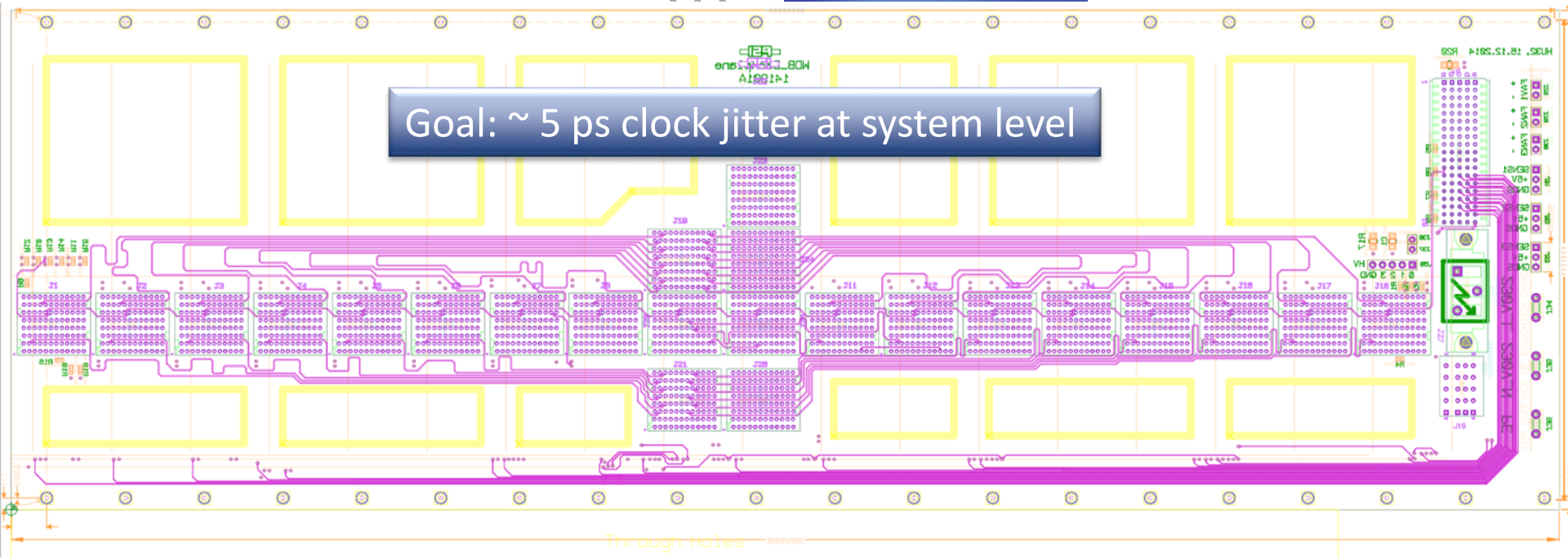
WaveDAQ Clock Distribution



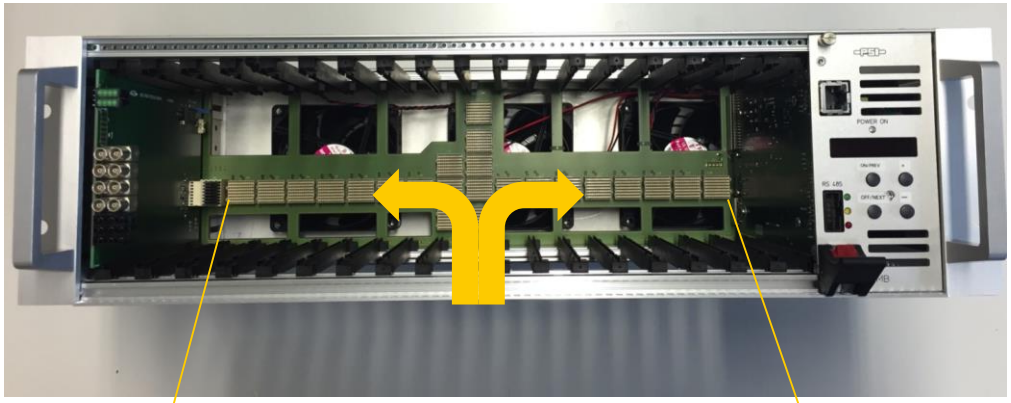
LMK03000 Jitter Cleaner



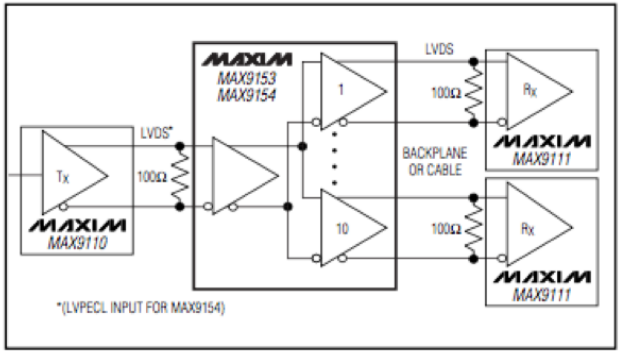
FCI Densishield Cable



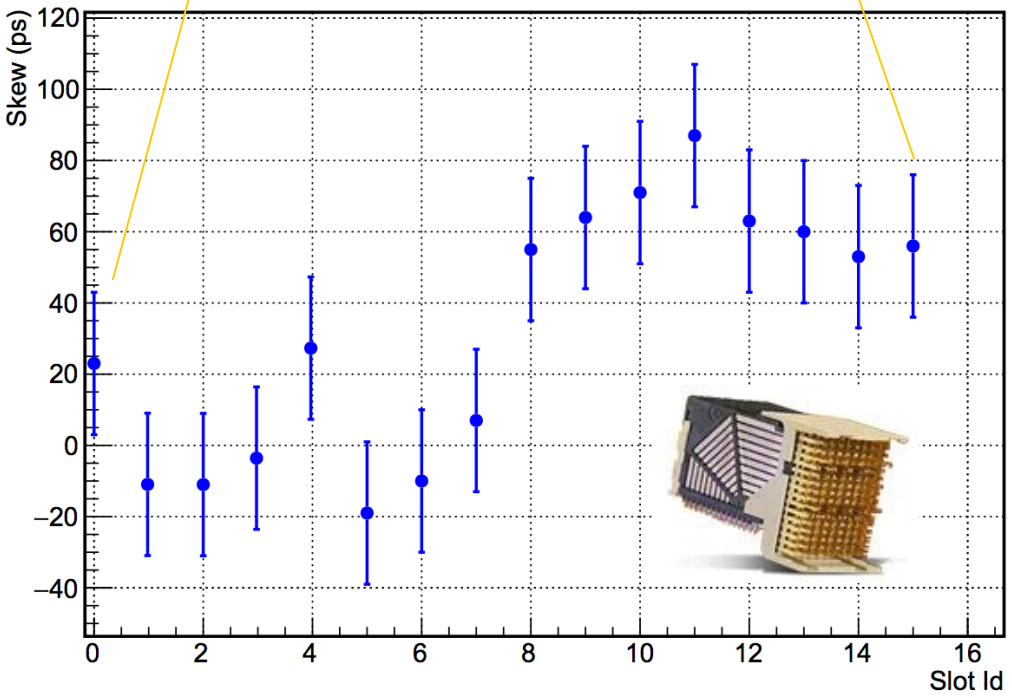
Clock skew



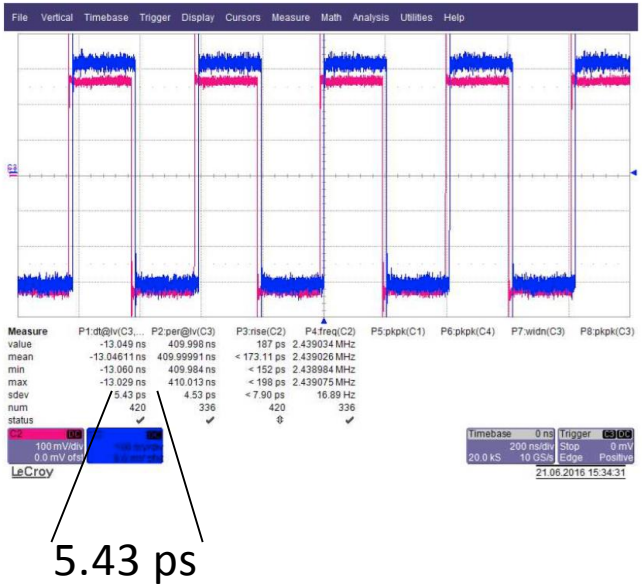
MAX9153 LVDS Repeater (1 ps Random Jitter)



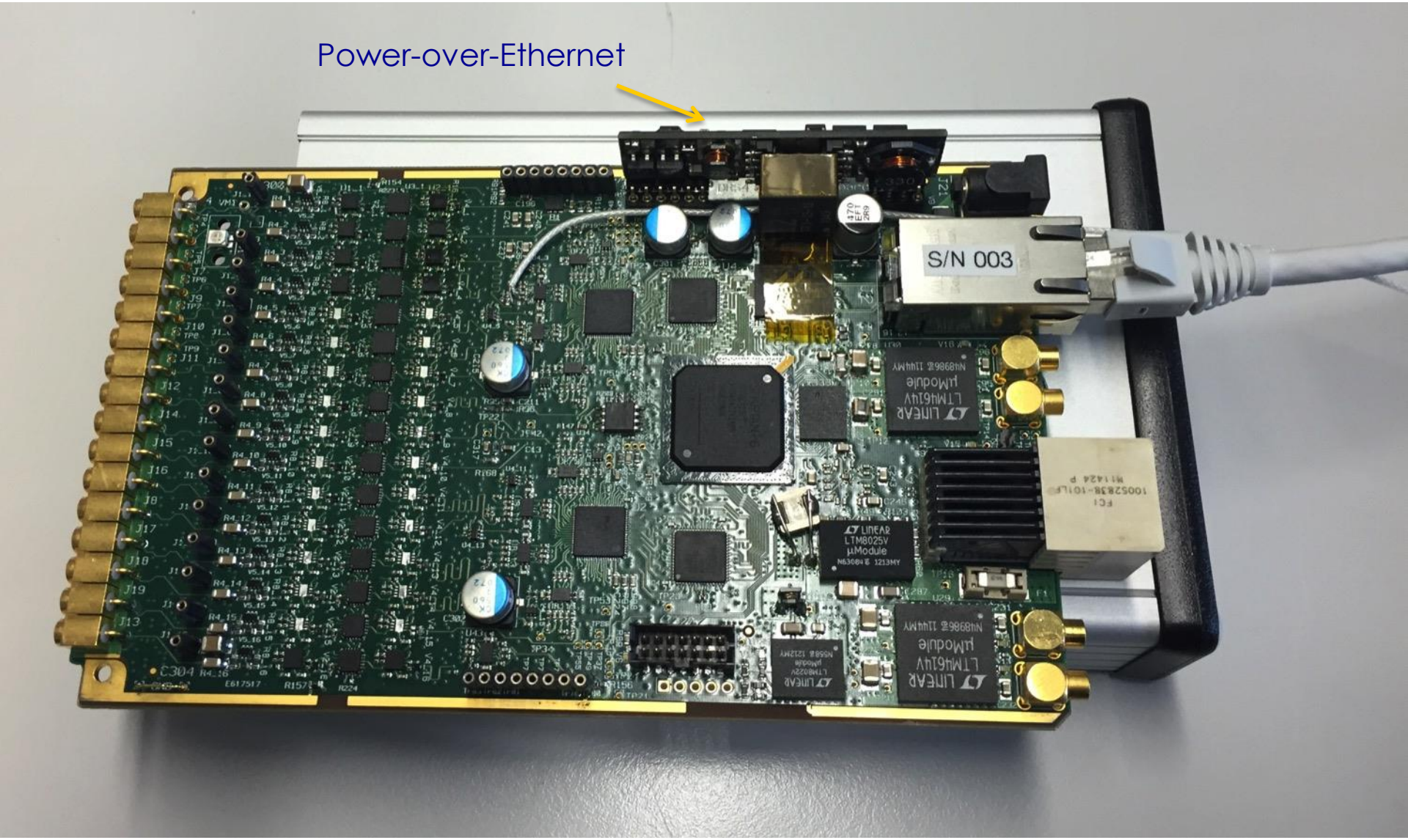
Reference CLK skew



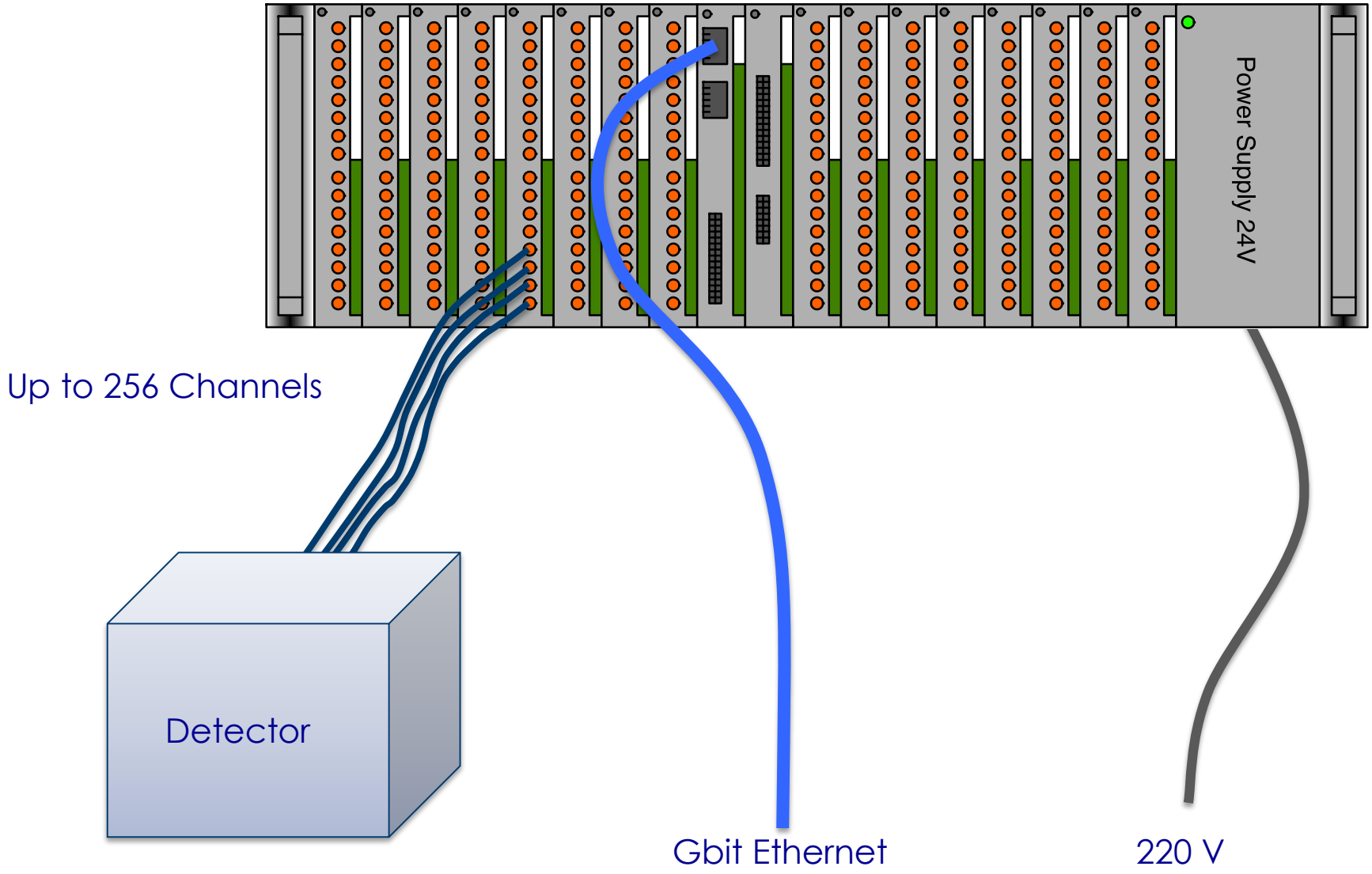
Random Jitter



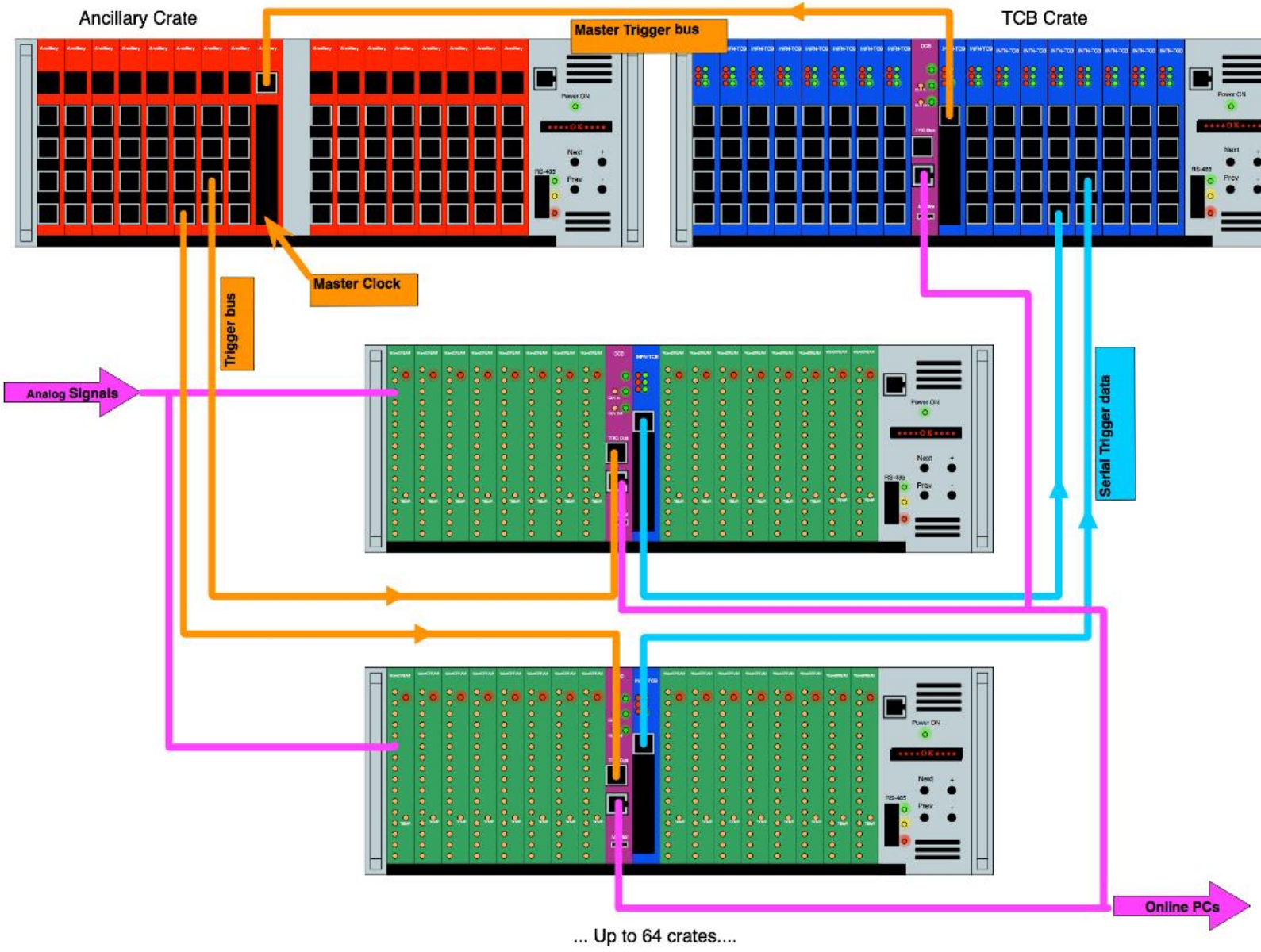
Minimal System



One-crate system Trigger & DAQ



MEG II System



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Some lessons learned

Which is the best voltage regulator ?

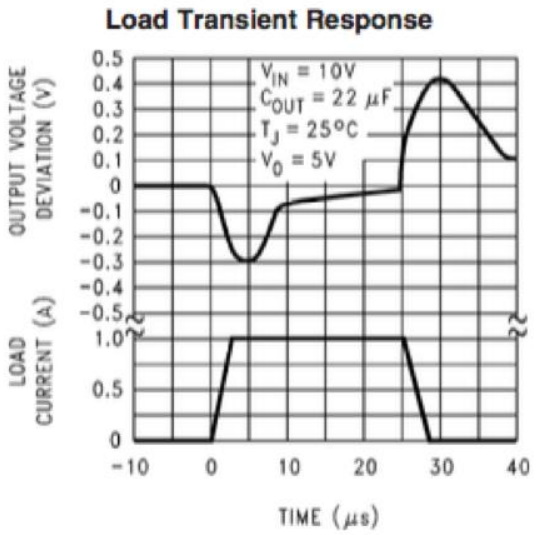
- Switching regulator (DC-DC converter)
  - high efficiency
  - switching noise
  - not suited for analog designs

- Linear regulator
  - lower efficiency ("burns" power to reduce voltage)
  - no switching noise
  - suited for analog designs

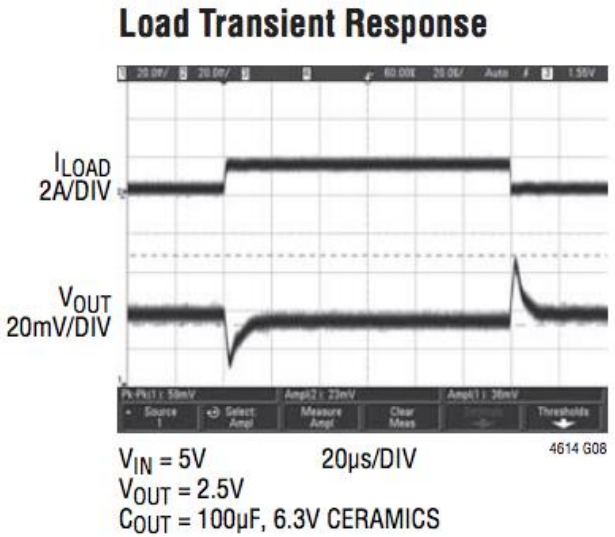
Which is the best voltage regulator ?

- Linear regulator shows a larger response to load transients
- Switching noise can be filtered very efficiently
- **E**lectro **M**agnetic **I**nterference getting better these days

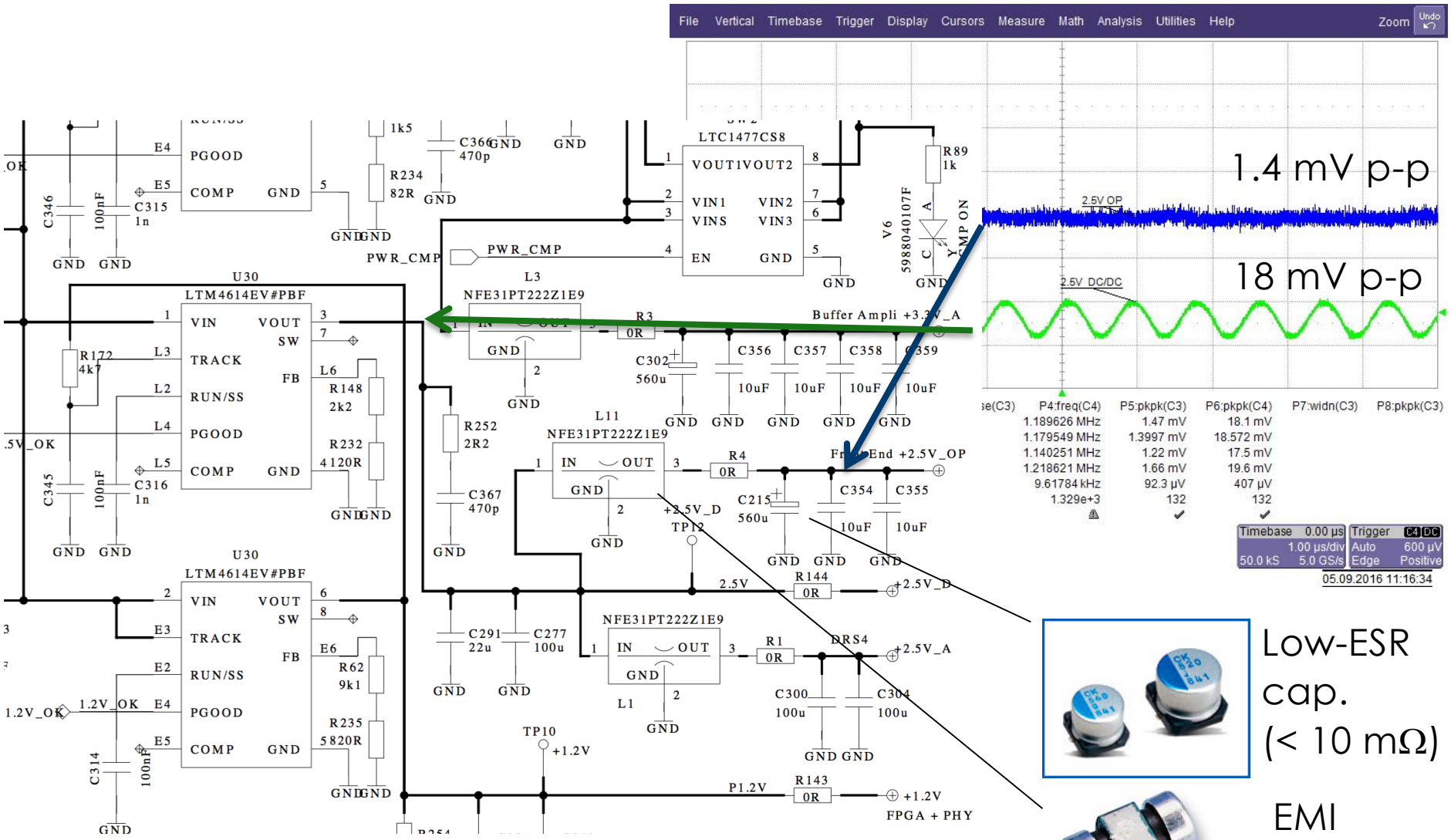
LM2941
(linear)



LTM4614
(switched)

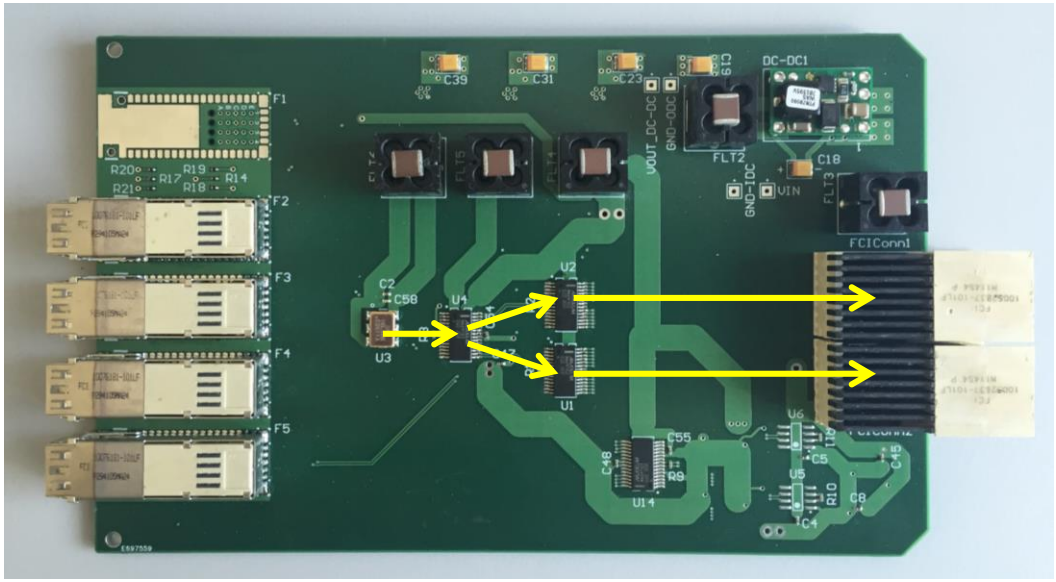


Switching Regulator Noise

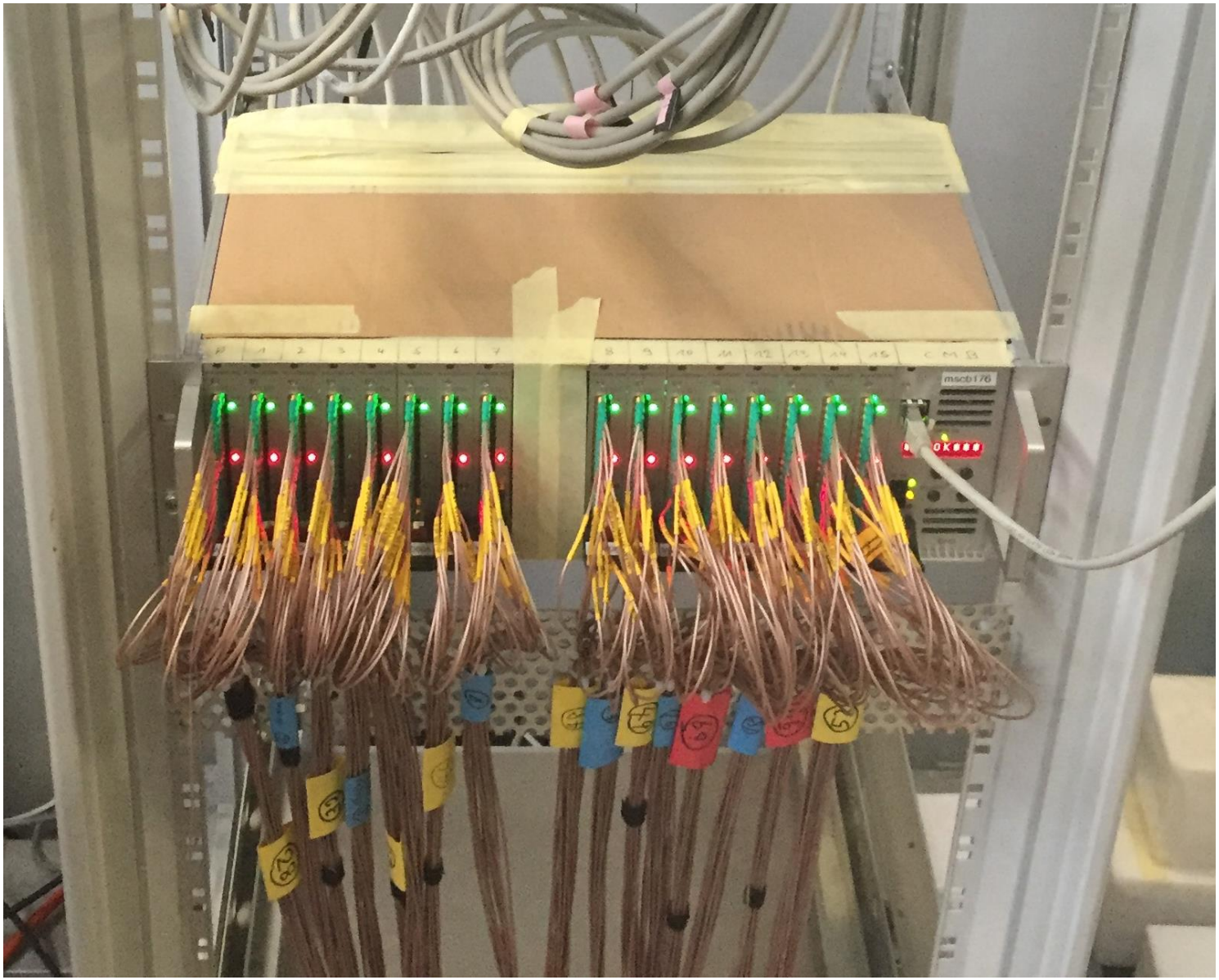


Optimal Clock Distribution

- "Simple" low jitter oscillator is enough (e.g. ASEMPLV-100) (no atomic clock required!)
- Precision clock distribution **ONLY** point-to-point with low jitter LVDS repeater (e.g. MAX9153), **NEVER** split a clock passively
- Power supply noise << 1 mV



Beam test 1 full crate



WaveDAQ Performance

- Trigger resolution 10 ns (100 MHz clock)
- Trigger bandwidth 8 Gbit / s
- Trigger latency <380 ns *) (9000 channels)

- DAQ bandwidth 2 Gbit / s
- DAQ time measurement 10 ps *)
- DAQ dead time 3 - 35 μs / event

- MEG II: 7 x 10^7 μ/s, DAQ eff. > 95% @ 30 Hz *)

*) projected

Conclusions

- WaveDAQ system has been designed to fulfill needs of MEG II experiment
- System has huge potential for many others (costs: ~150 US$ / channel incl. crate, power, HV)
- Status: Crate fully working, trigger board and WaveDREAM board successfully tested, beam test 2015, DCB under design
- 4 crate system end of 2016, full system (35 crates) in 2017
- DRS5 chip (no dead-time) planned for 2018+

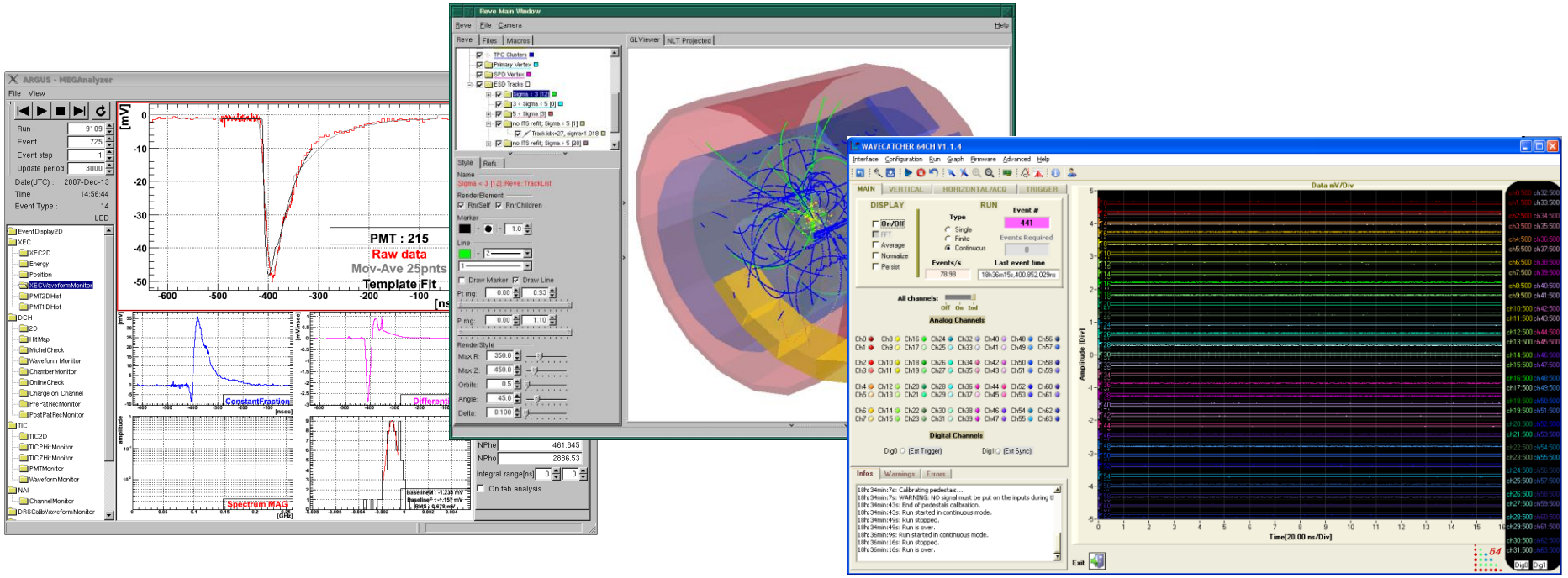
Not without -

My thanks go to

- Ueli Hartmann, PSI
- Luca Galli, INFN Pisa
- Elmar Schmid, PSI
- Gerd Theidel, PSI
- Roberto Dinapoli, PSI

Extra: Visualization with HTML5

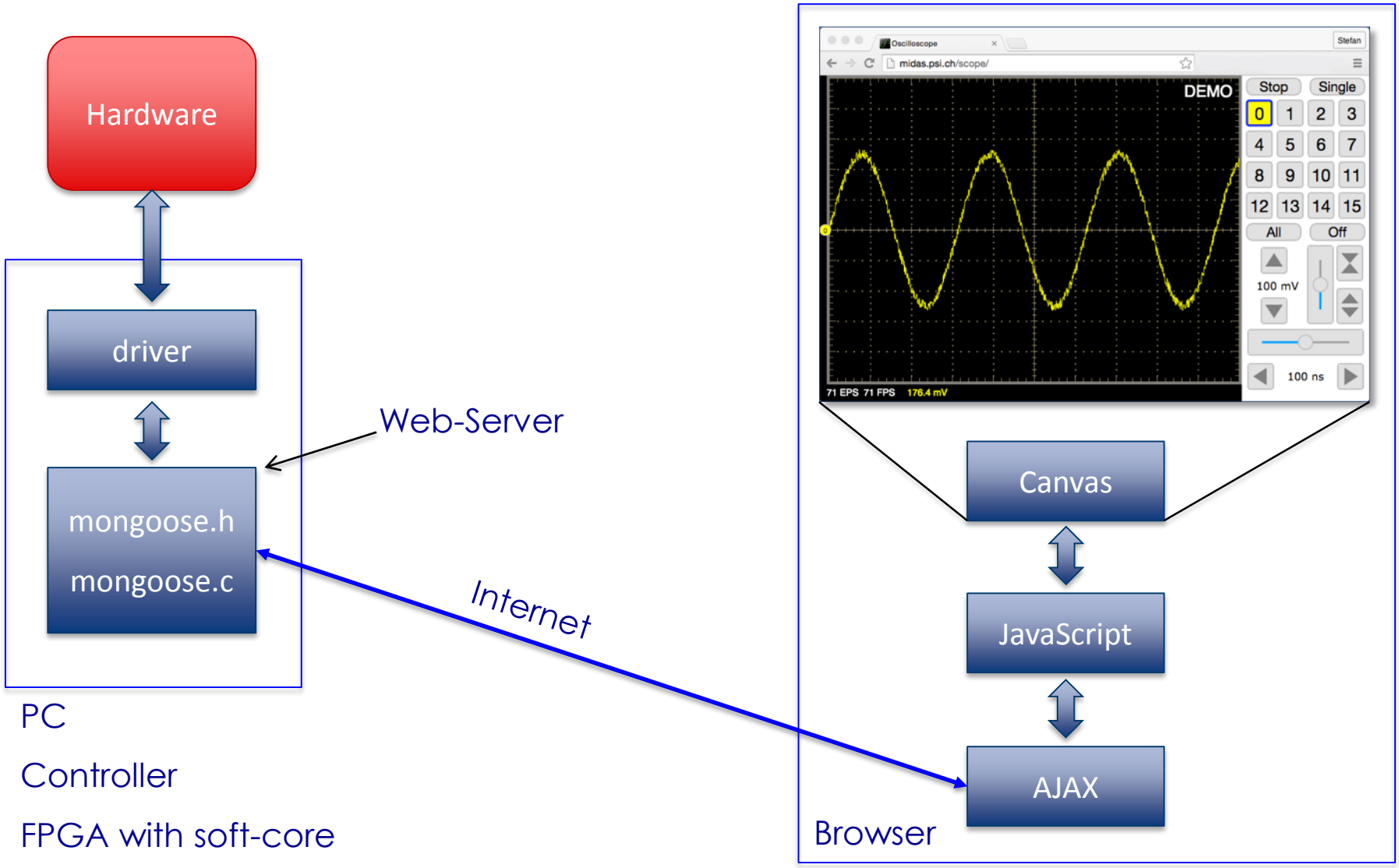
- The traditional way
  - Dedicated programs (ROOT, Qt, TCL/TK, Labview, ...)
  - Must be compiled for different OS
  - Require certain libraries to be installed
  - Limited smartphone support



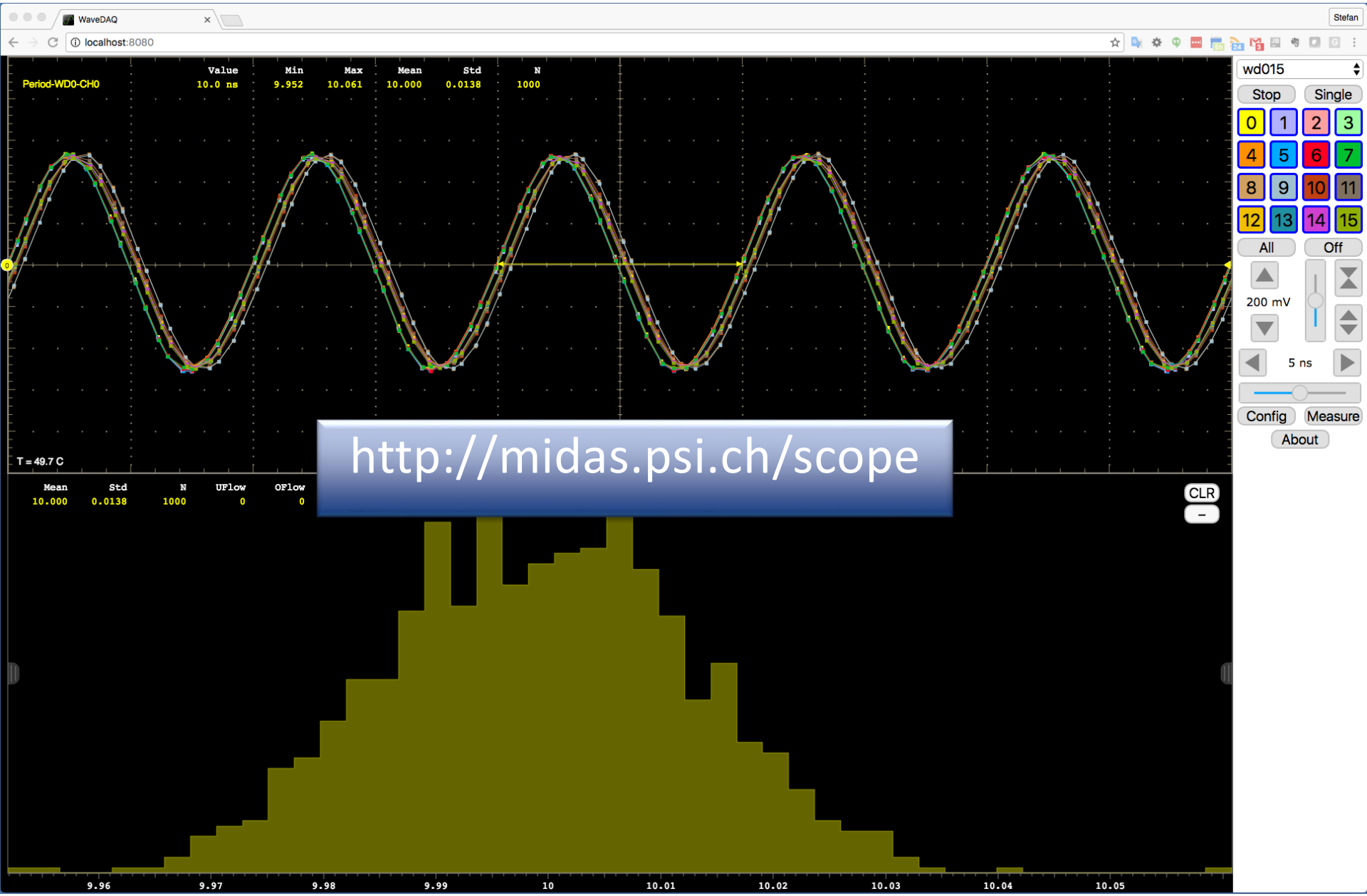
A new opportunity

- Visualization can now be done directly inside the browser using HTML5 – CSS3 – JavaScript – JSON
- Modern browsers run JavaScript at the speed of native programs some years ago
- <canvas> functions are very powerful
- Software updates get deployed automatically
- Automatic support for tablets and smartphones
- Use mongoose library on server side

Remote Data Visualization



Demo


WaveDAQ
Stefan
localhost:8080
Value Min Max Mean Std N
Period-WD0-CH0
10.0 ns 9.952 10.061 10.000 0.0138 1000
wd015
Stop
Single
0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
All
Off
200 mV
5 ns
Config
Measure
About
T = 49.7 C
http://midas.psi.ch/scope
Mean Std N UFlow OFlow
10.000 0.0138 1000 0 0
CLR
9.96 9.97 9.98 9.99 10 10.01 10.02 10.03 10.04 10.05

Smartphone and Tablet