University of Sao Paulo

"Advanced Very Deep CMOS Technologies"

João Antonio Martino

University of São Paulo (USP), Brazil

martino@usp.br

4th Summer School on INtelligent signal processing for FrontIEr Research and Industry (INFIERI)

January 26th, 2017

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Outline

- ✓ University of São Paulo - SOI CMOS Group
- ✓ Seminar Presentation : CMOS Technologies
  - Basic concept : MOSFET
  - History: past, present, future
  - Experimental and simulation results

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Site: www.usp.br

*More than 2.000 Ph.D per year

The most important
University of Brazil
(First in Latin America)

90.000 Students
60.000 under graduation
30.000 Master and Ph.D

5.000 Faculty Member

Engineering
5.000 Students
500 Faculty Member

Electrical Engineering
1.200 Students
120 Faculty Member

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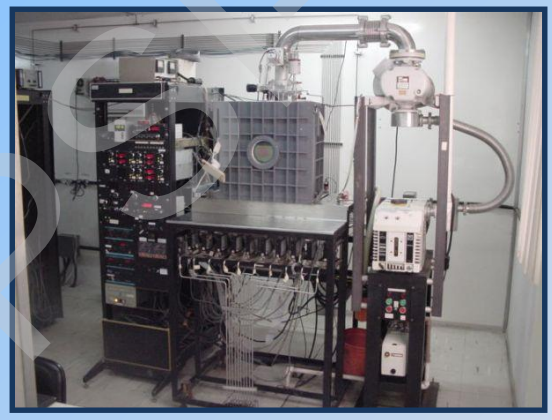
First Microelectronic Laboratory in Brazil (1968)



University Clean Room Facilities

University of Sao Paulo

University of Sao Paulo

Characterization Facilities

Microwave Measurement Systems

Optical Measurements Systems

Devices Characterization Laboratory

University of Sao Paulo

SOI CMOS GROUP since 1990
Electrical Engineering Department
University of Sao Paulo, Brazil

João Antonio Martino

M.Sc and Ph.D at USP
Pos-Doc : Imec/Belgium in 1990
Full Professor at USP since 2005
Chair of the EDS/IEEE South Brazil Chapter
Distinguished Lecturer of EDS/IEEE
Vice-Chair of Region 9 SRC

University of Sao Paulo

University of Sao Paulo

SOI CMOS GROUP at USP - 2016

All my present students and researchers of SOI CMOS Group (USP)

University of Sao Paulo

International Collaborations
Imec/KUL + UCL + Grenoble + Caen

University of Sao Paulo

SOI CMOS GROUP

Main Research Activities

1. Study of planar and Multiple Gate (3D) SOI MOSFETs (μ, Rs, DIBL, Vth, SS, GIDL, Ground Plane, Strained devices…)
   Electrical Characterization, modeling and Simulation (2D and 3D) as a function of Temperature (80K a 700K)

2. Radiated devices for medical/space applications

3. Microfabrication for research (FinFET - 3D Transistor) and educational application (Bulk and SOI Technology)

4. Study of UTBB SOI MOSFET and NW

5. Tunnel FET Devices (planar and NW)

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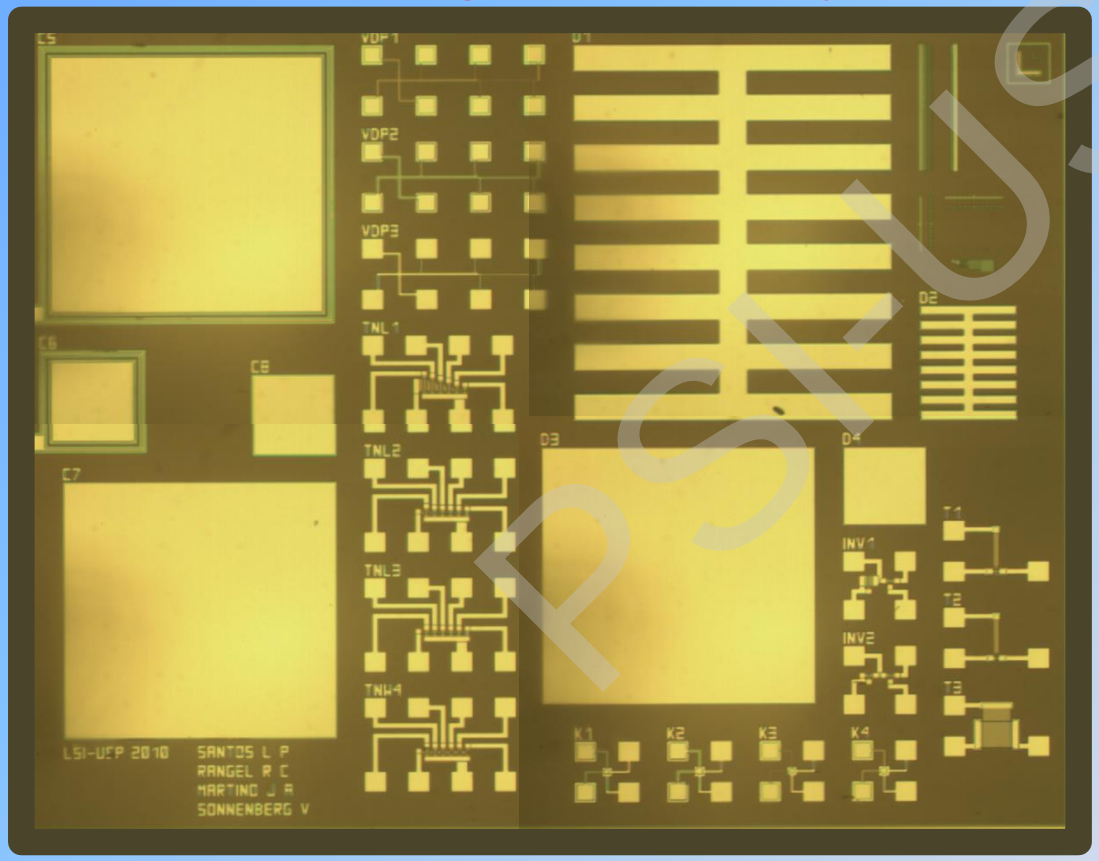
Nowadays at USP

Hands-on on Microelectronic Fabrication at University of Sao Paulo for educational application (NMOS polysilicon-gate)



Every year for undergraduate students at USP

University of Sao Paulo

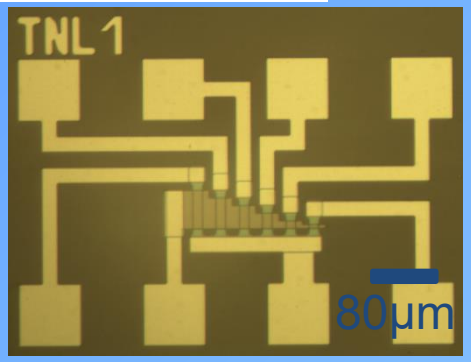
Nowadays at USP

Hands-on on Microelectronic Fabrication at University of Sao Paulo for educational application (SOI MOSFET Technology)

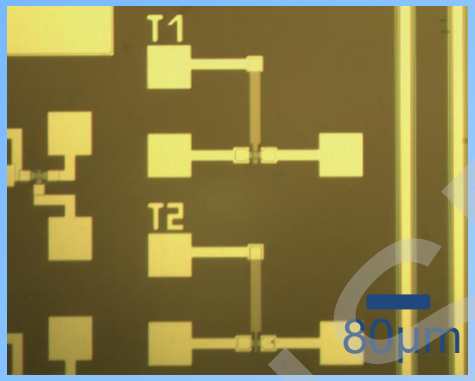
- Every year (40 hours)
- University of Sao Paulo, LSI/LME clean room
- For people from Brazilian community

University of Sao Paulo

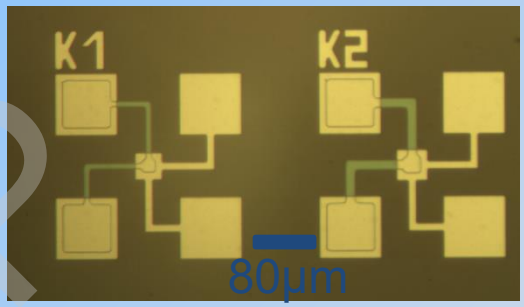
Fabrication Results



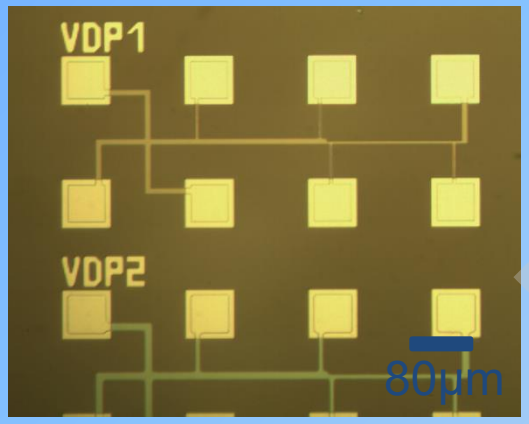
Picture of transistor array with W=12µm and L from 50 to 5µm.



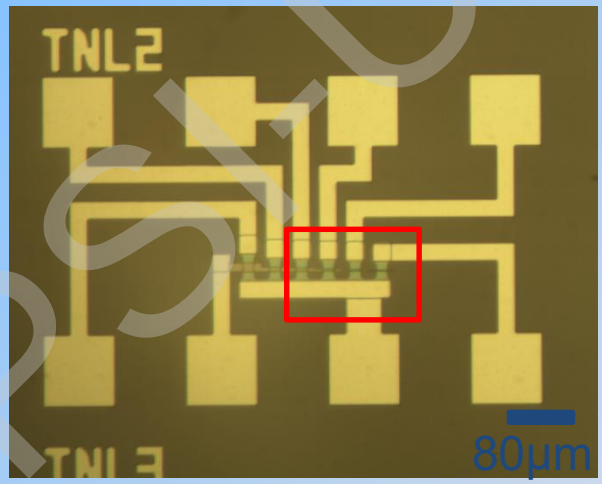
Picture of isolated transistors.



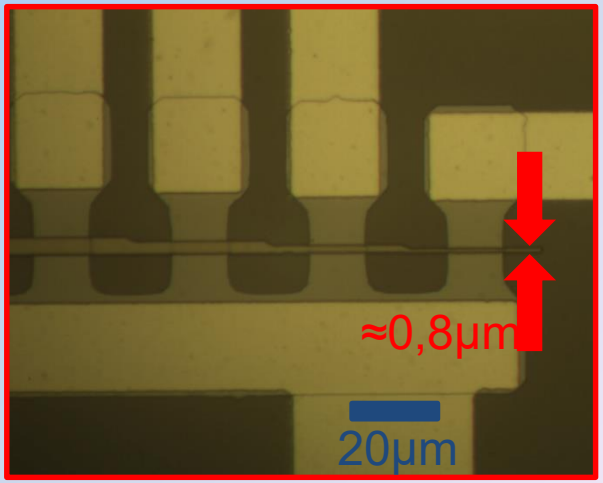
Kelvin Structures.



Van Der Pauw Structures.



Picture of transistor array with W=12µm and L from 10 to 1µm.



Detail of transistor array.

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Nowadays at USP

Hands-on on Electrical Characterization of Advanced Transistors at University of Sao Paulo (MOS, SOI, FinFET, TFET)

- Every year (40 hours)
- University of Sao Paulo, LSI/PSI/USP
- For people from Brazilian community

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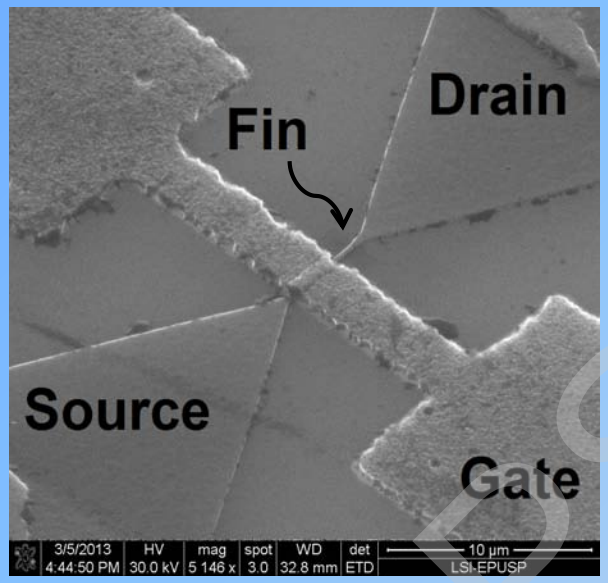
Nowadays at USP

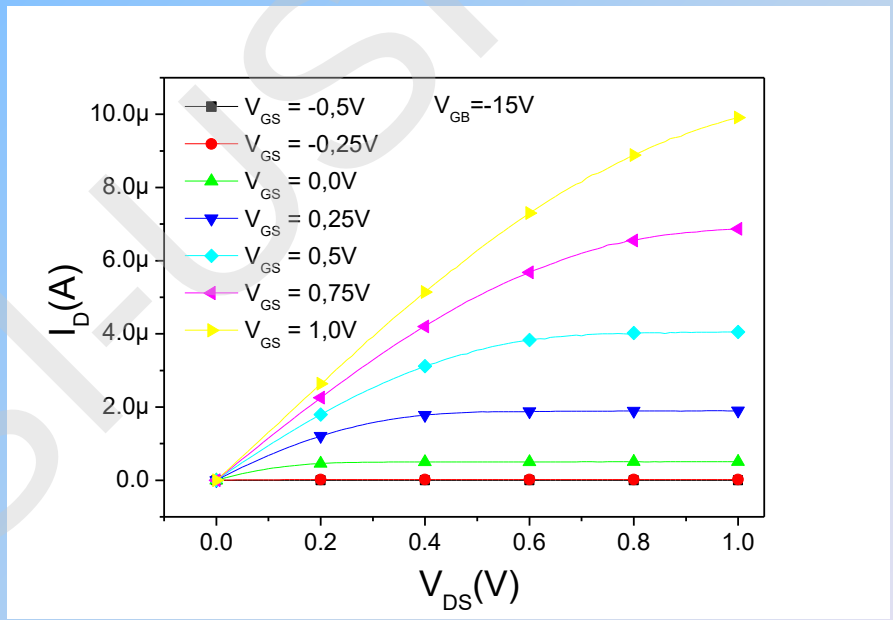
First FinFET Transistor (3D)

with Fully Electron-Beam-Lithography

Ebeam sample (USP): W_{FIN}= 100nm, H_{FIN}= 100nm, t_{ox}= 4.5nm, t_{box} = 200nm, L = 3.5μm; Gate electrode: Si-Poly; undoped channel.



FinFET view by scanning electron microscopy (SEM).



Channel cross-section layers obtained by FIB

* MARTINO, J. A, FAPESP Week, Salamanca, Spain, December,12, 2012

* RANGEL, R. ; POJAR, M.; SEABRA, A.C.; SANTOS Filho, S.G.; MARTINO, J. A, SBMicro 2013, Curitiba, Proc. IEEExplorer, p.1-5.

IC Brazil: Skilled labor force

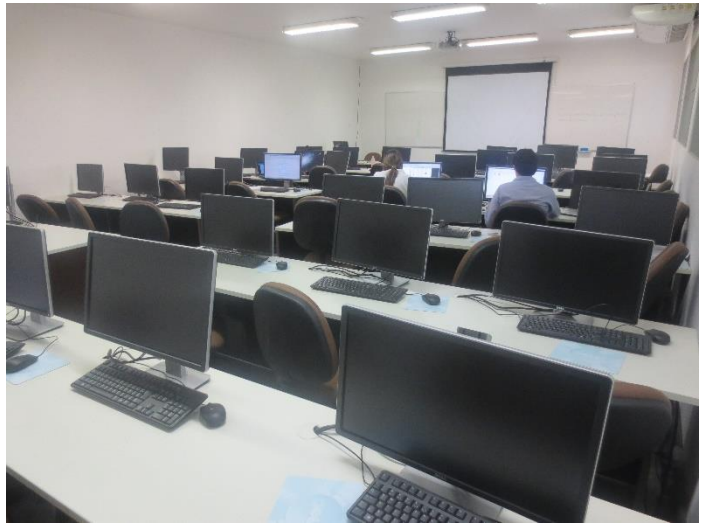
- 21 Fabless Companies in Brazil
  - Focus: design services & IP (Power Management, automotive audio, video, wireless, communications, etc)
  - All with outstanding technical capacity in several segments of the Semiconductor Industry
- 2 Silicon Plants (CEITEC , UNITEC)
- 2 Design Training Centers (USP, UFRGS):
  - 120 total seats capacity;
  - 1 year long training
  - Strong partnership
    - Cadence, Agilent – ADS & SystemVue, MunEDA, SMART, ARM…

Brazil IC – Design Training Center

- Development of the Brazilian Industry
  - Human resources
    - Training Center
    - International Industries partners

Mentor Graphics®
Agilent Technologies
SMART® Modular Technologies
ARM®
FAB MIXED-SIGNAL FOUNDRY EXPERTS
MunEDA
cadence™

IC Design Training Center at USP



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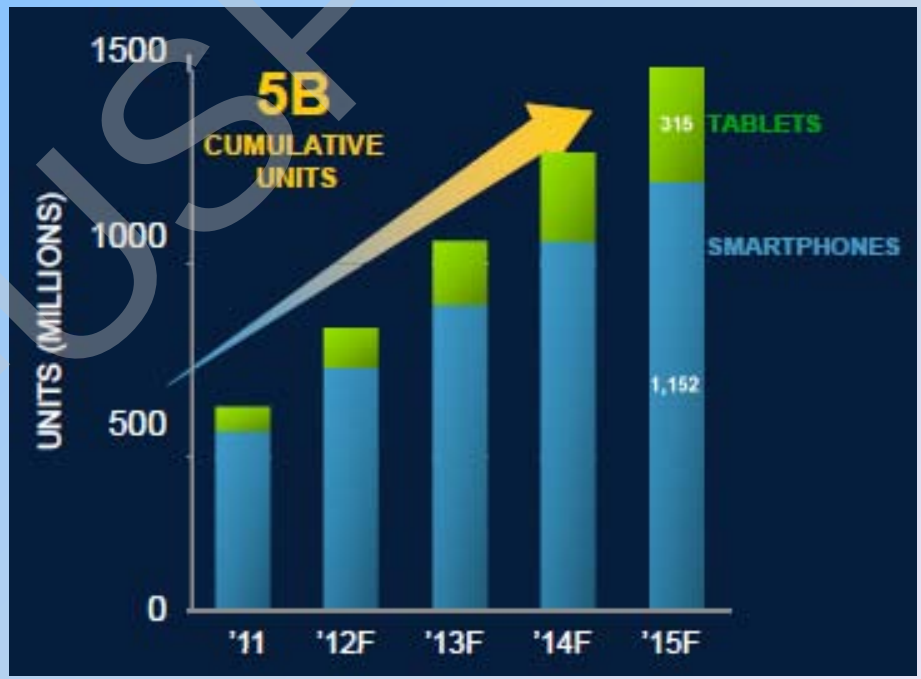
Micro and Nano-technology
Many applications



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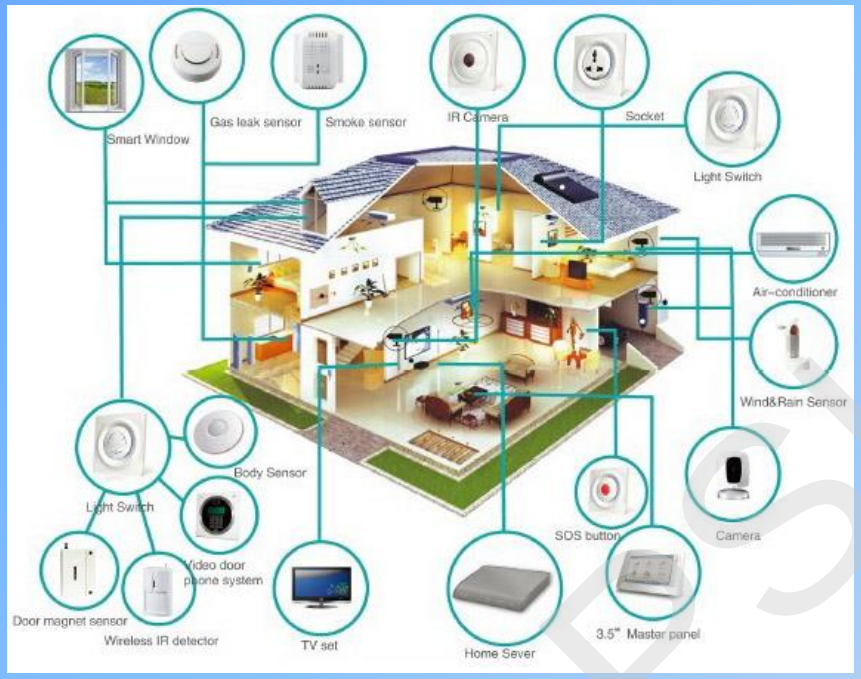
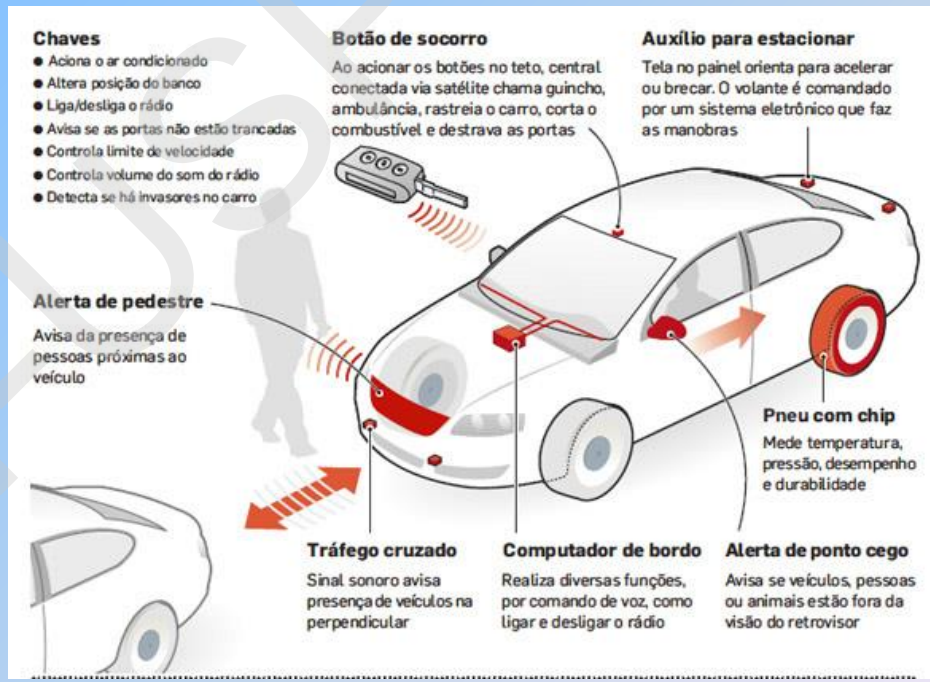
Micro and Nano-technology
Many applications

Smart house



Smart car



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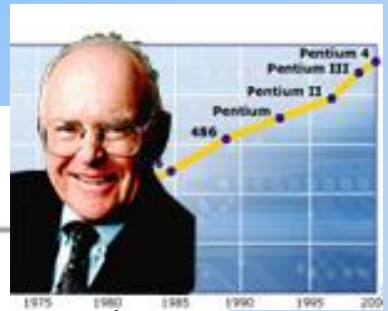
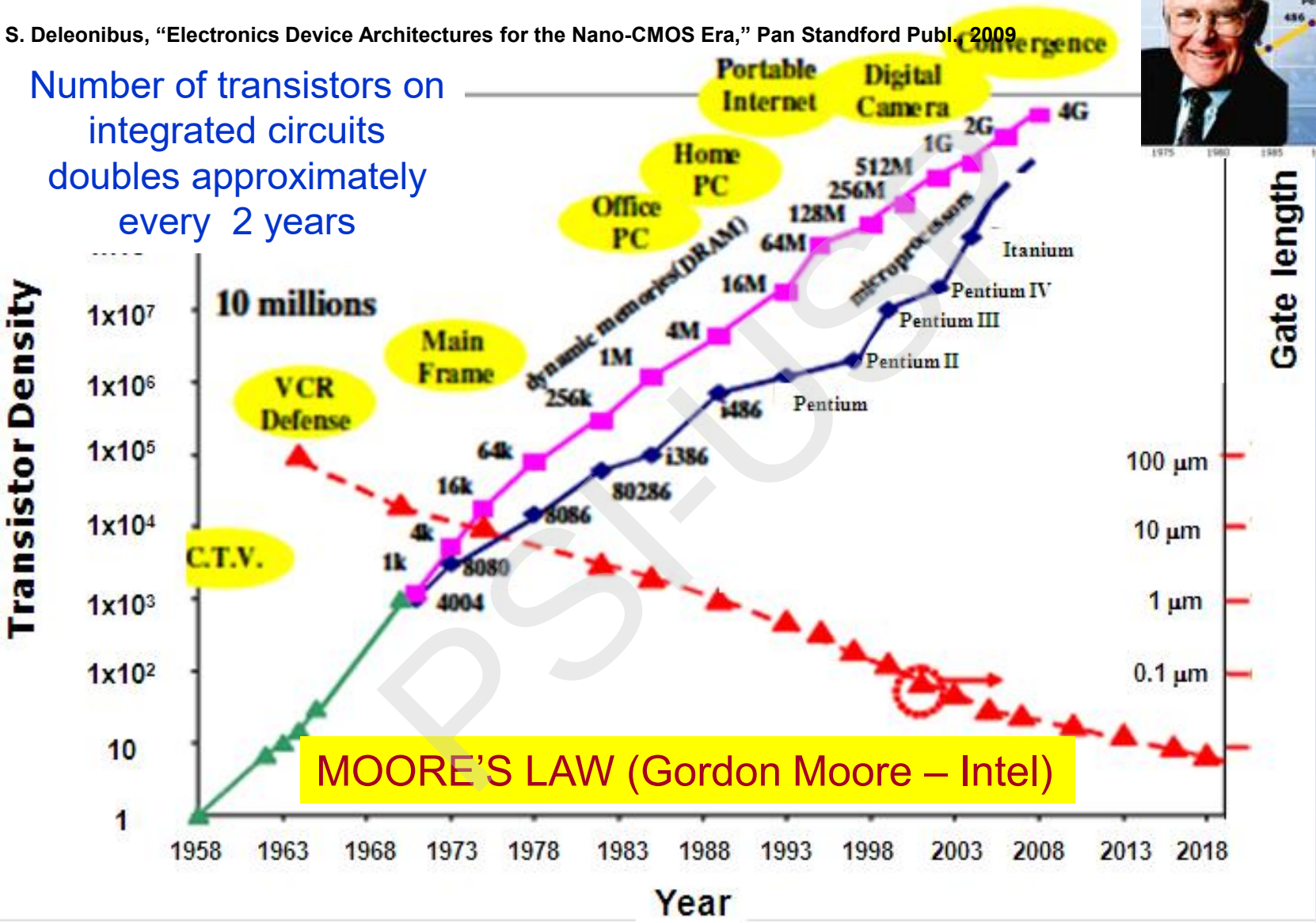
Keep increase of the number of components.

Cost per components decreases!



S. Deleonibus, "Electronics Device Architectures for the Nano-CMOS Era," Pan Standford Publ., 2009

Number of transistors on integrated circuits doubles approximately every 2 years



G.E. Moore, "Cramming more components onto integrated circuits," Electronics Mag., vol. 38, pp. 114-117, 1965.

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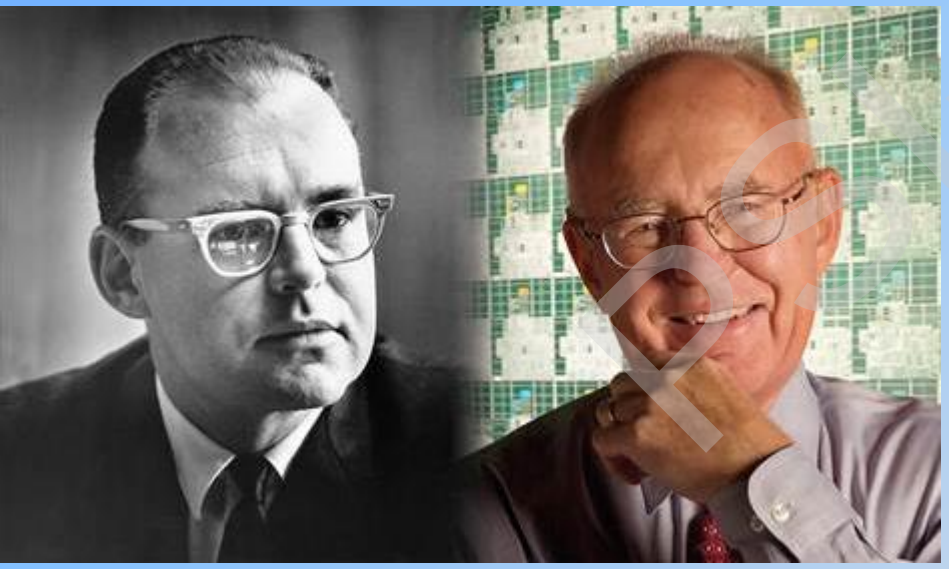
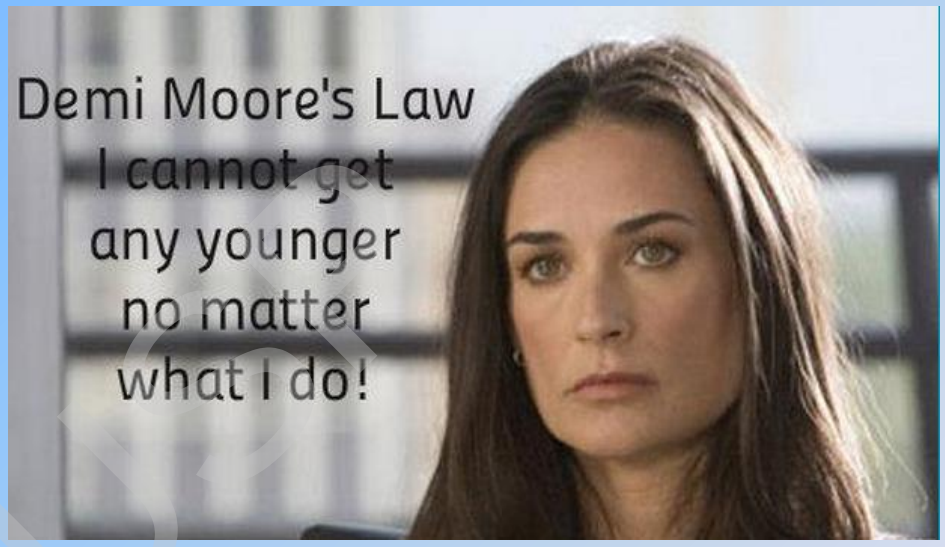
Moore`s Law 1965



Gordon Moore



Moore 1962

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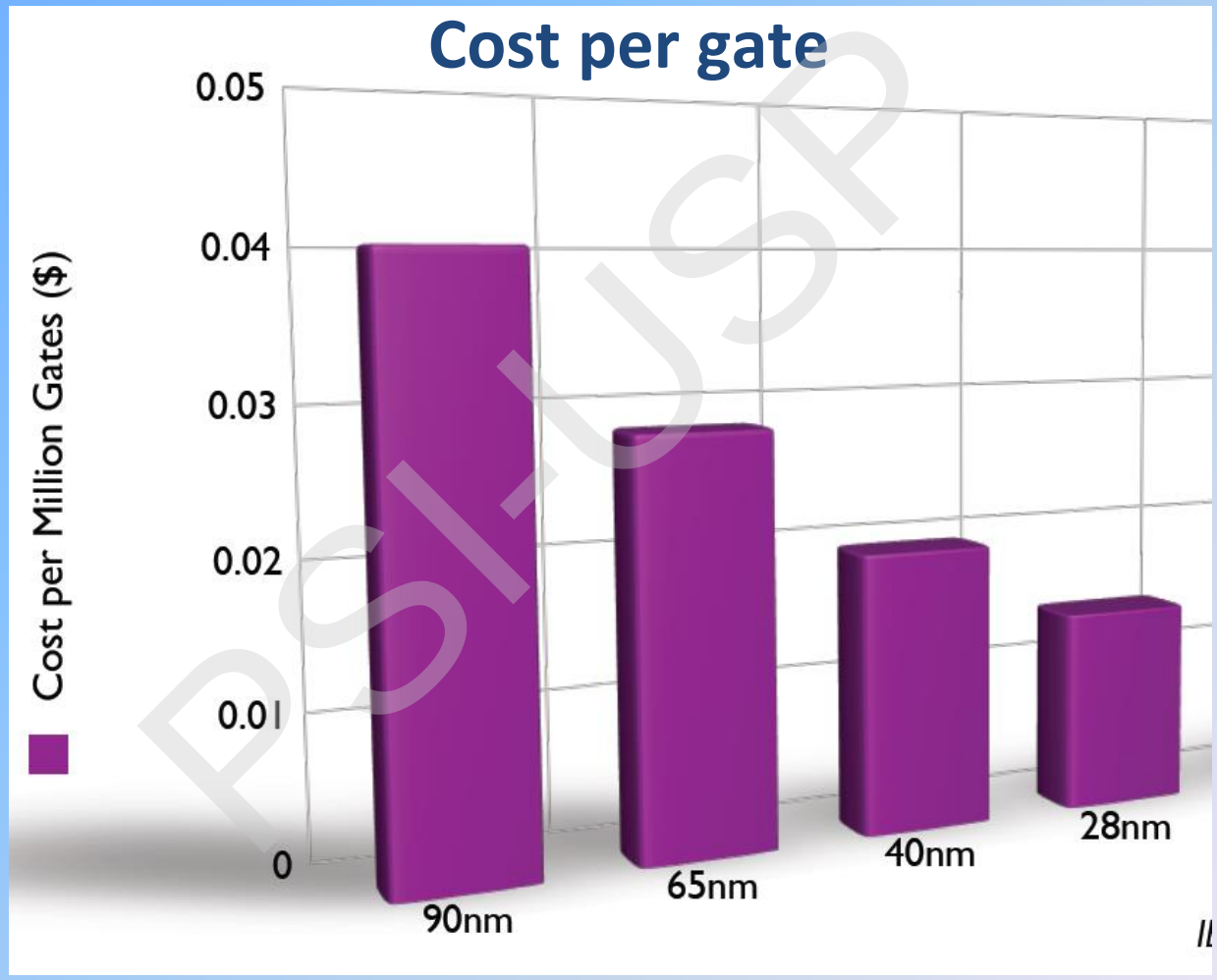
Micro- and Nano-technology Many applications



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First Patent of FET

Julius Edgar Lilienfeld (April 18, 1882 – August 28, 1963) was an Austro-Hungarian physicist. He was born in Lemberg in Austria-Hungary (now called Lviv in Ukraine), moved to the United States in the early 1920s, and became an American citizen in 1934. Lilienfeld is credited with the first patents on the field effect transistor (1925)

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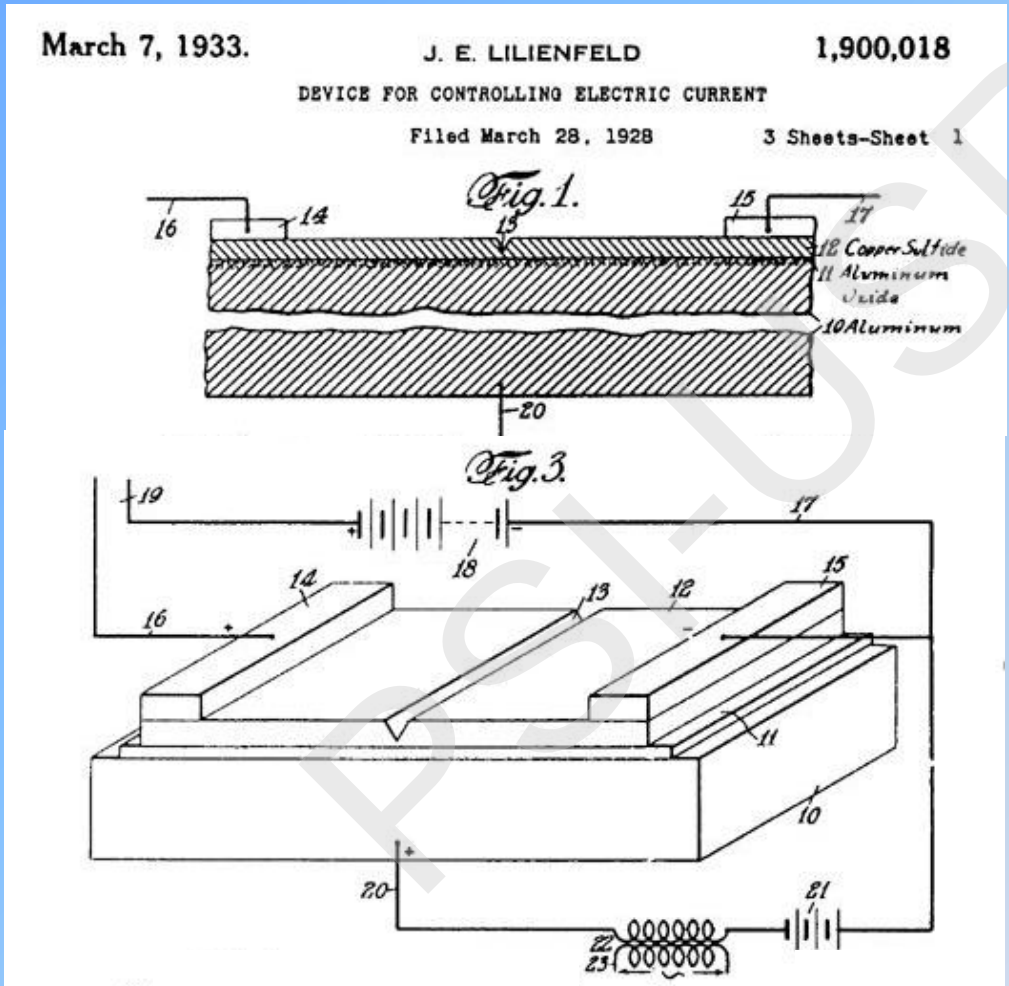
1925
First Patent of FET



J. E. Lilienfeld: "Method and apparatus for controlling electric current" US patent 1745175 first filed in Canada on 22nd October 1925

J. E. Lilienfeld: "Device for controlling electric current" US patent 1900018, filed on 28th March 1928

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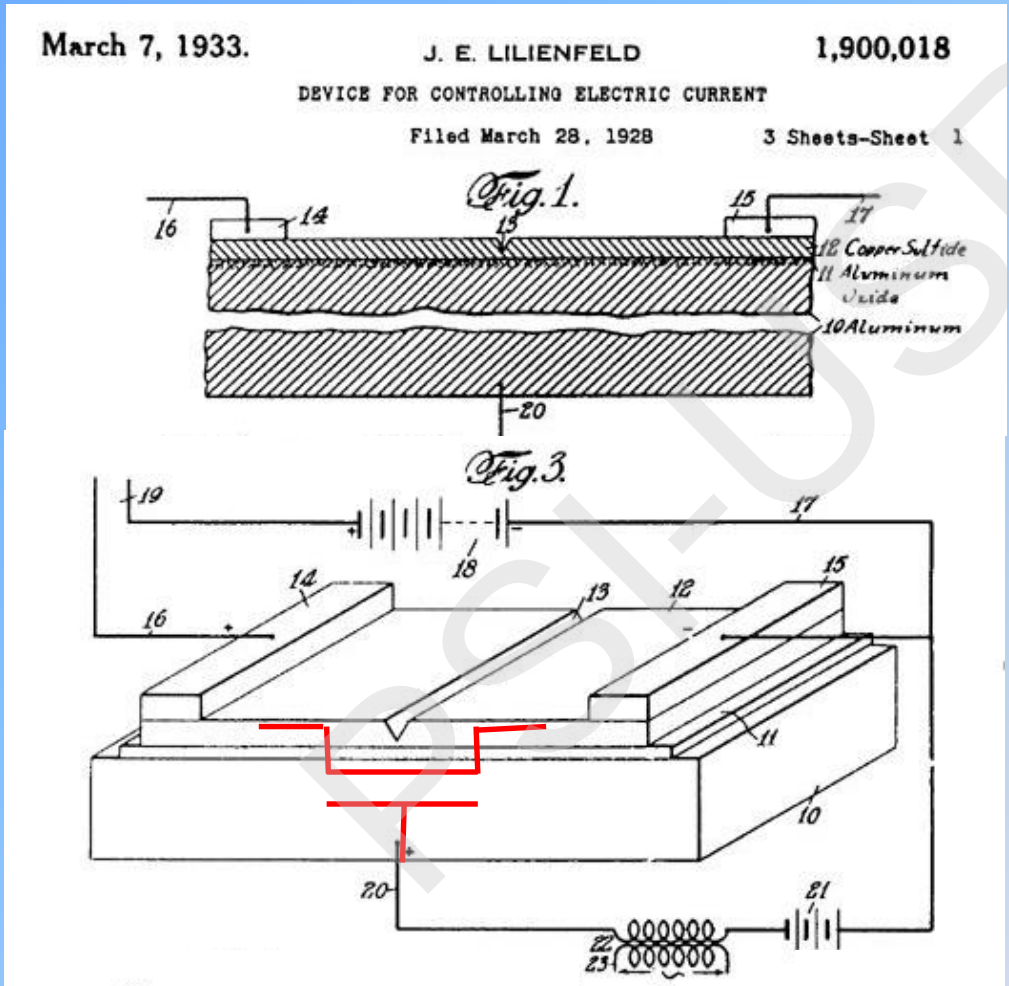
1925
First Patent of FET



J. E. Lilienfeld: "Method and apparatus for controlling electric current" US patent 1745175 first filed in Canada on 22nd October 1925

J. E. Lilienfeld: "Device for controlling electric current" US patent 1900018, filed on 28th March 1928

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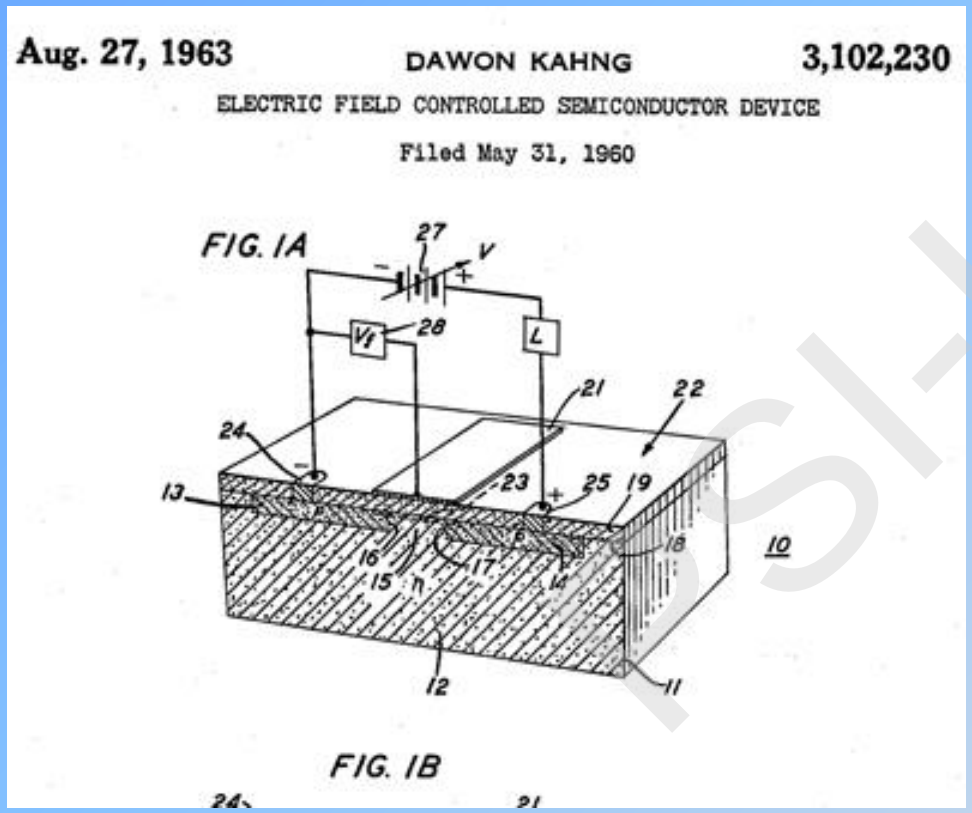
1960
First Demonstrated MOSFET

Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET)



Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

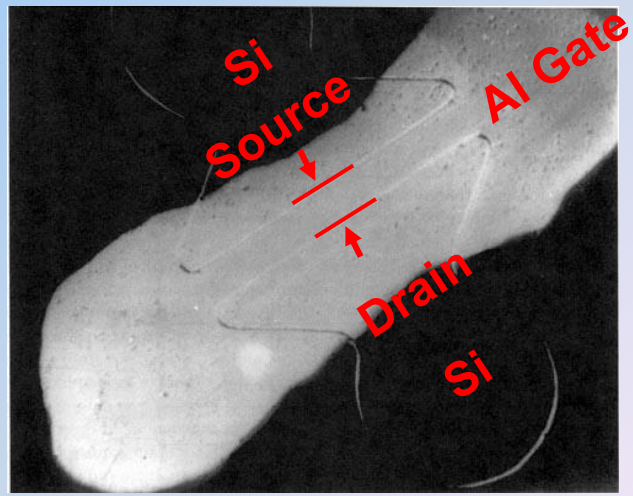
Filed May 31, 1960

FIG. 1A

FIG. 1B

M. M. (John) Atalla and Dawon Kahng at Bell Labs achieved the first successful insulated-gate field-effect transistor (MOSFET),

Top View



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The **MOSFET** (metal–oxide–semiconductor field-effect transistor) utilizes an insulator (typically SiO_2) between the gate and the body.

The **SOI MOSFET** is a Silicon-On Insulator MOSFET

The **FinFET** is a transistor fabricated around of a Fin

The **TFET** (tunnel field-effect transistor) is based on band-to-band tunneling

NMOSFET

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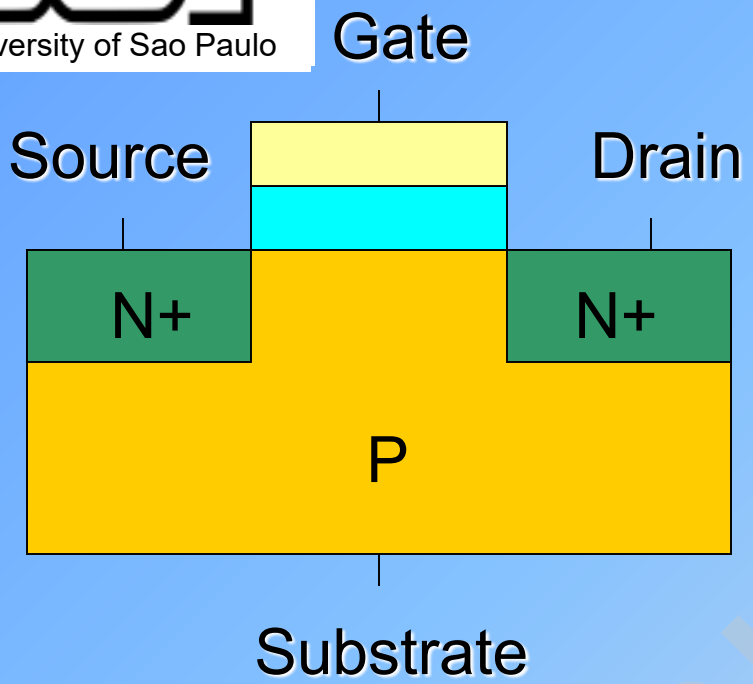
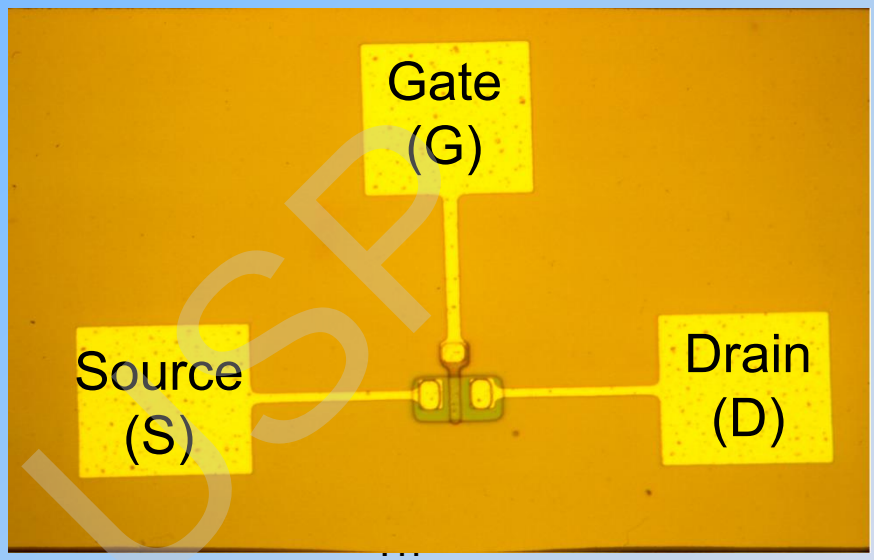
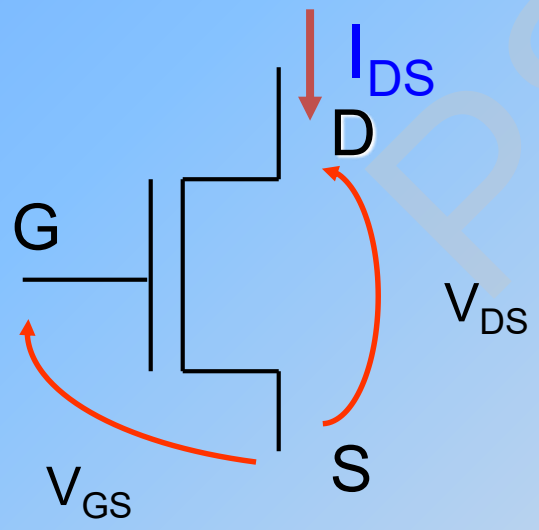
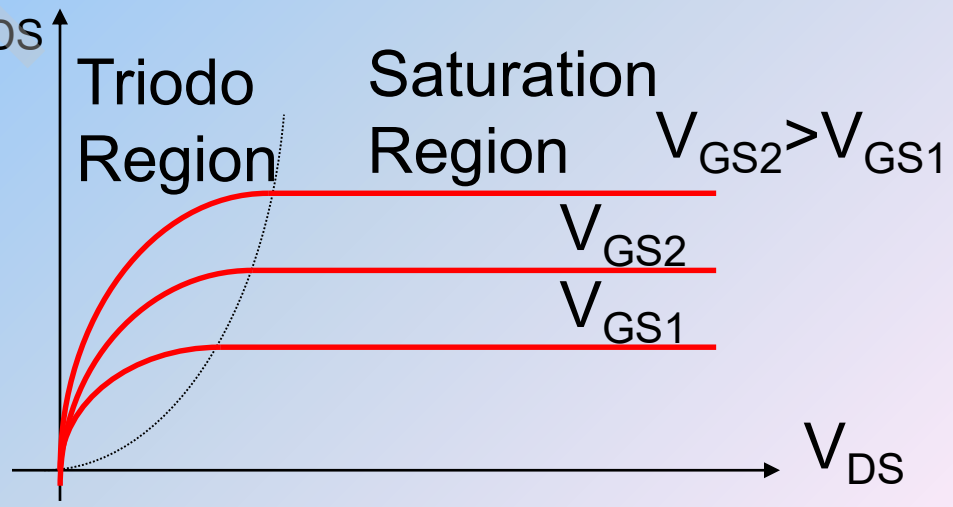




(USP/Brazil)





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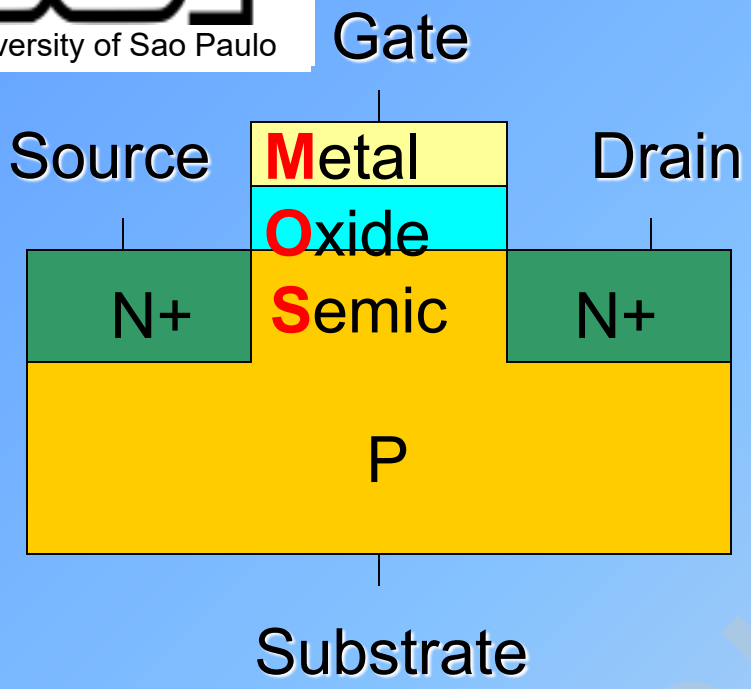
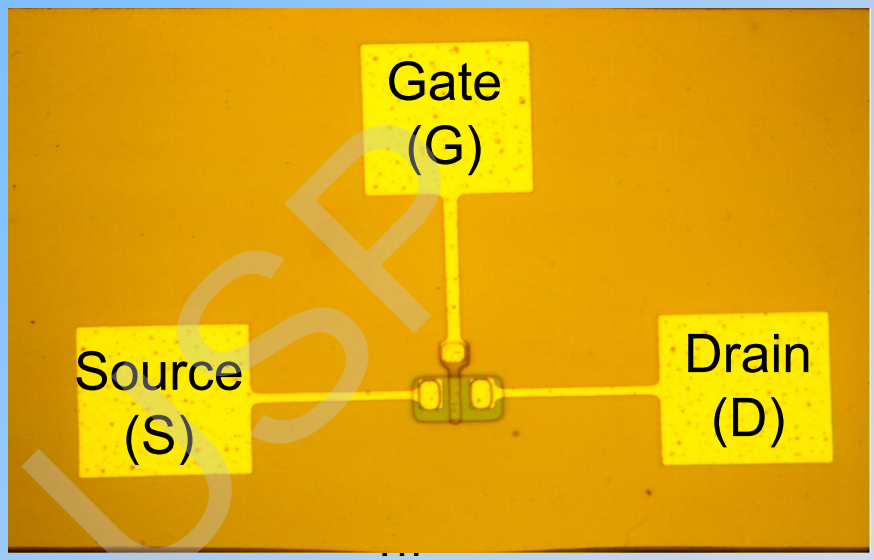
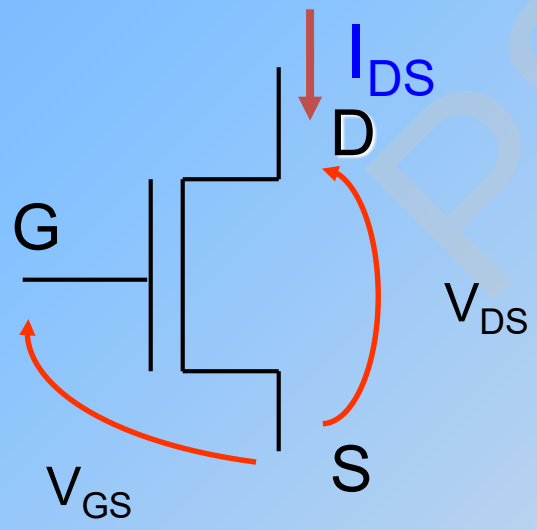
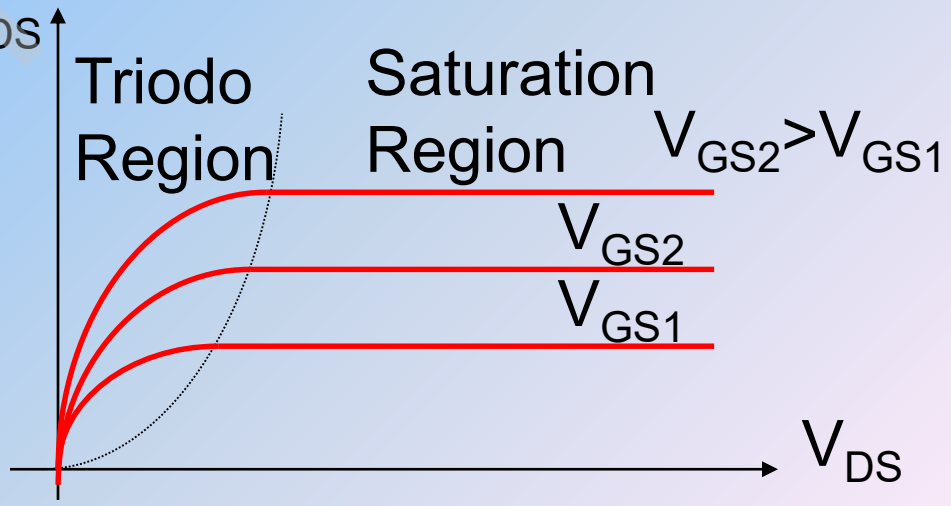
NMOSFET





(USP/Brazil)





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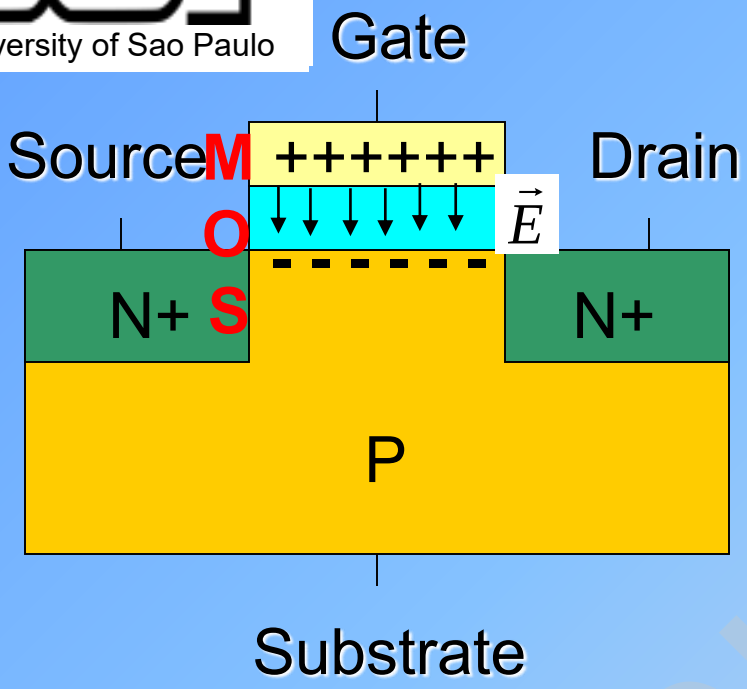
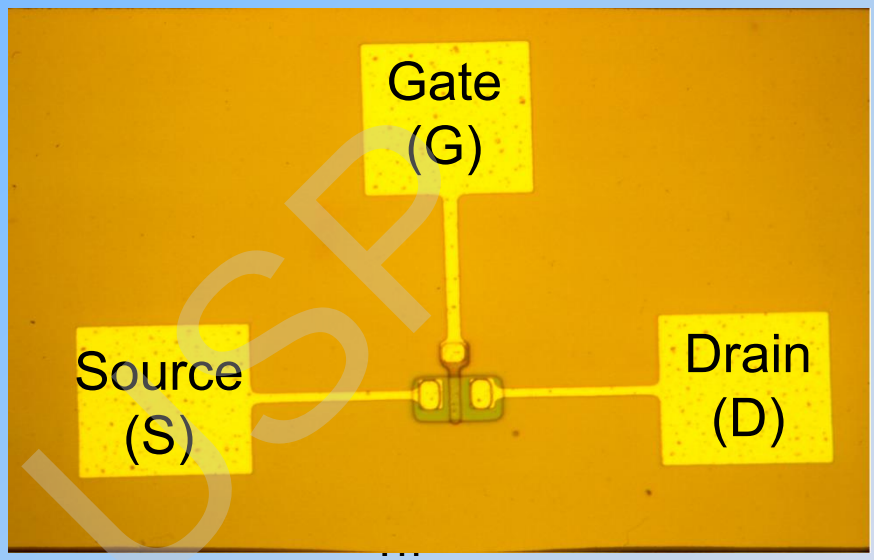
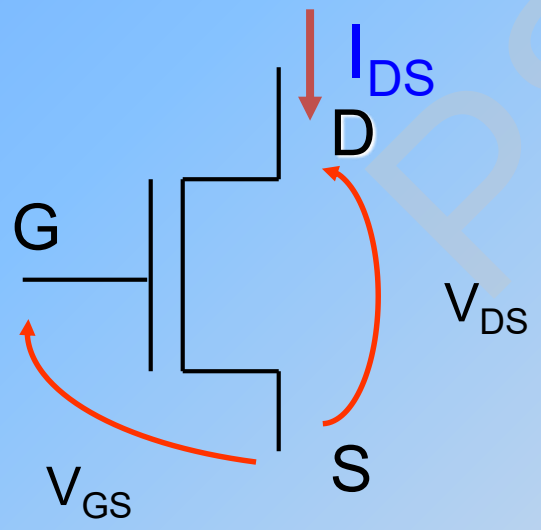
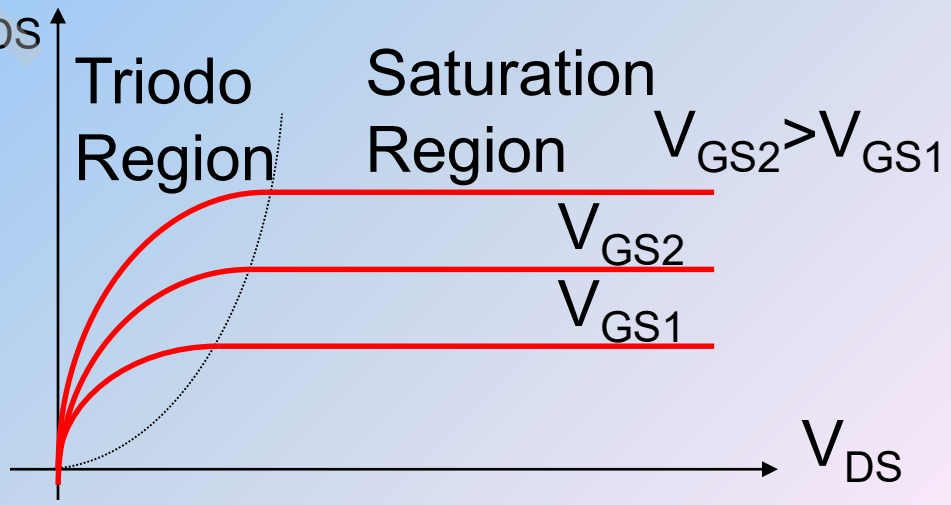
NMOSFET





(USP/Brazil)





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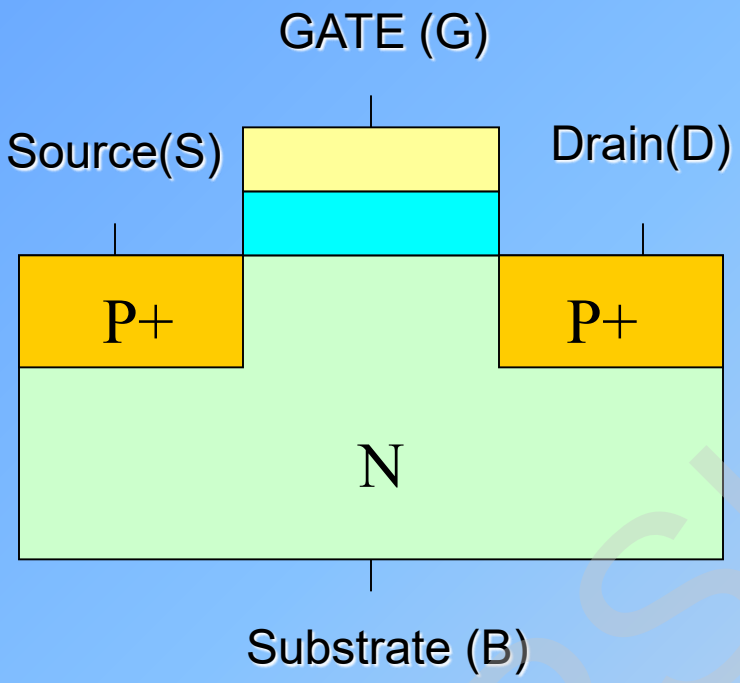
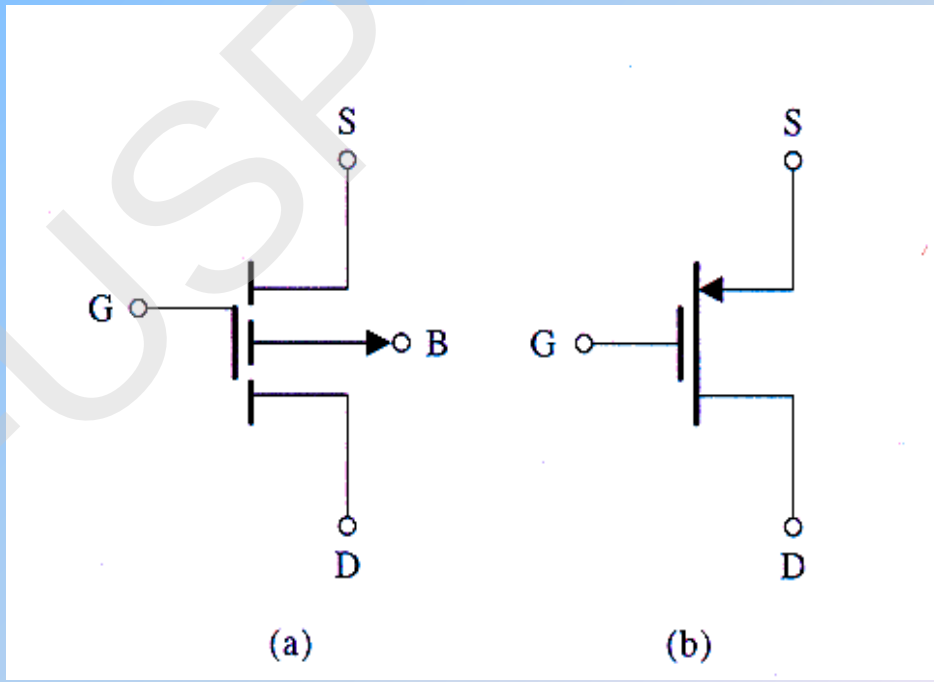
PMOSFET





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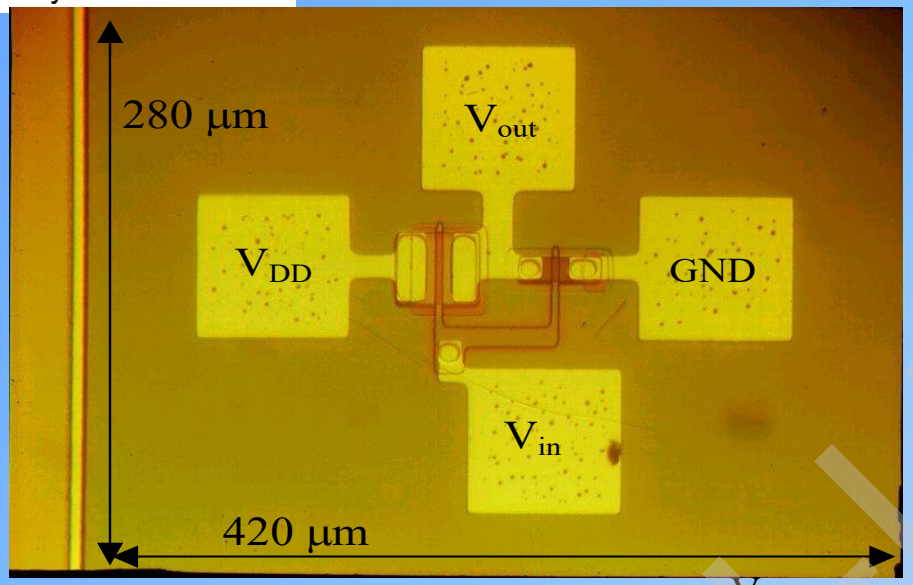
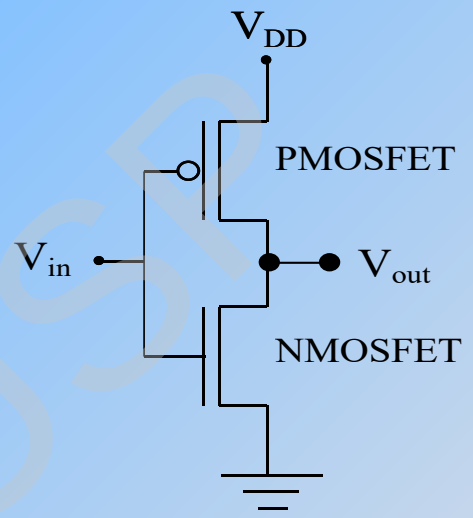
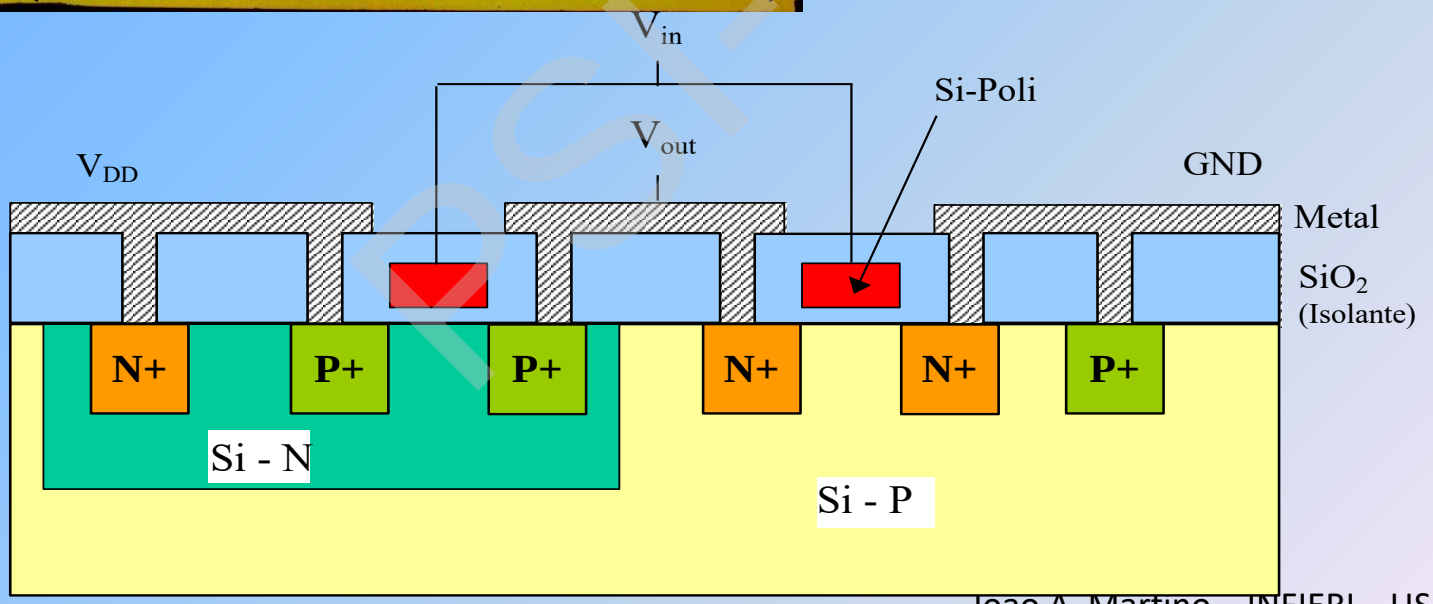
Inversor Lógico Digital CMOS







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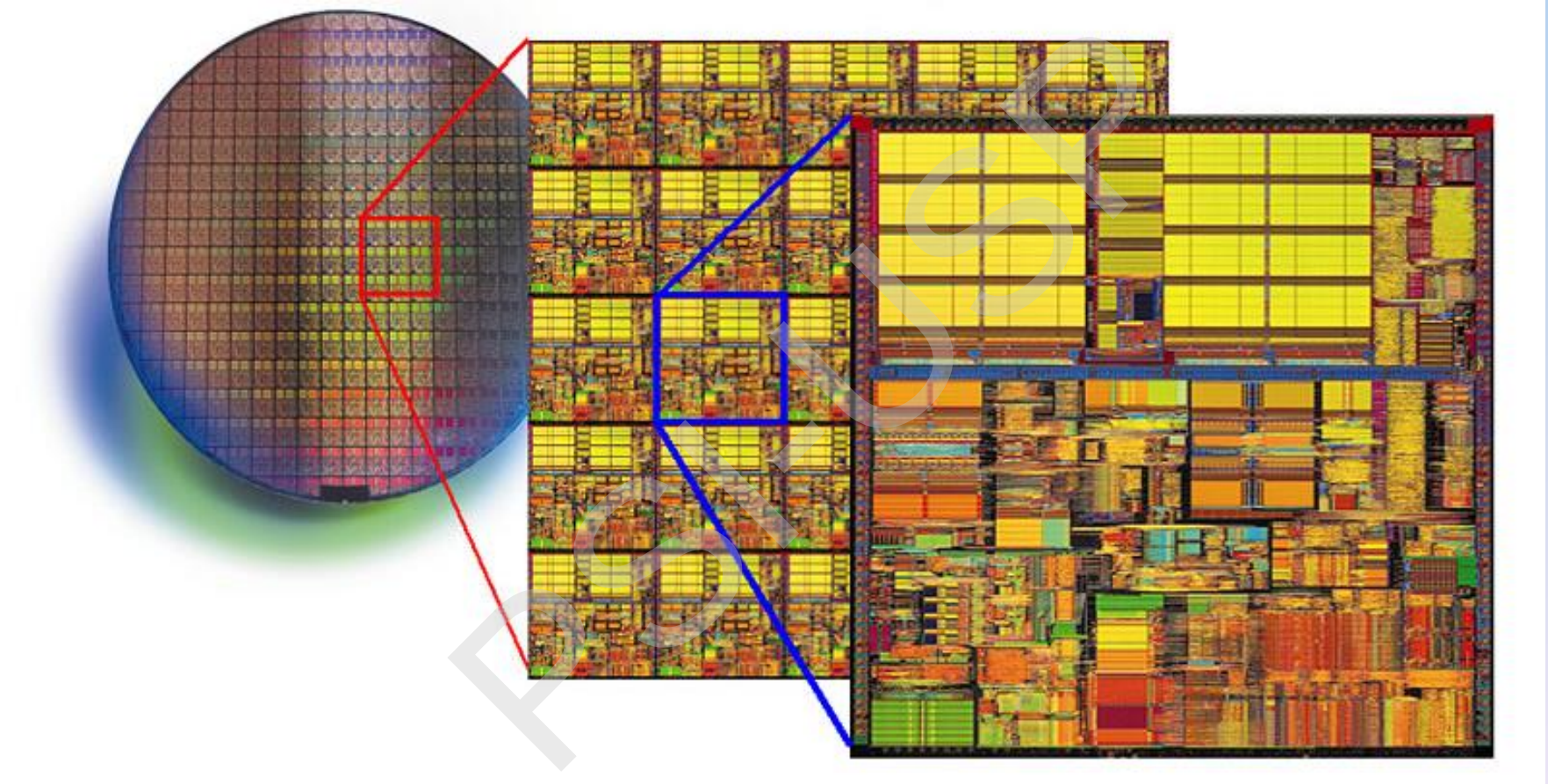

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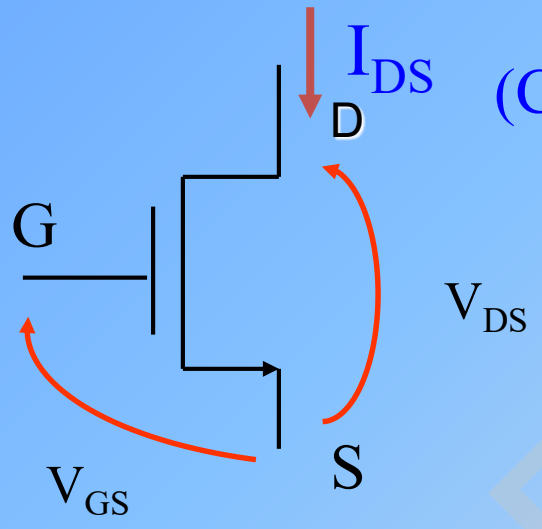
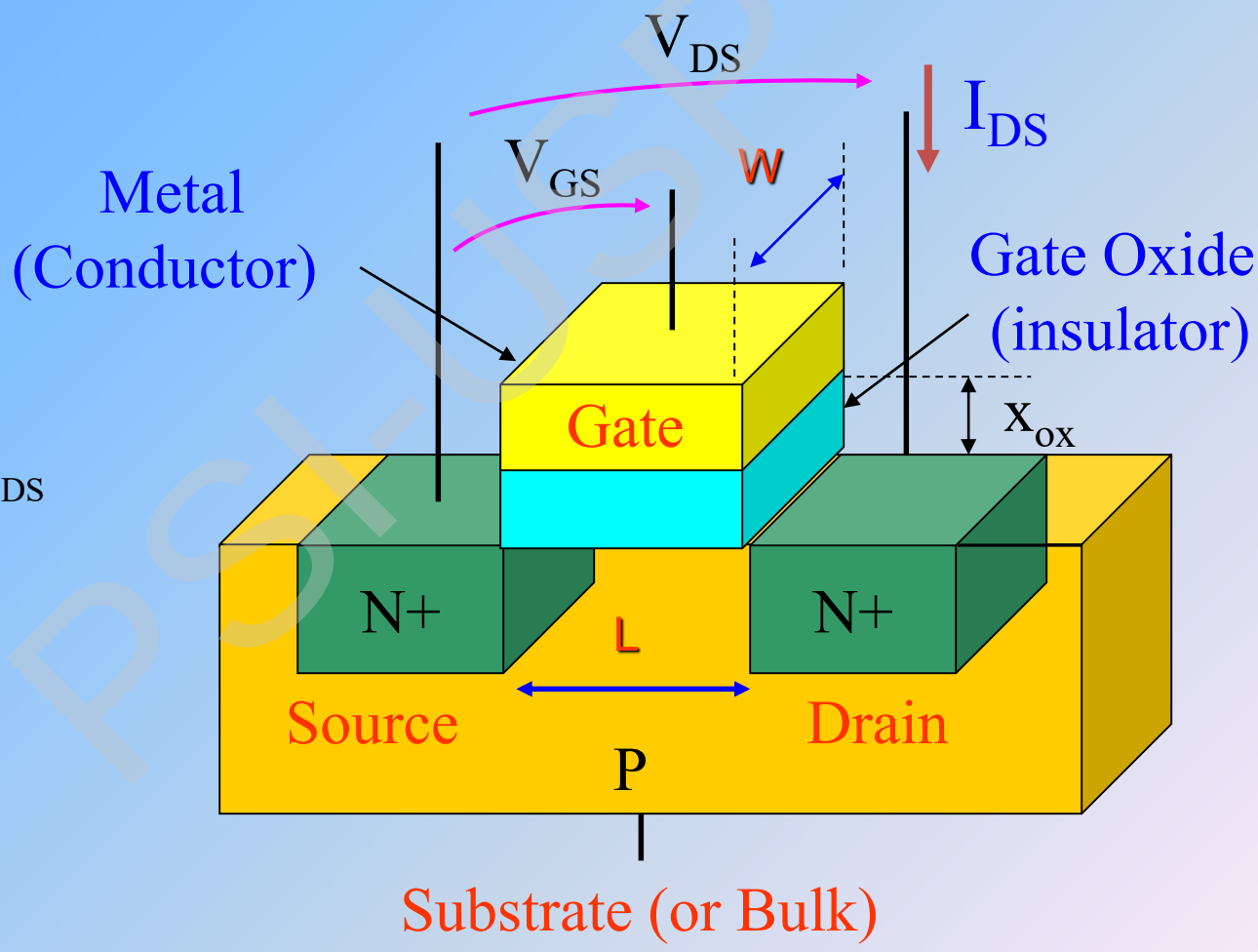
NMOSFET

(*Metal-Oxide-Semiconductor Field Effect Transistor*, canal N, Enhancement type)





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Keeping Pace with Moore's law

- Use of new materials (high-κ dielectrics, midgap metal gate, silicides, metals,…

- Use mobility enhancement (strained silicon, SiGe, Ge,…

- Modify MOSFET structure to improve electrostatics: Bulk→SOI→Multigate (FinFET…)

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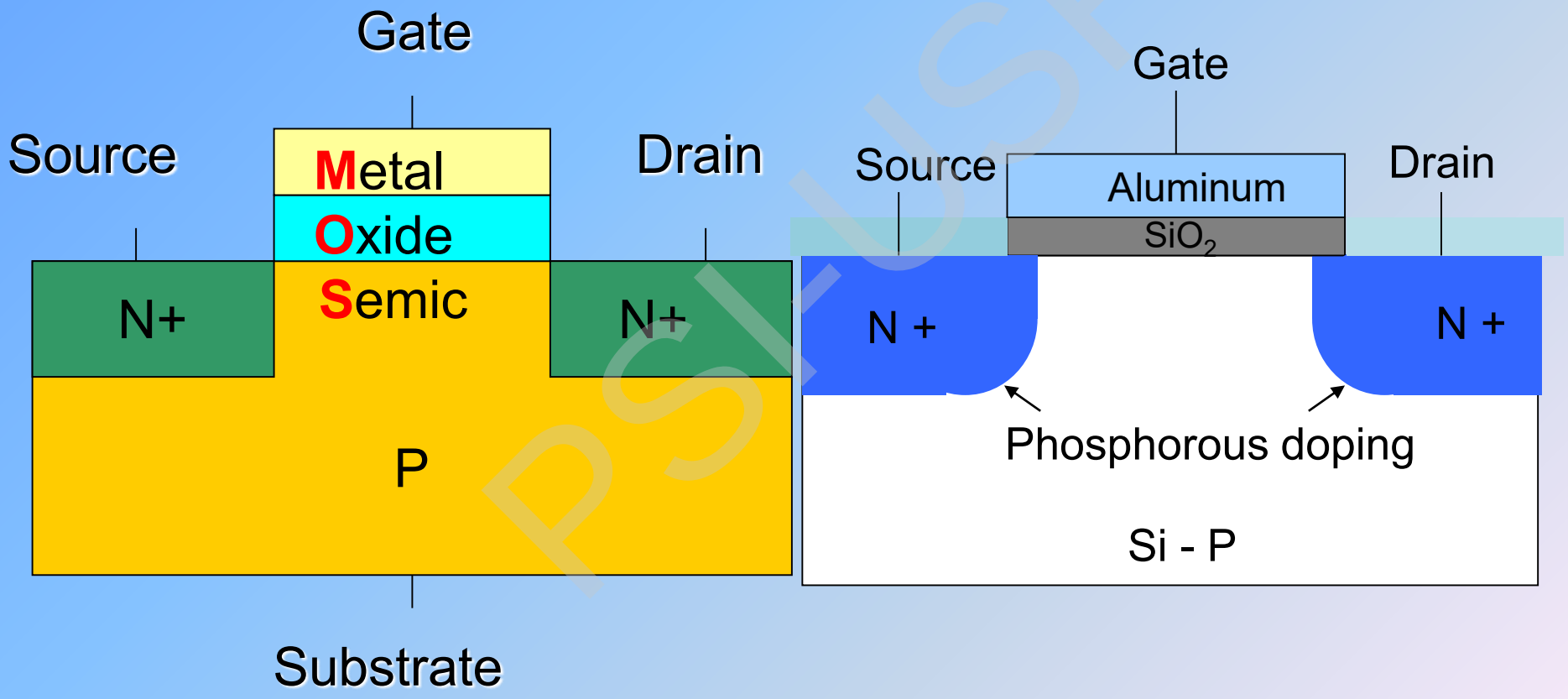
MOSFET
First Generation [~60]



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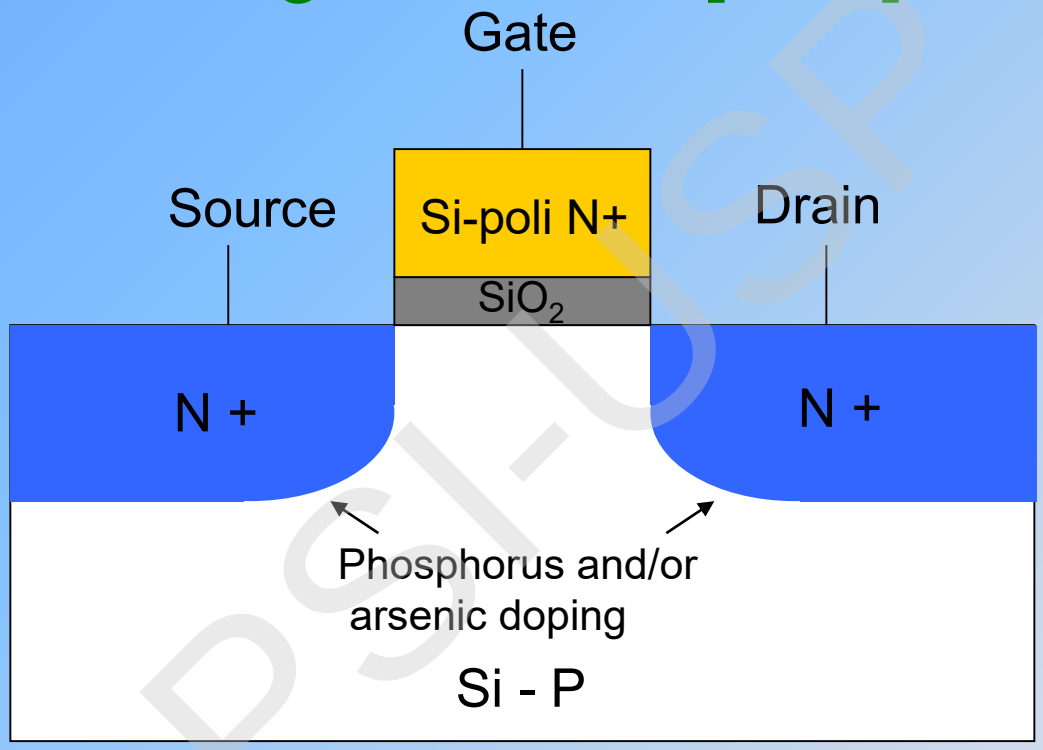
MOSFET
2nd generation [70's]



* Self-aligned : between gate and (source/drain) – lower parasitic capacitance;

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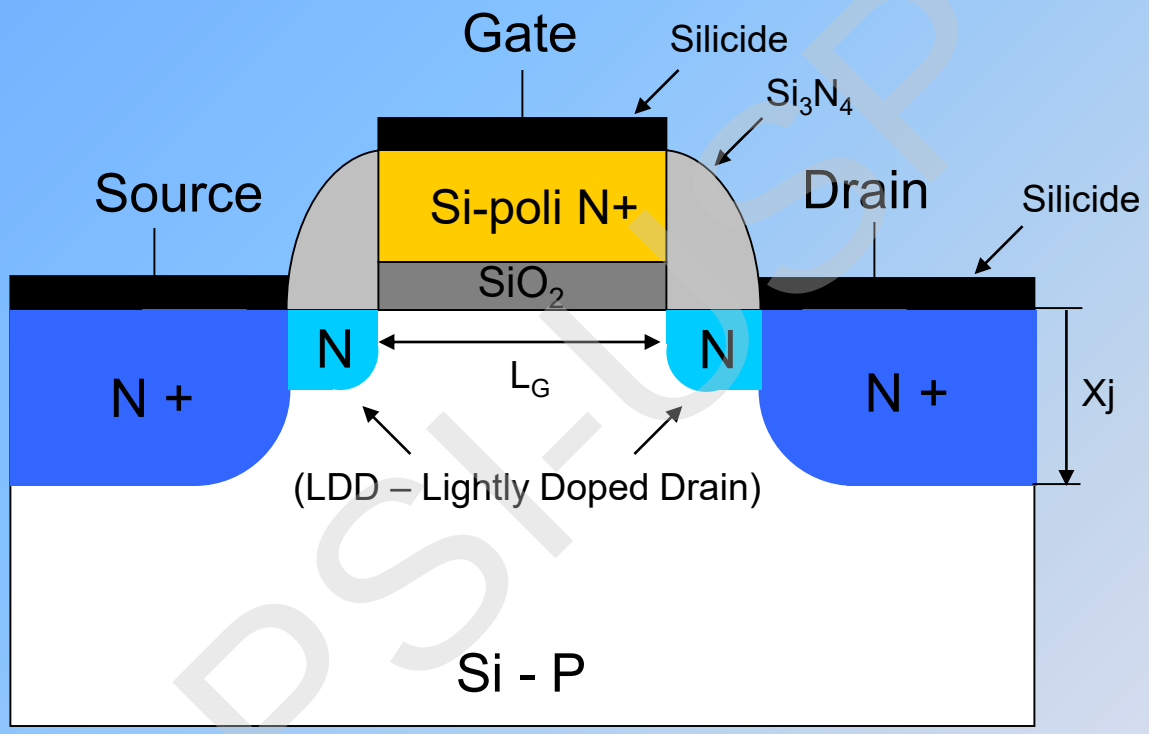
MOSFET
3rd generation [80's]



* LDD: Lower longitudinal electric field
* Silicide: Lower gate and source/drain series resistance

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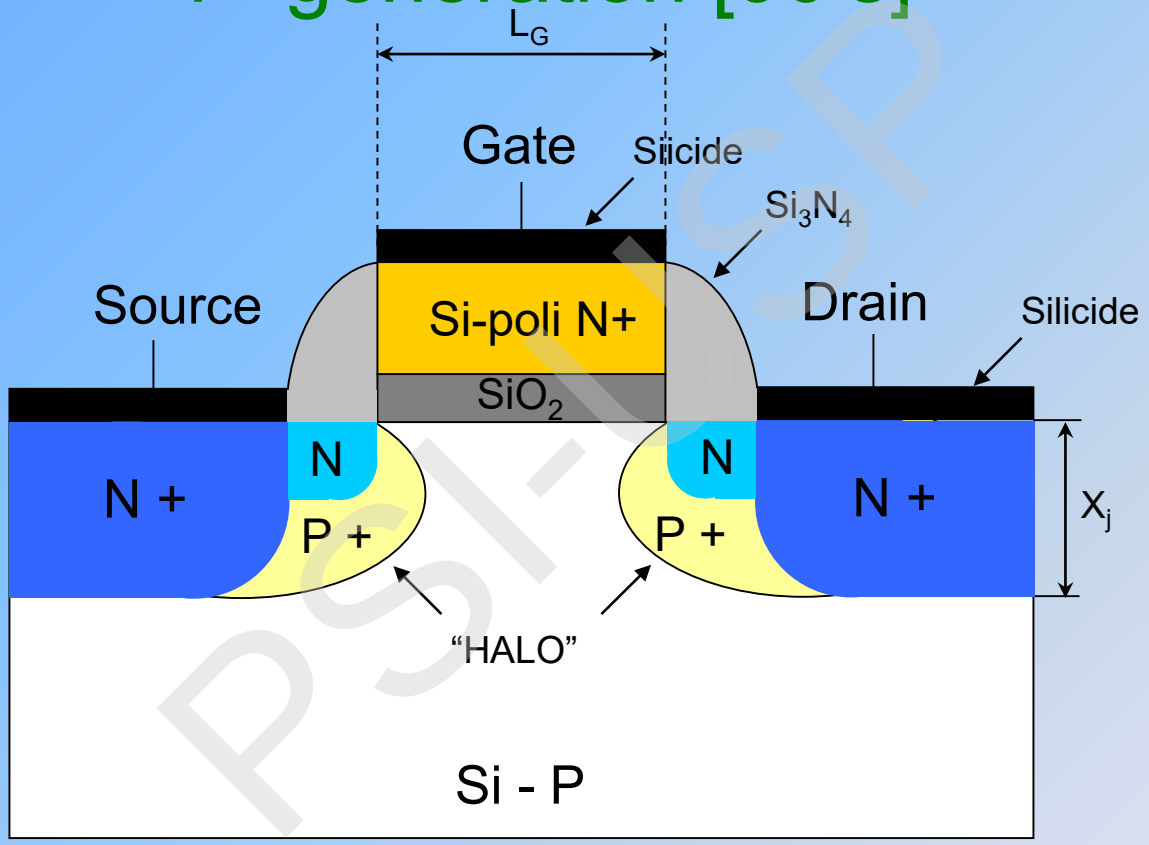
MOSFET
4th generation [90's]



* HALO: Better control of Short Channel Effect (SCE)

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Scaling roadmap

Ge/III-V, VFET, TFET, NW, Graphene…

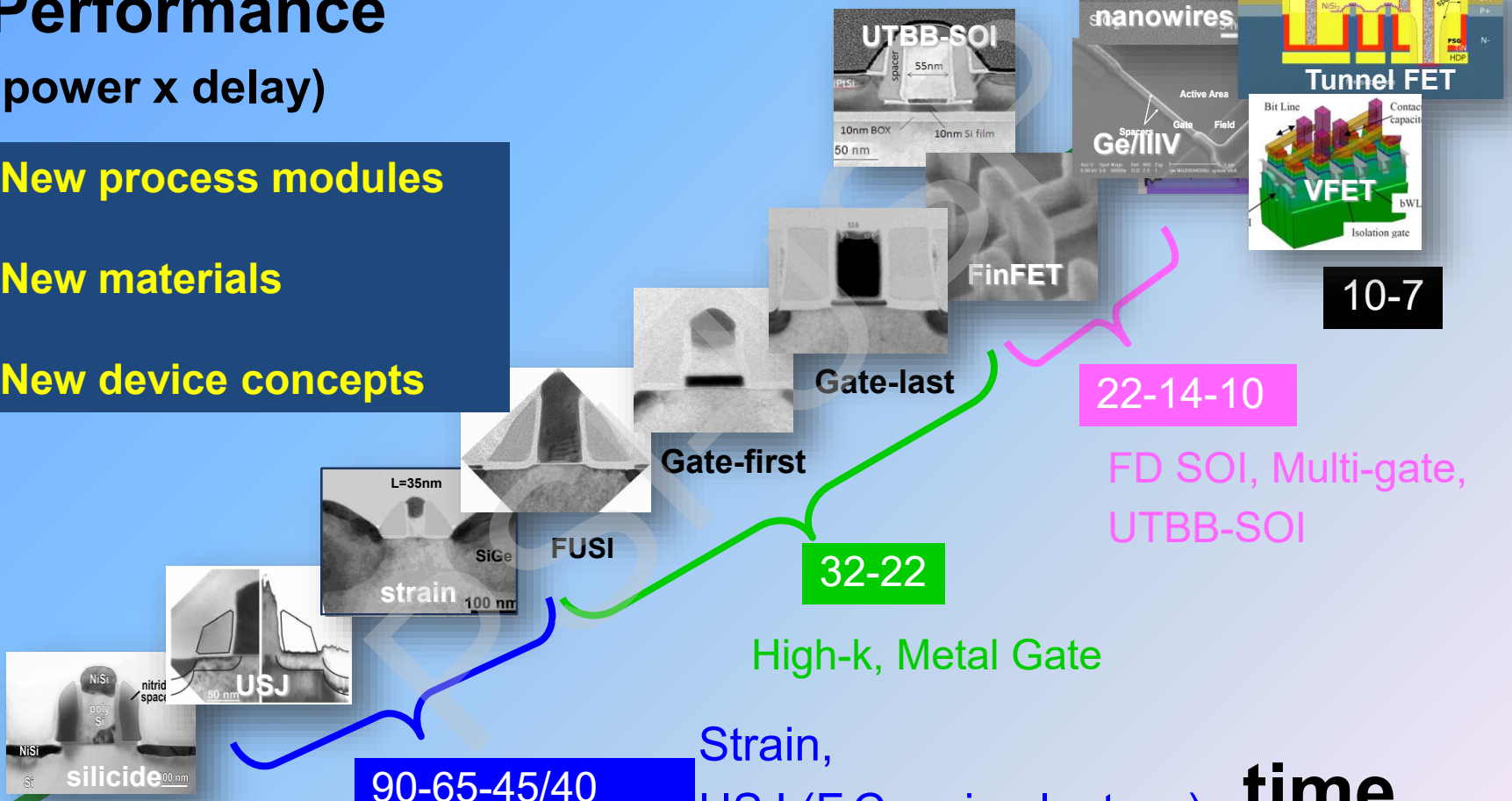
Performance

(power x delay)

New process modules

New materials

New device concepts



* By Cor Claeys

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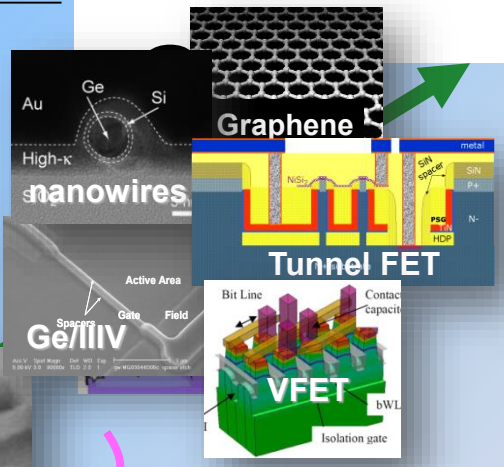
Scaling roadmap

Ge/III-V, VFET, TFET, NW, Graphene…



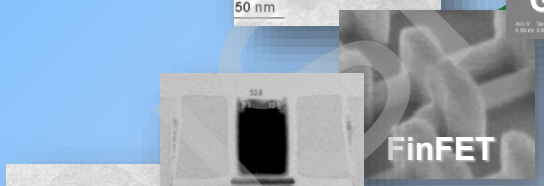
Performance

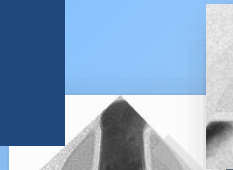
(power x delay)

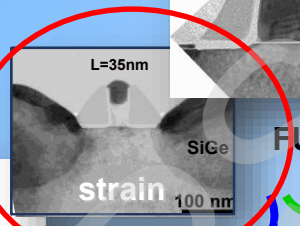
New process modules

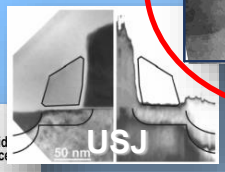
New materials

New device concepts









10-7

22-14-10

FD SOI, Multi-gate, UTBB-SOI

32-22

High-k, Metal Gate

90-65-45/40

Strain, USJ (F,C co-implant, …)

>130

time

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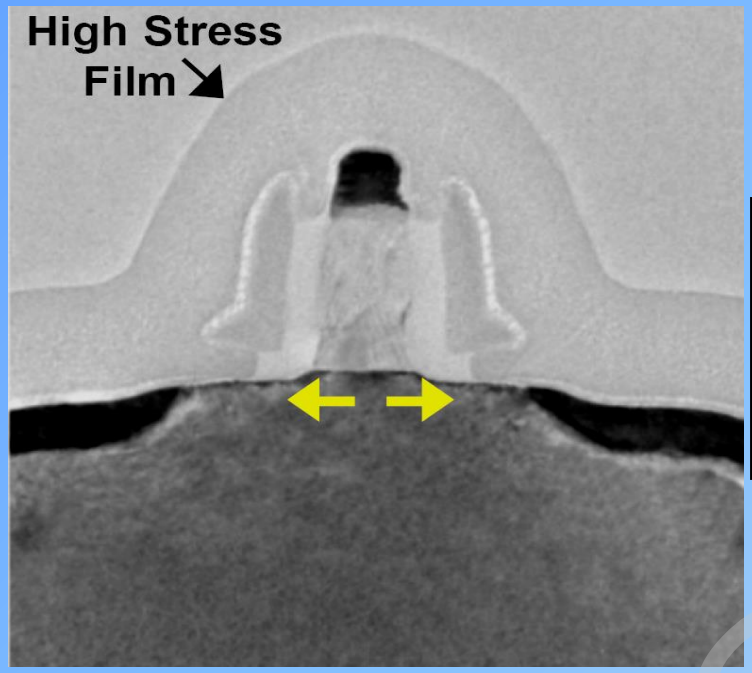
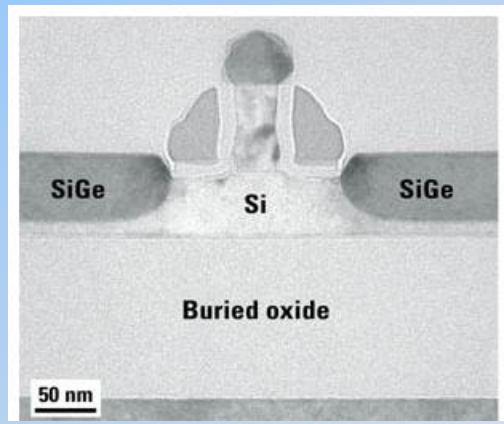
Strain Technology



on Bulk (Intel)

A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors

T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann*, K. Johnson#, C. Kenyon, J. Klaus, B.McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson and M. Bohr
IEDM 2003, p. 978



on SOI (Freescale+ASM)

http://www.reed-electronics.com/semiconductor/article/CA507185#fig4

nMOS: tensile channel strain

In order to boost the carrier mobility (hence the drive current) and improve the device performance uniaxial and biaxial strains are being successfully used

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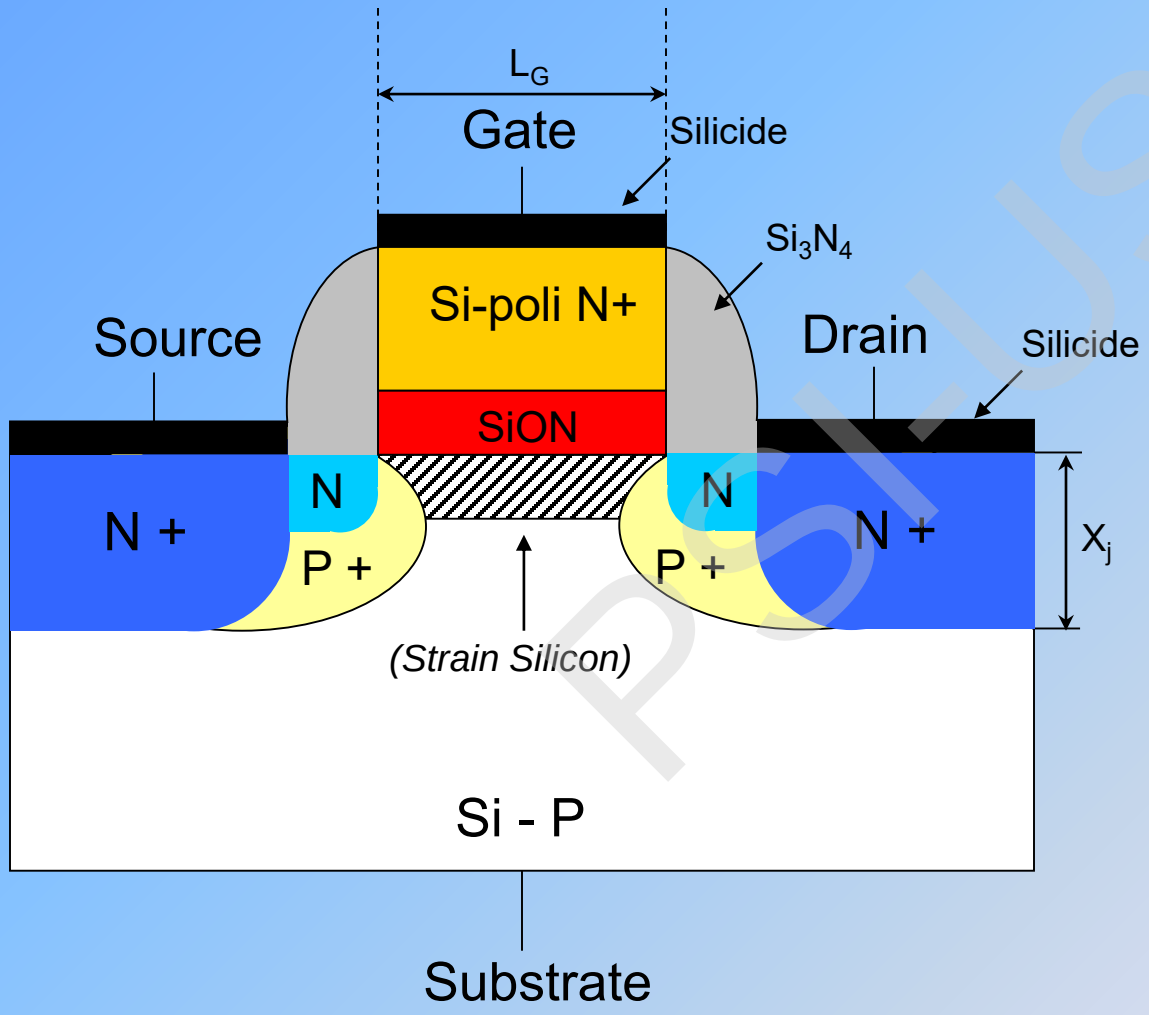
MOSFET
5th generation [end of ~90]



* Strained silicon: Improvement of carrier's mobility

* SiON : Reduces the gate leakage current

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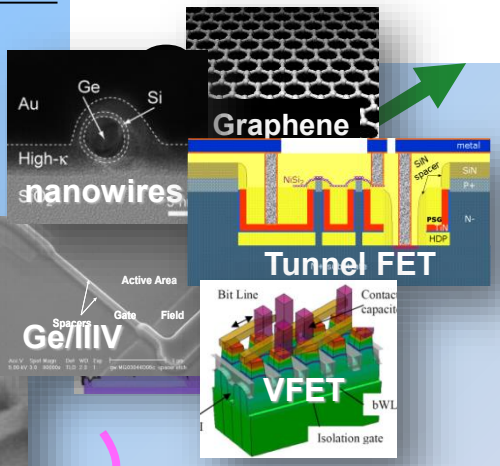
Scaling roadmap

Ge/III-V, VFET, TFET, NW, Graphene…



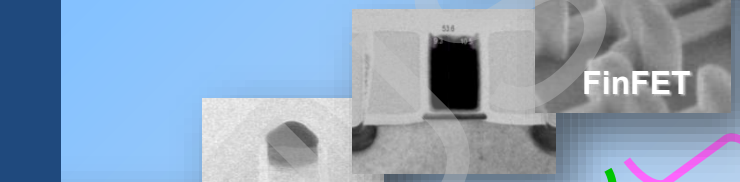
Performance

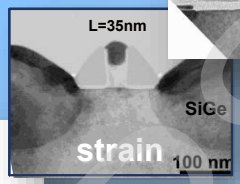
(power x delay)

New process modules

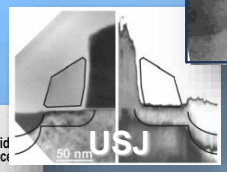
New materials

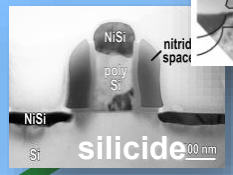
New device concepts





FUSI





10-7

22-14-10

FD SOI, Multi-gate, UTBB-SOI

32-22

High-k, Metal Gate

90-65-45/40

Strain, USJ (F,C co-implant, …)

>130

time

* By Cor Claeys

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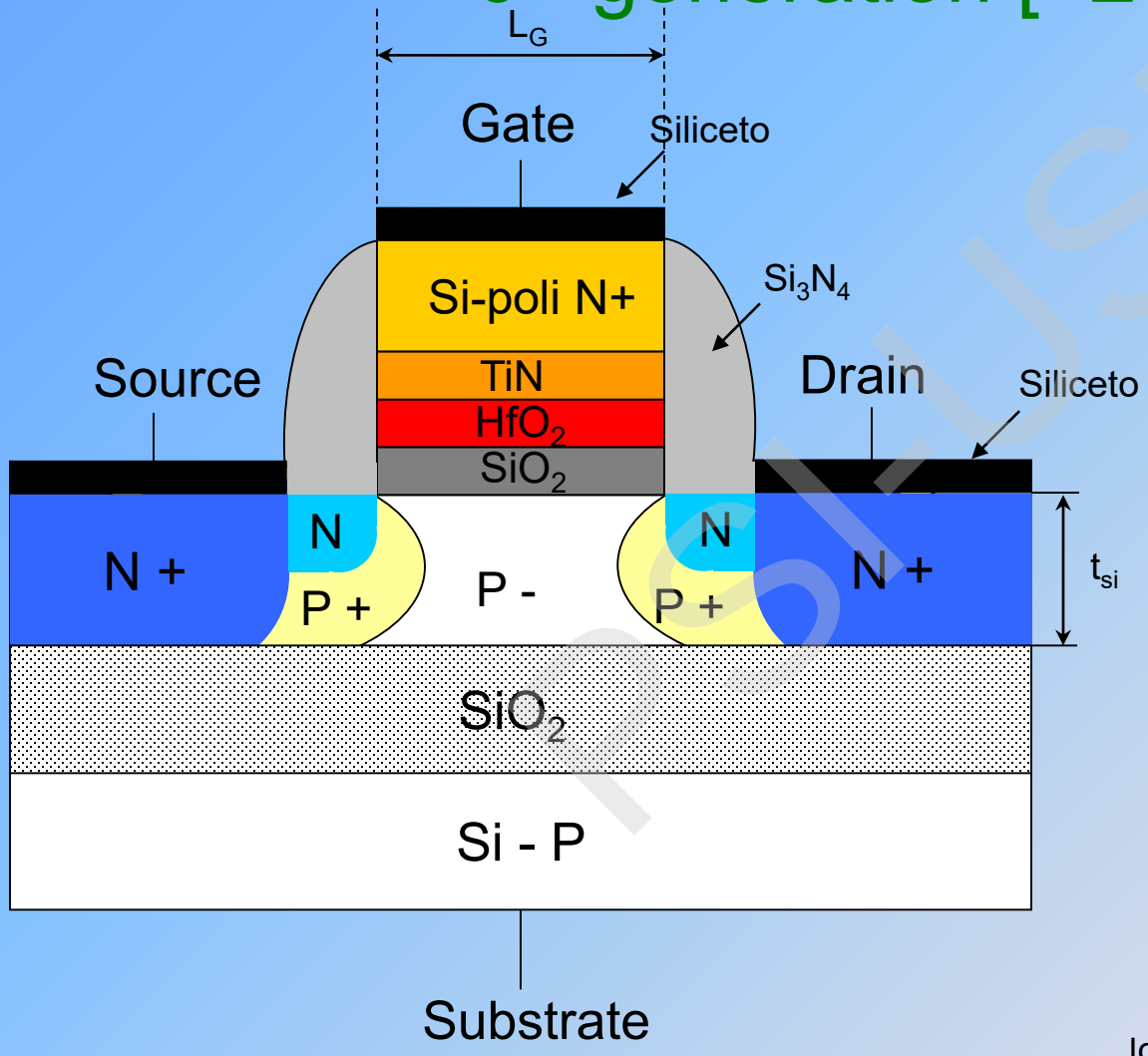
MOSFET
6th generation [~2000]



* SiO_2/HfO_2 (HK): Reduces gate leakage

* TiN (Metal Gate): Avoid the Poly-Si depletion

•SOI: Silicon on Insulator option (IBM, Sansung, STMicroelectronics…)

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Basic MOSFET equations

Why SOI option ?

- Triode $$I_D = \mu C_{ox} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2} n V_D^2\right]$$

- Saturation $$I_{Dsat} = \frac{1}{2n} \mu \ C_{ox} \frac{W}{L}(V_G - V_{TH})^2$$

- Subthreshold swing $$S = n \frac{kT}{q} \ln(10)$$

- Transistor Efficiency $$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox} W/L}{n I_D}}$$

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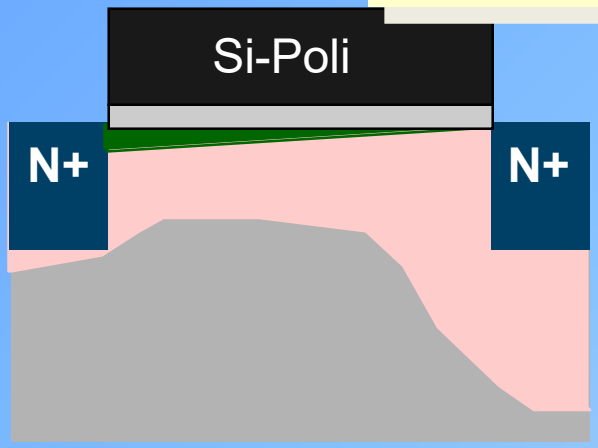
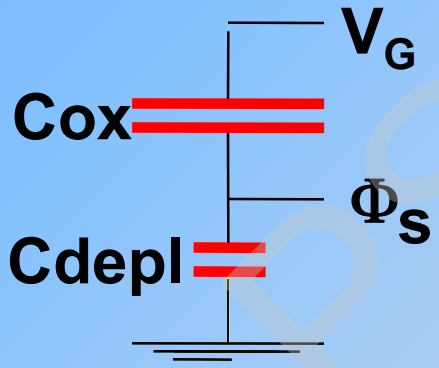
Gate-to-channel coupling

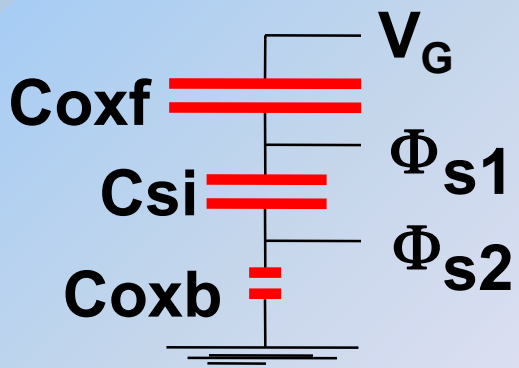
Body Fator (n)



Bulk MOSFET



SOI MOSFET



$n=1+Cdepl/Cox$

$n=1+(Csi*Coxb)/[(Csi+Coxb)*Cox]$

1,3<n<1,5 em MOS convencional **n ≈ 1,05 para SOI**

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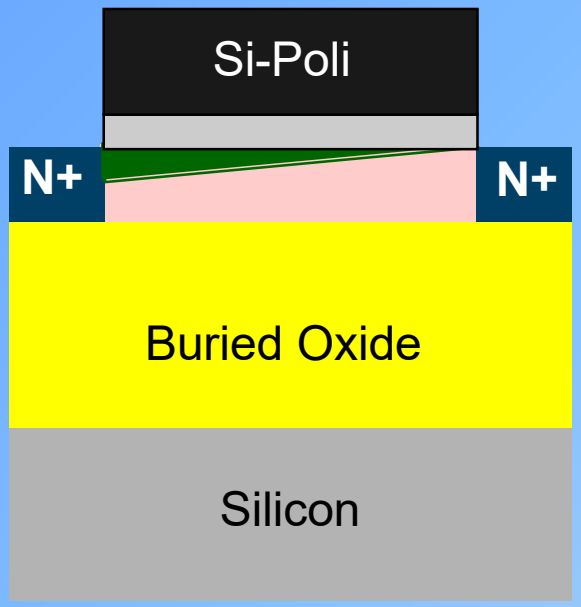
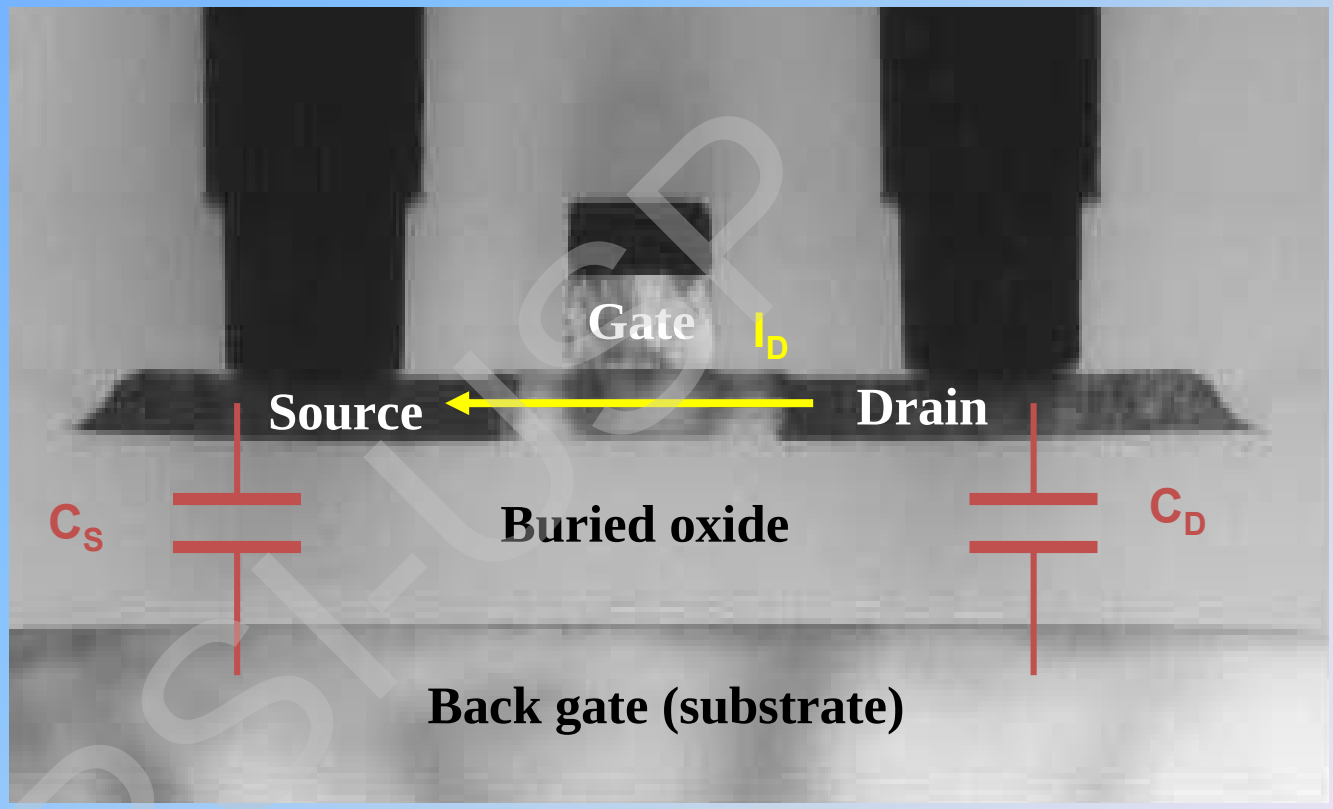
SOI MOSFETs





- C_J in SOI is ~10 X lower than in Bulk MOSFET
- I_D in SOI is 30% higher than Bulk MOSFET
- One generation ahead

G.K. Celler, S. Cristoloveanu, Journal of Applied Physics, Vol. 93, no. 9, p. 4955, 2003

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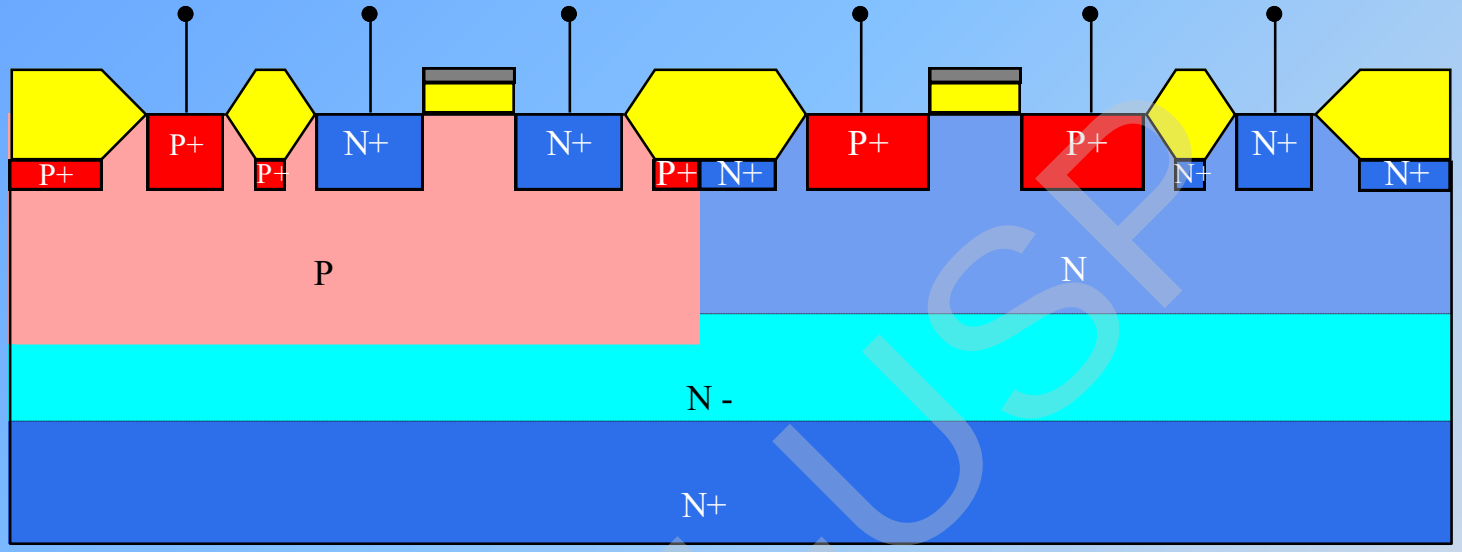
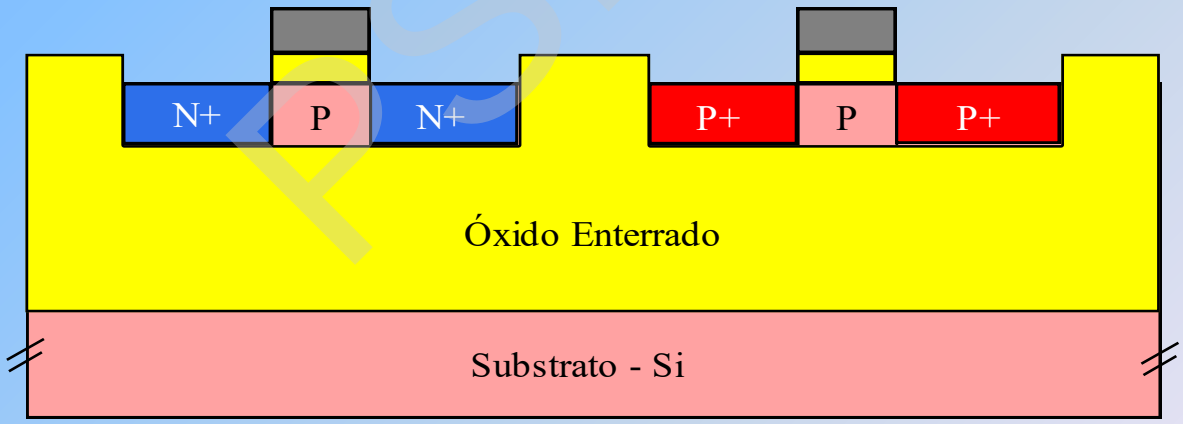
Bulk CMOS



SOI CMOS



- Higher integration density

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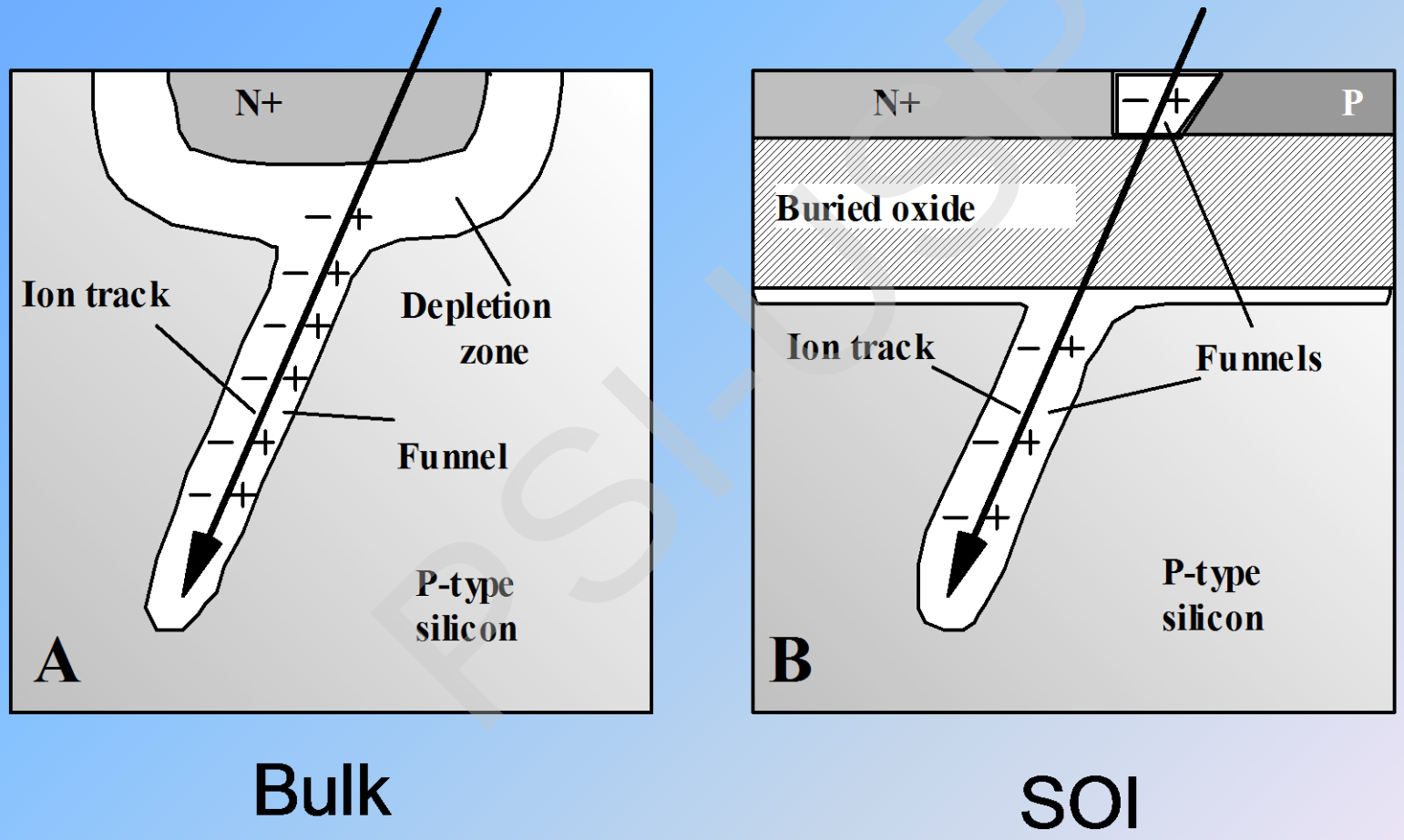
•Radiation Hardness: Single event upset



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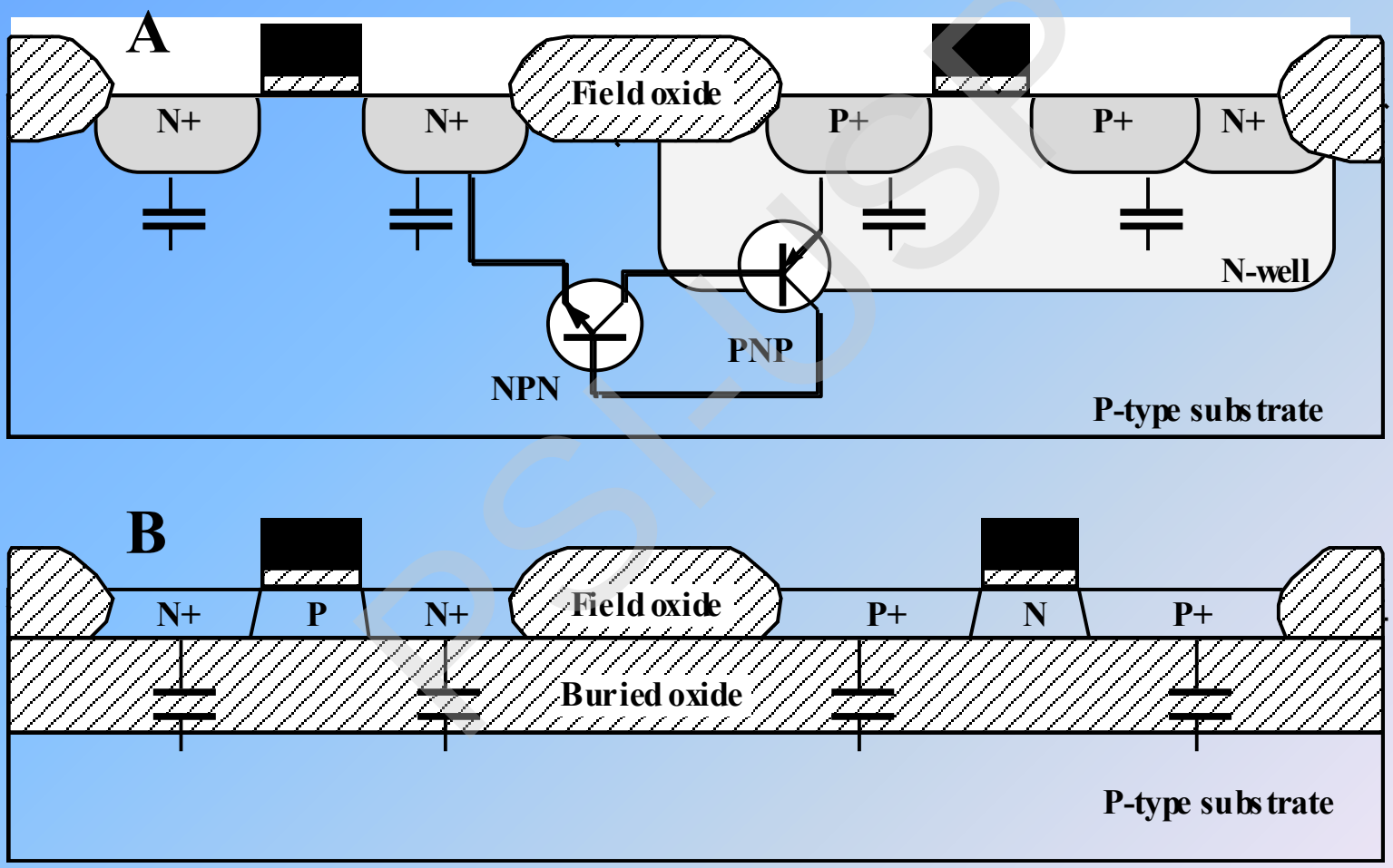
•SOI technology is Latch up free



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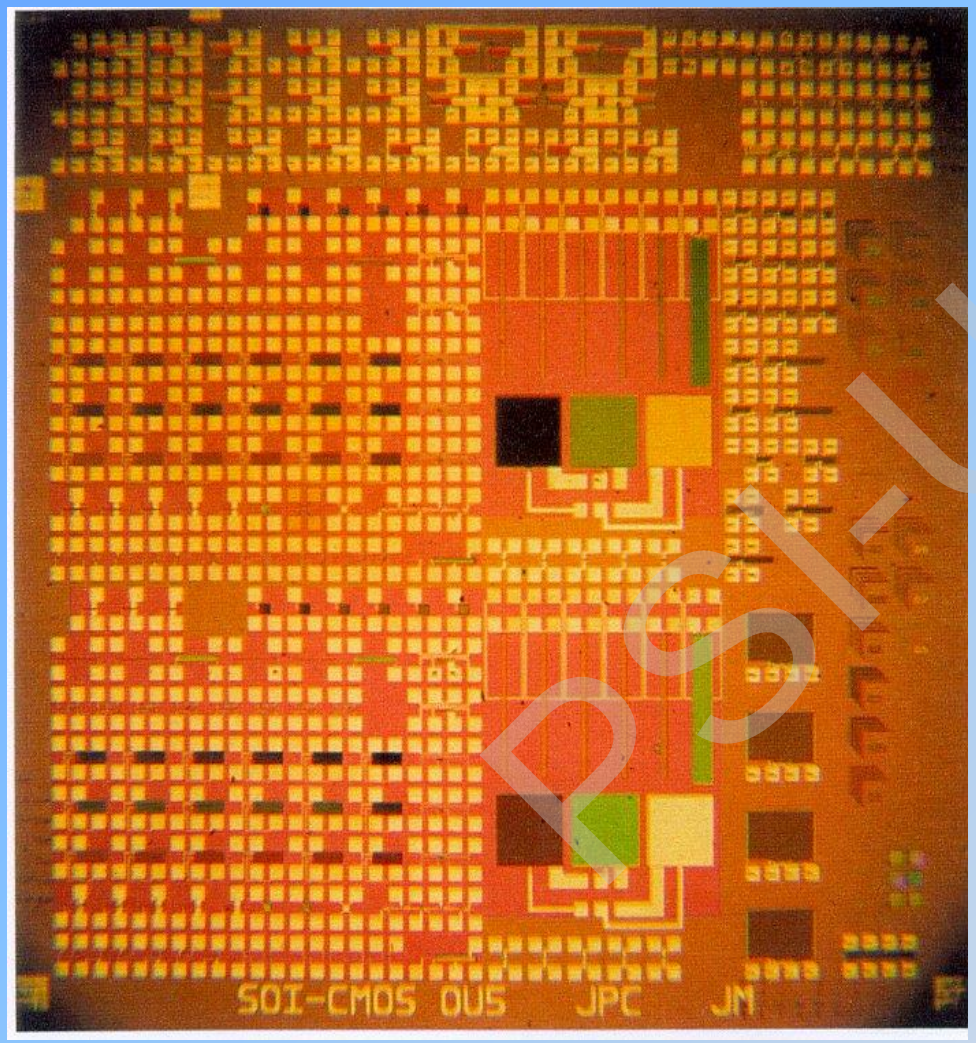
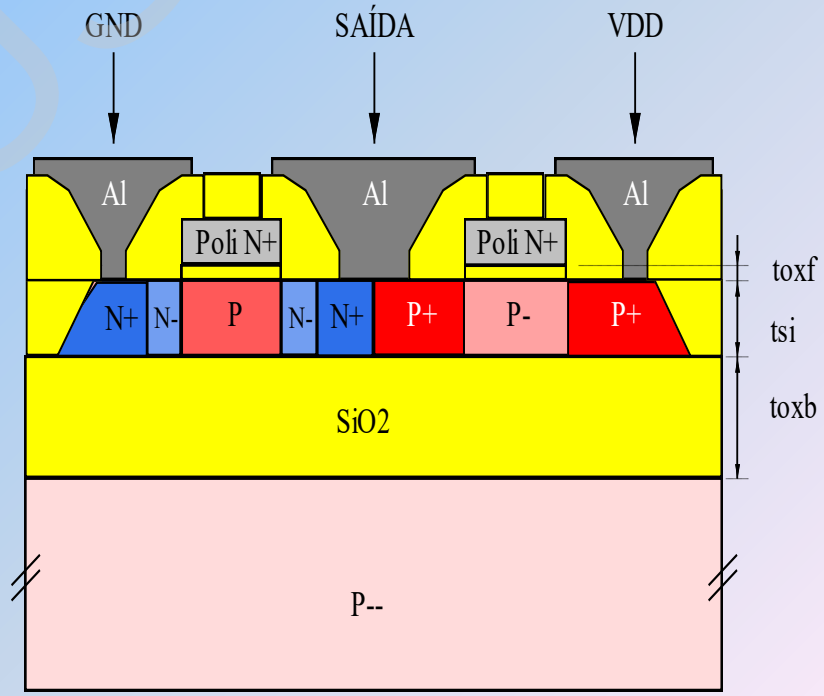
0.5 μm SOI CMOS Technology



- Test integrated circuit (test chip)
- 0.5 μm SOI CMOS Technology developed in Imec at 90's years...



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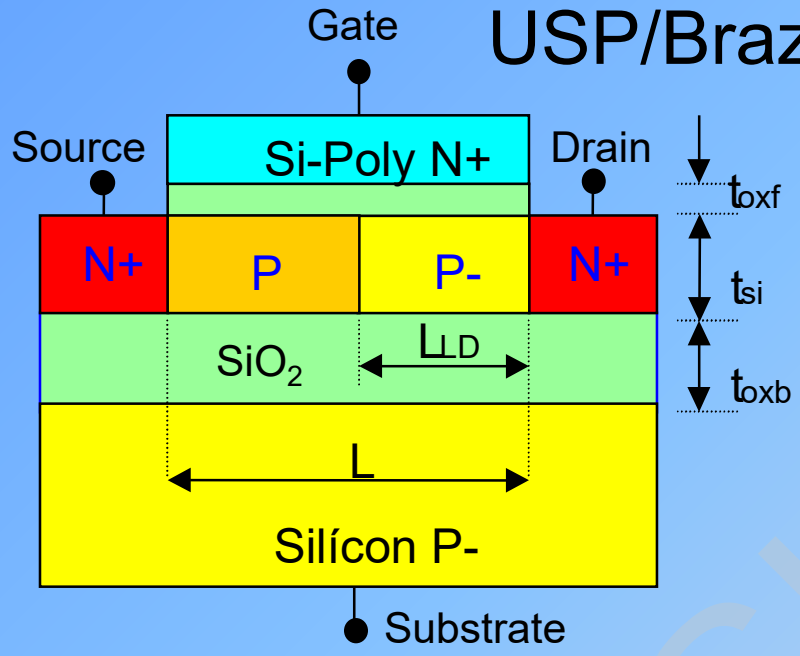
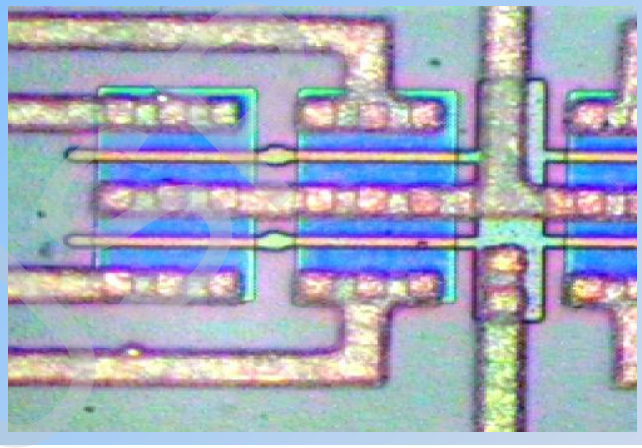
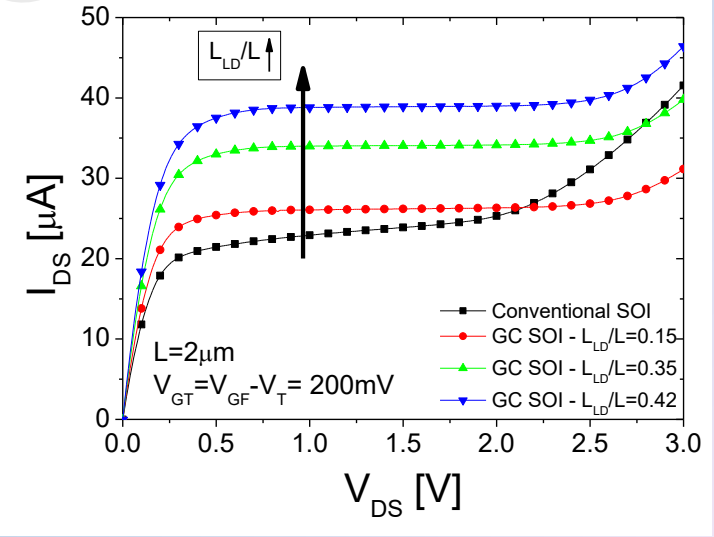
GC SOI MOSFET (Graded Channel) USP/Brazil-UCL/Belgium







Advantages of GC SOI :

- Higher gm
- Lower (better) g_D (higher V_{EA})
- Higher A_V
- Larger Breakdown voltage
- Reduced Harmonic Distortion

* M. A. Pavanello, J. A. Martino e D. Flandre; Solid State Electronics,2000

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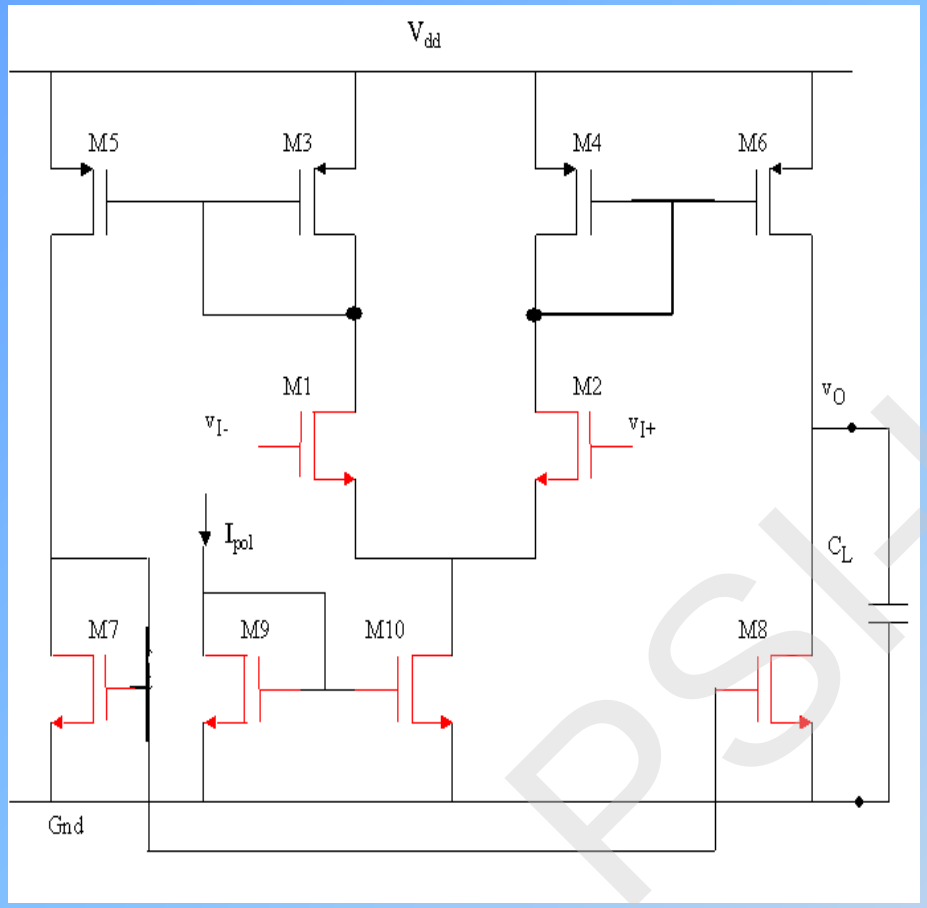
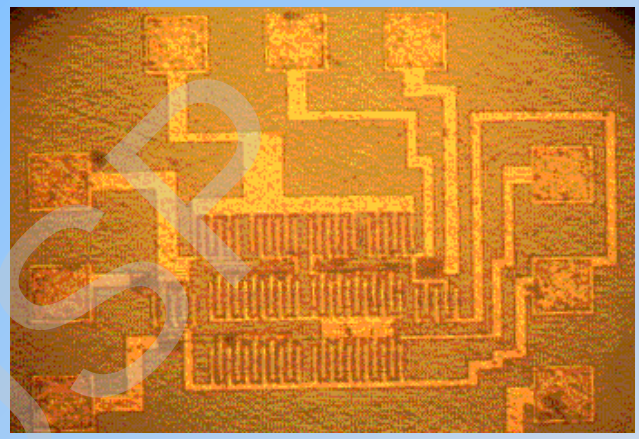
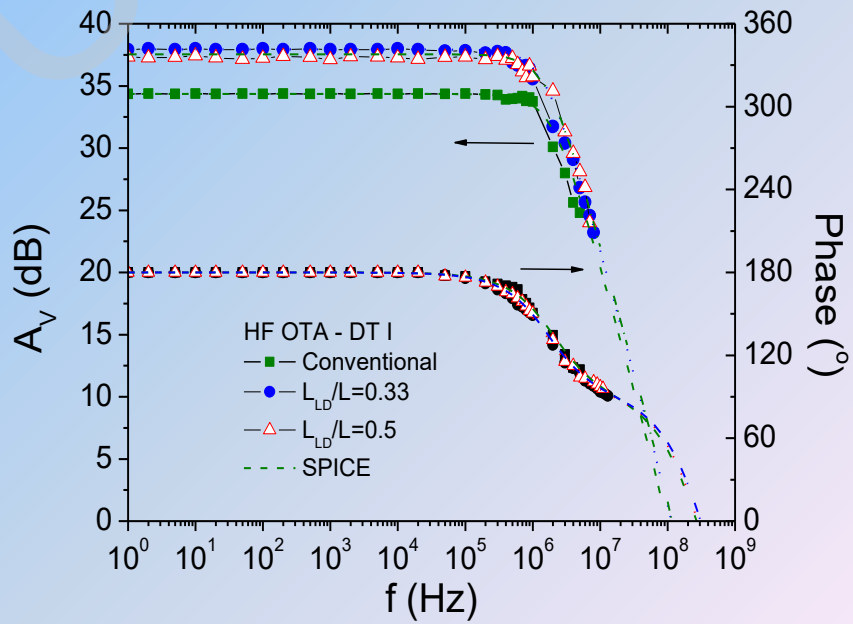
Operational Amplifier
USP/Brazil-UCL/Belgium







•Red Transistors are CG SOI

*S. P. Gimenez, M. A. Pavanello, J. A. Martino; SOI Symposium/ECS, Quebec, 2005

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Scaling roadmap

Ge/III-V, VFET, TFET, NW, Graphene…

Performance

(power x delay)

New process modules

New materials

New device concepts

10-7

22-14-10

FD SOI, Multi-gate, UTBB-SOI

32-22

High-k, Metal Gate

90-65-45/40

Strain, USJ (F,C co-implant, …)

>130

time

* By Cor Claeys

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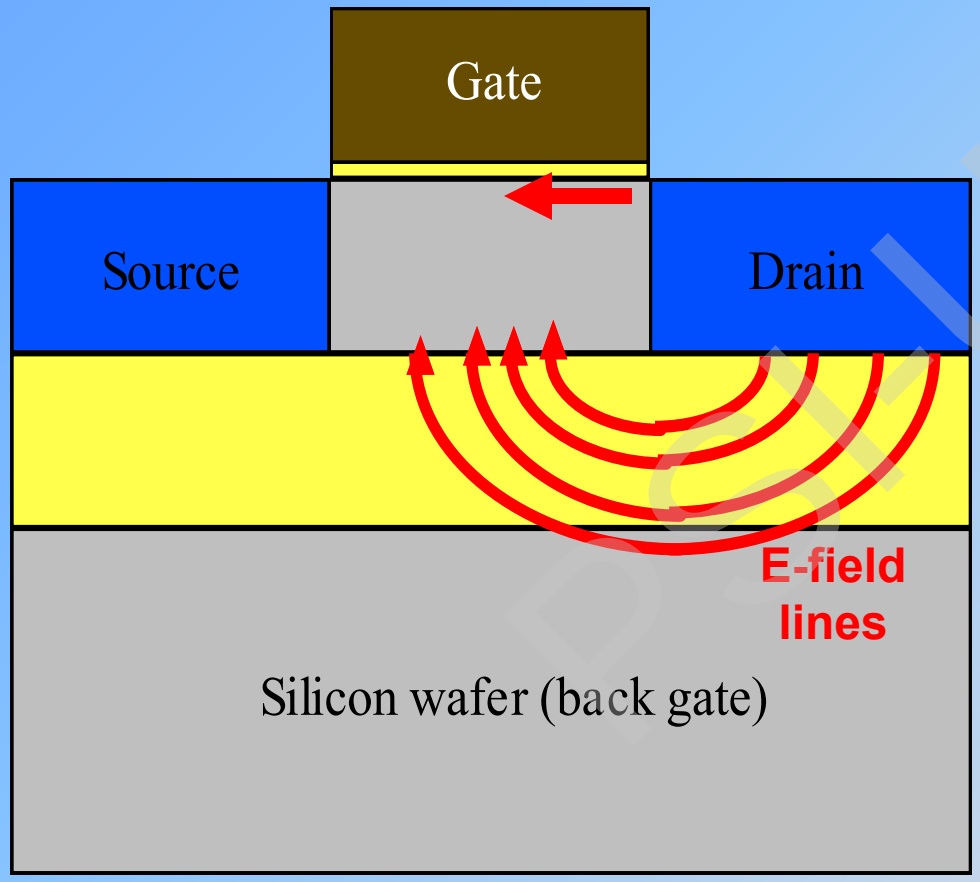
Short-channel problems in MOSFETs



Electric field lines from the drain encroach on the channel region. Any increase of drain voltage decreases the control exerted by the gate on the channel region.

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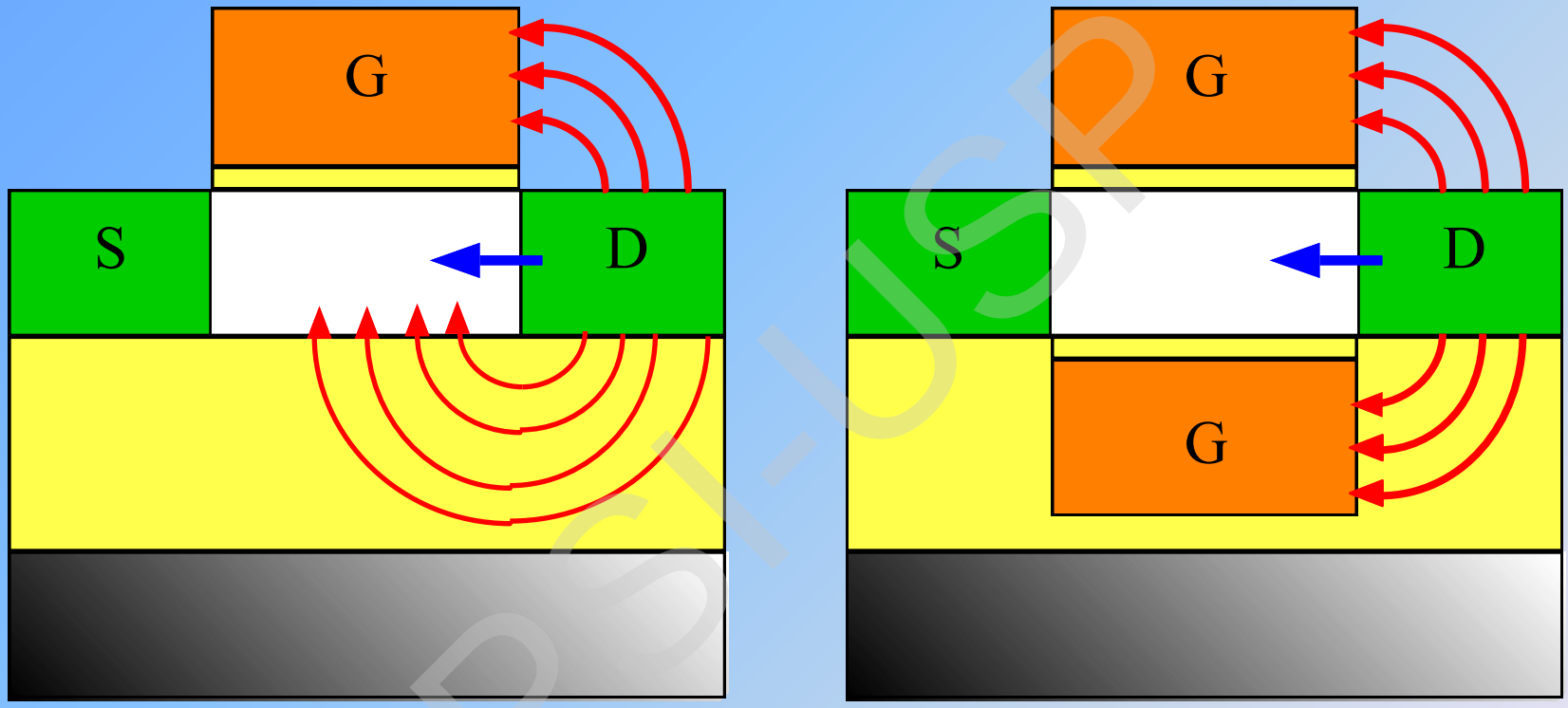
E-Field lines



Regular SOI MOSFET Double-gate MOSFET

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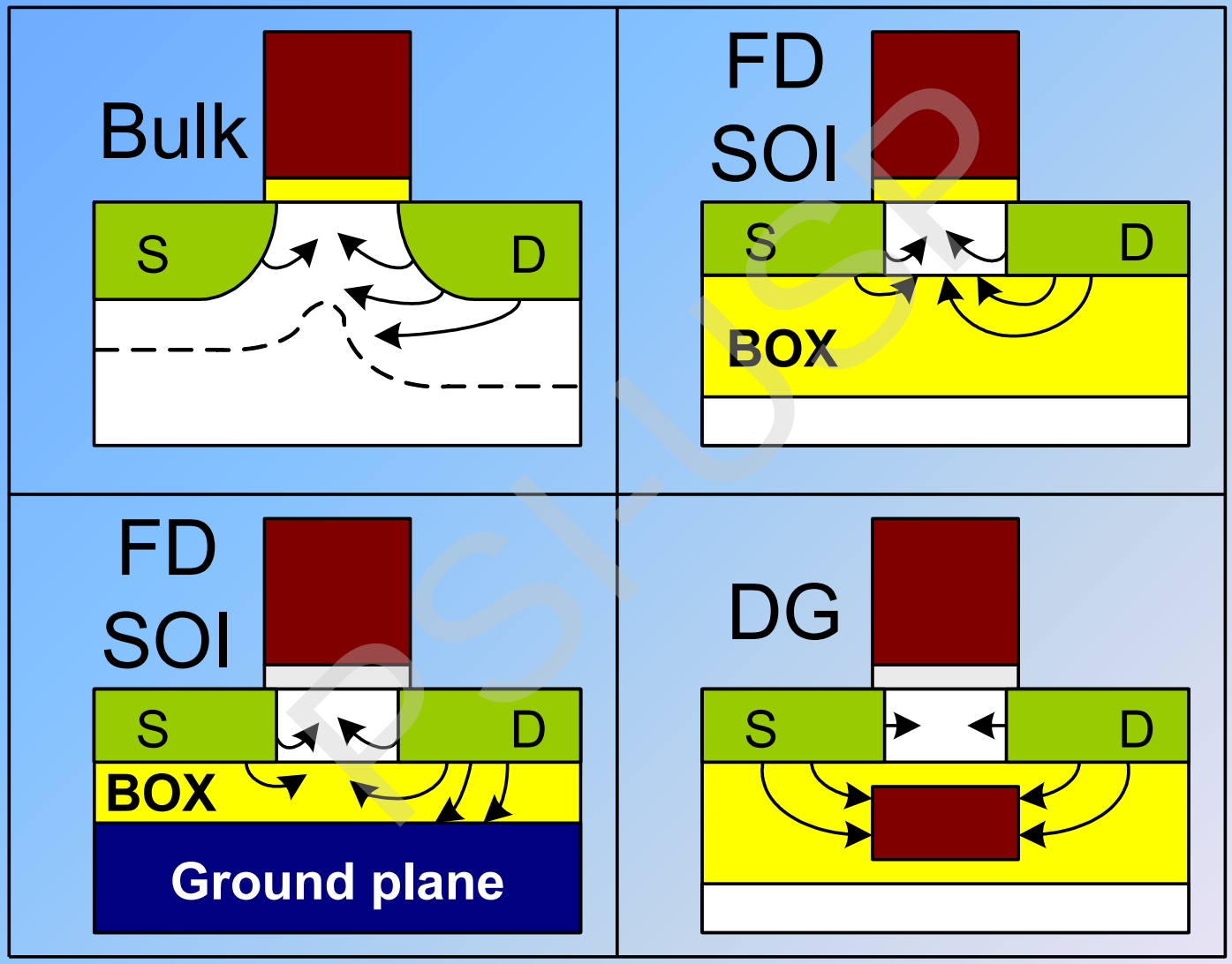
Short Channel Effect



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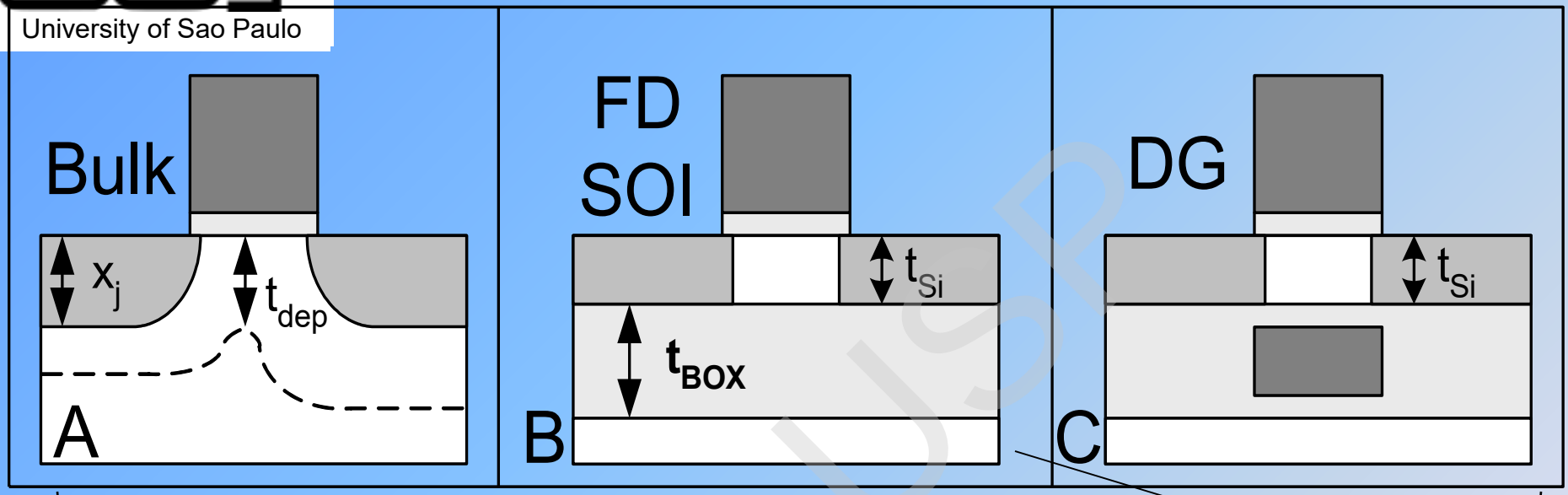
Electrostatic Integrity (EI)



$$V_{TH} = V_{TH\infty} - SCE - DIBL$$

$$SCE = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI\, V_{bi}$$

$$DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI\, V_{DS}$$

$$EI = \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}}$$

$$EI = \left[1 + \frac{t_{Si}^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{Si} + \lambda t_{BOX}}{L_{el}}$$

$$EI = \frac{1}{2}\left[1 + \frac{t_{Si}^2/4}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{Si}/2}{L_{el}}$$

* Jean-Pierre Colinge

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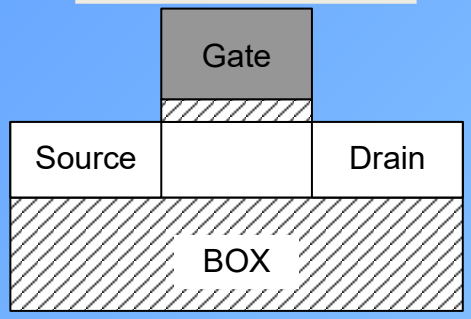
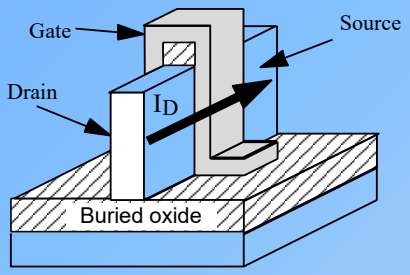
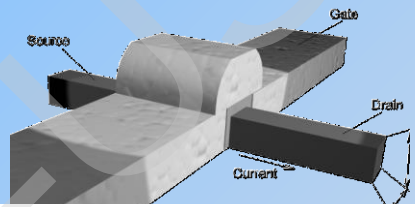
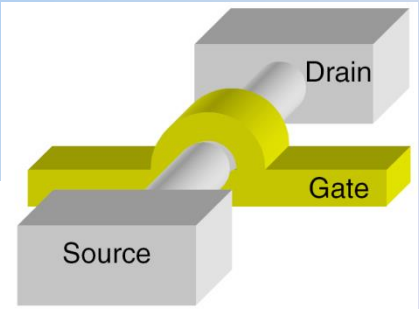
Evolution of Transistors

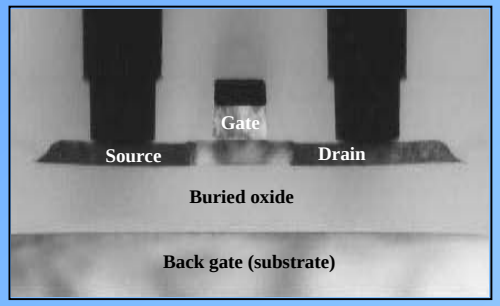
"1 Gate" → "2 Gates" → "3 Gates" → "Gate-all-Around"

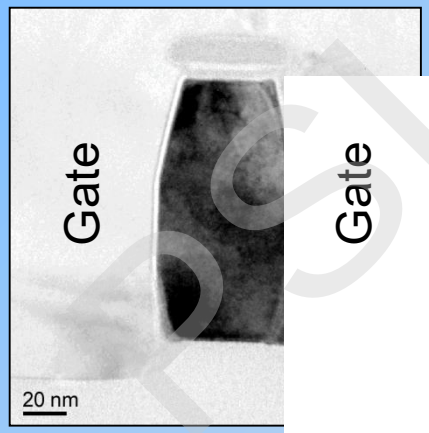


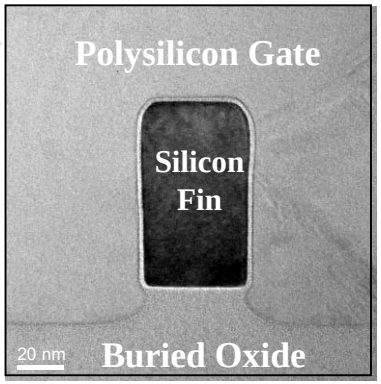


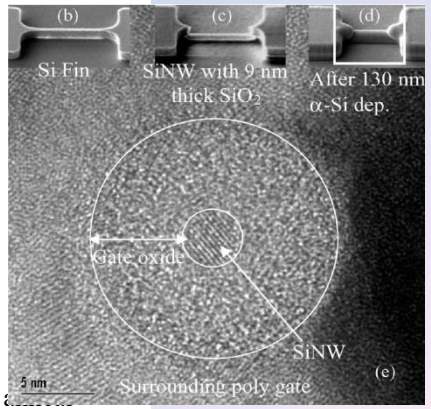












* Jean-Pierre Colinge

Tri-Gate with 800C 600Torr 5min H2Anneal
Fins are 45x78nm, Nice corner rounding by H2 a

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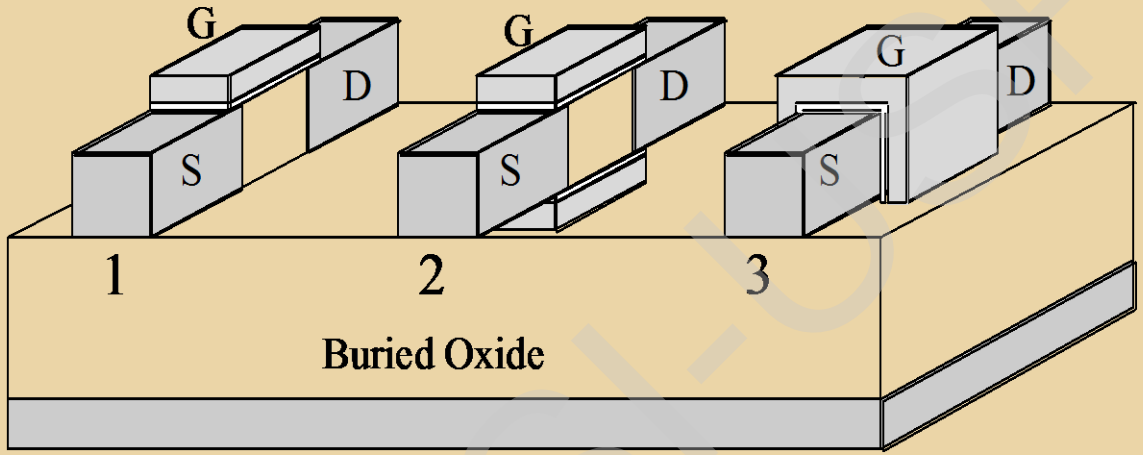
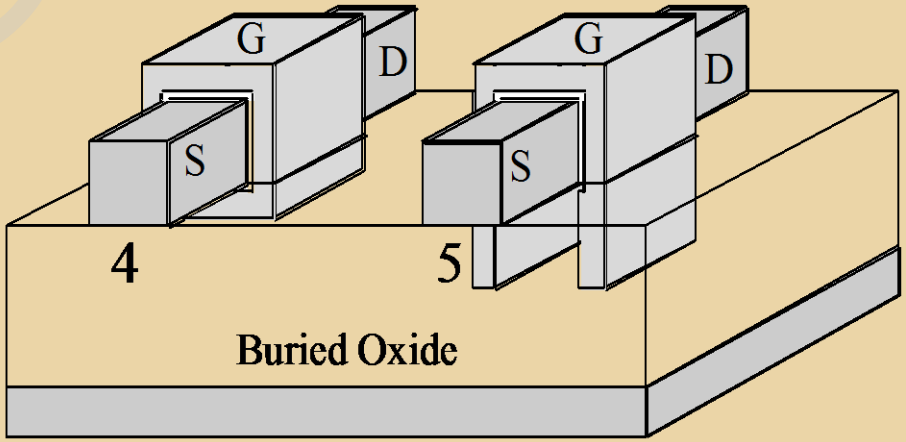
Evolution of Transistors

"Multiple-Gates" MOSFETs



* Jean-Pierre Colinge

1: Single gate
2: Double gate
3: Triple gate
4: Quadruple gate (GAA)
5: Πgate



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Triple^{+}-Gate Transistor

Ω gate

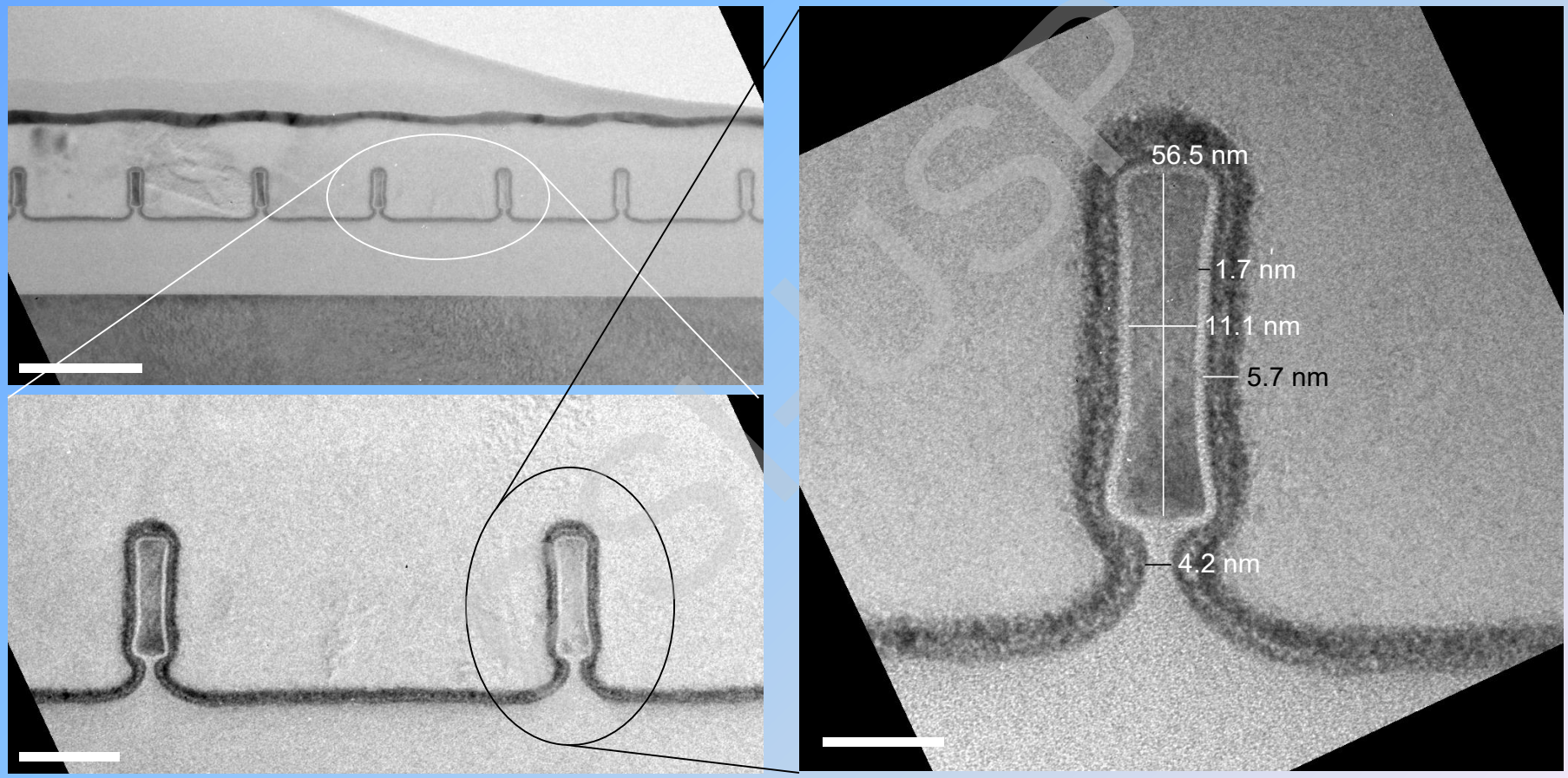

Photo: Courtesy Infineon and Texas Instruments, Inc.

Device Research Conference, 2006

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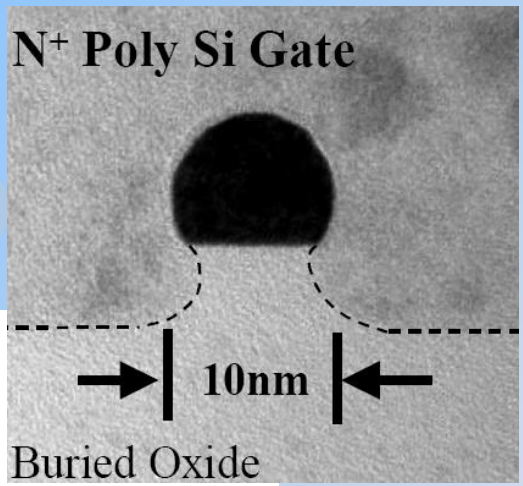
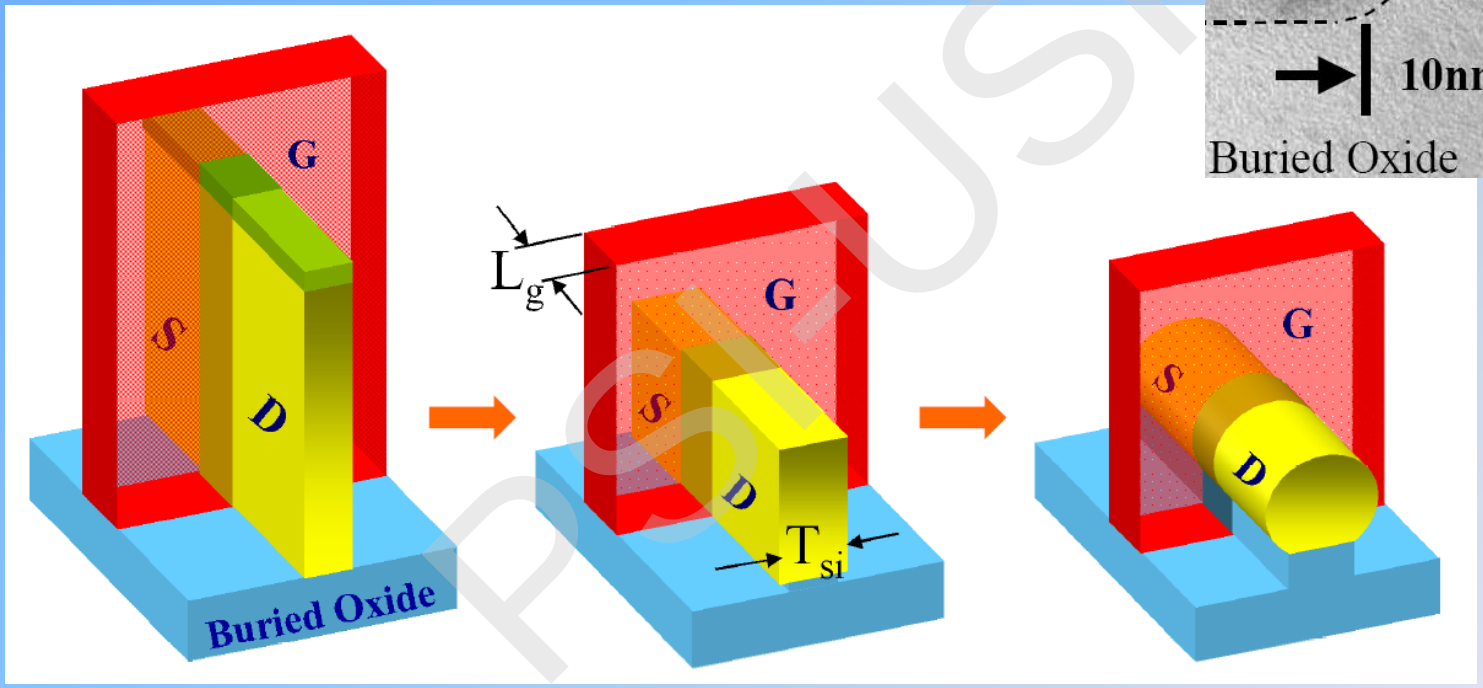
TSMC's Nanowire FET (VLSI'04)





FinFET **Trigate** **Ω gate nanowire**

Fu-Liang Yang, Di-Hong Lee, Hou-Yu Chen, Chang-Yun Chang, Sheng-Da Liu, Cheng-Chuan Huang, Tang-Xuan Chung, Hung-Wei Chen, Chien-Chao Huang, Yi-Hsuan Liu, Chung-Cheng Wu, Chi-Chun Chen, Shih-Chang Chen, Ying-Tsung Chen, Ying-Ho Chen, Chih-Jian Chen, Bor-Wen Chan, Peng-Fu Hsu, Jyu-Horng Shieh, Han-Jan Tao, Yee-Chia Yeo, Yiming Li, Jam-Wem Lee, Pu Chen, Mong-Song Liang, Chenming Hu, "5nm-gate nanowire FinFET" , Symposium on VLSI Technology. Digest of Technical Papers, pp. 196-7, 2004

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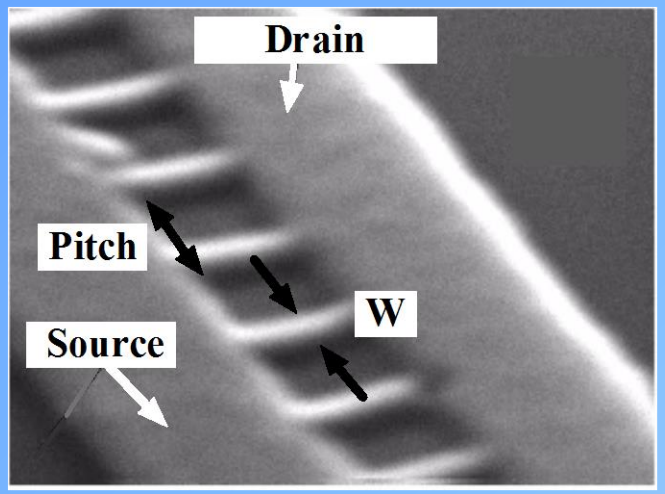
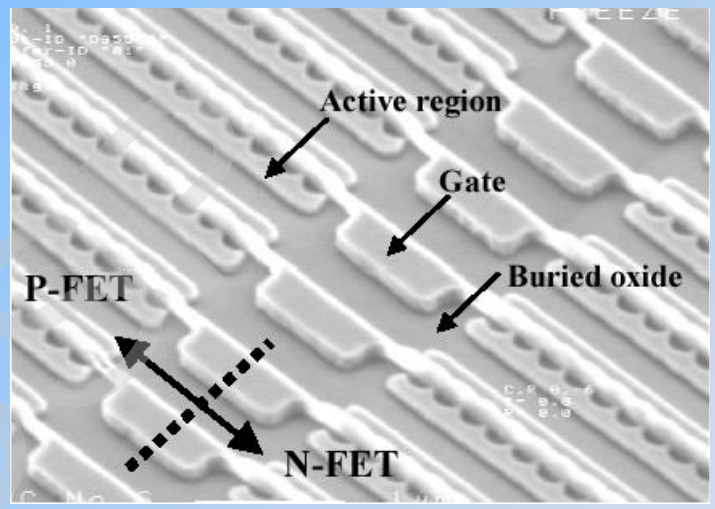
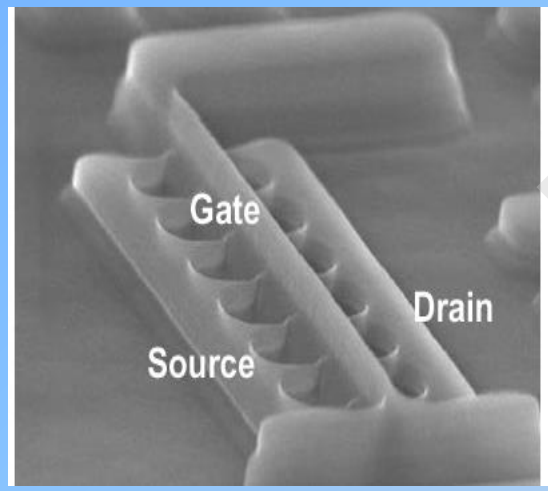
Fin structure
"Discrete" current values

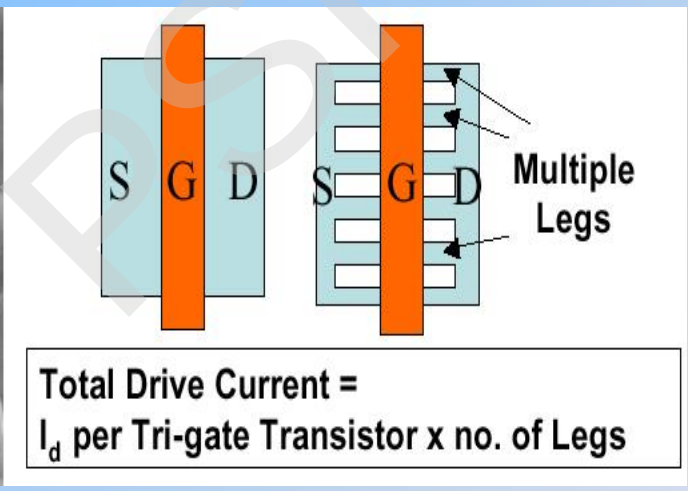


Quantum-Wire MOSFET
(UCL, SOI Conf., 1995)



Omega gate
(TSMC, IEDM 2002)





INTEL's Tri-gate
(SSDM'02)

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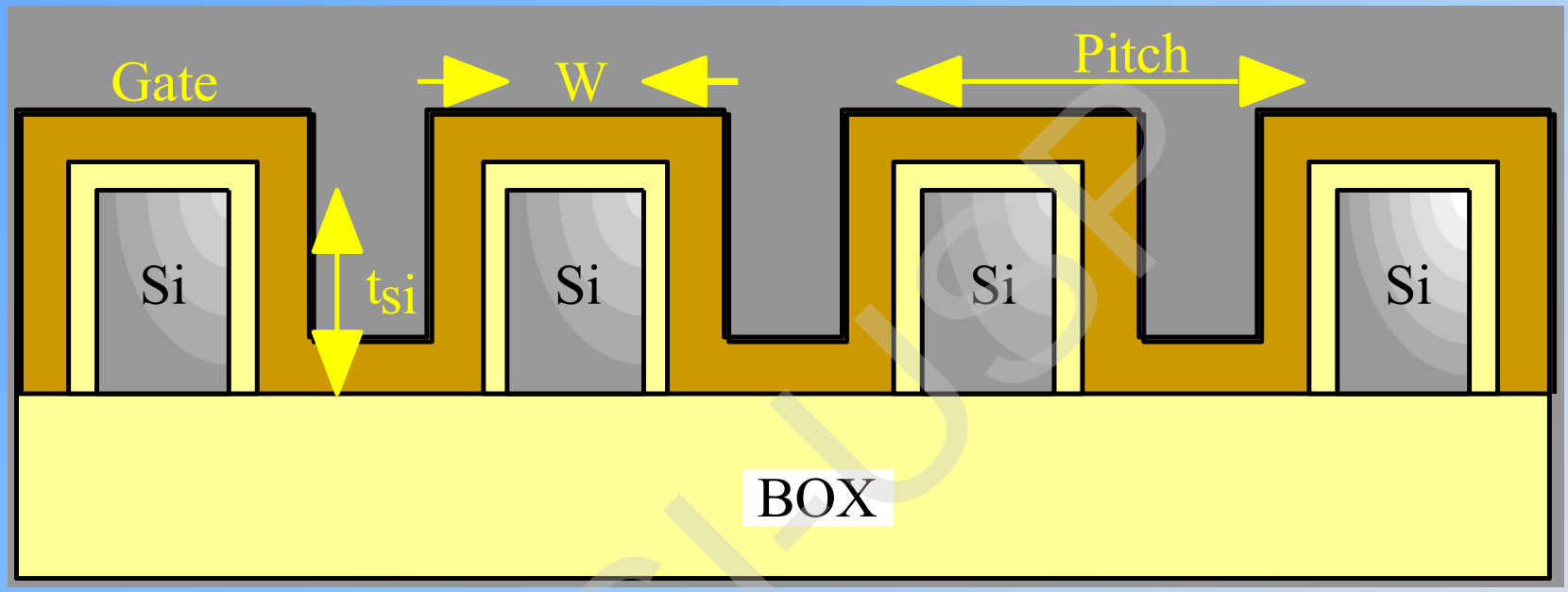
Current per Surface Area

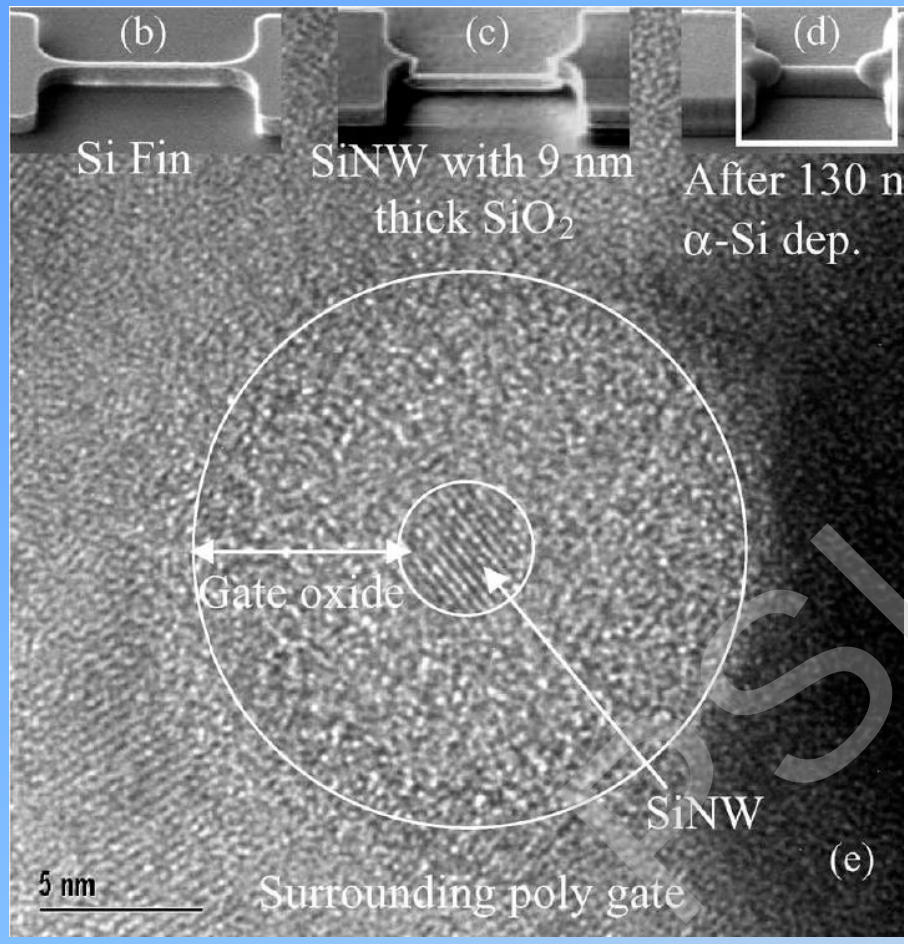


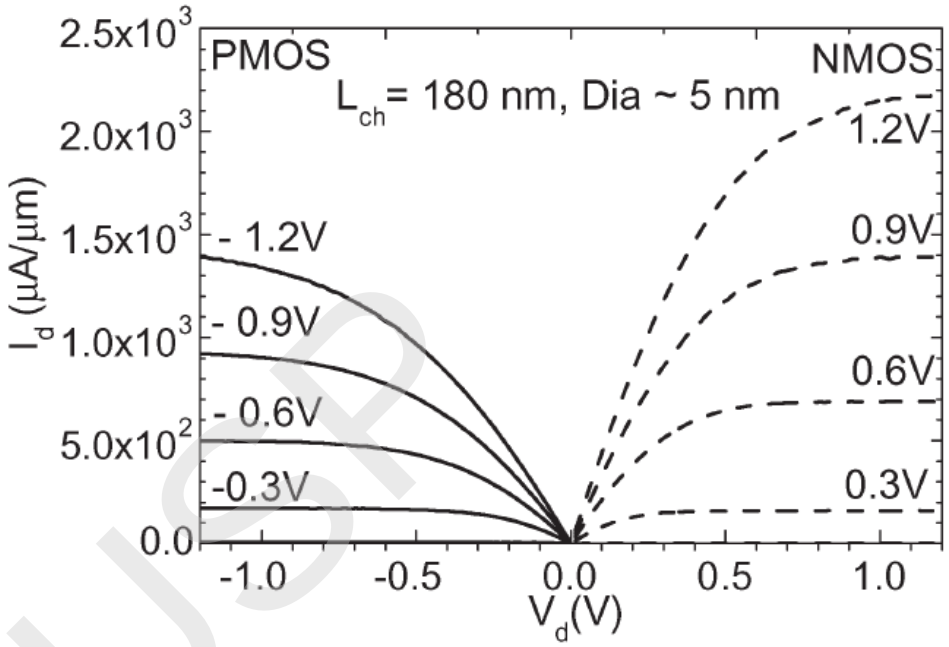
$$I_D = I_{Do}\frac{\theta\mu_o W + 2\mu_1 t_{si}}{\mu_o P}$$

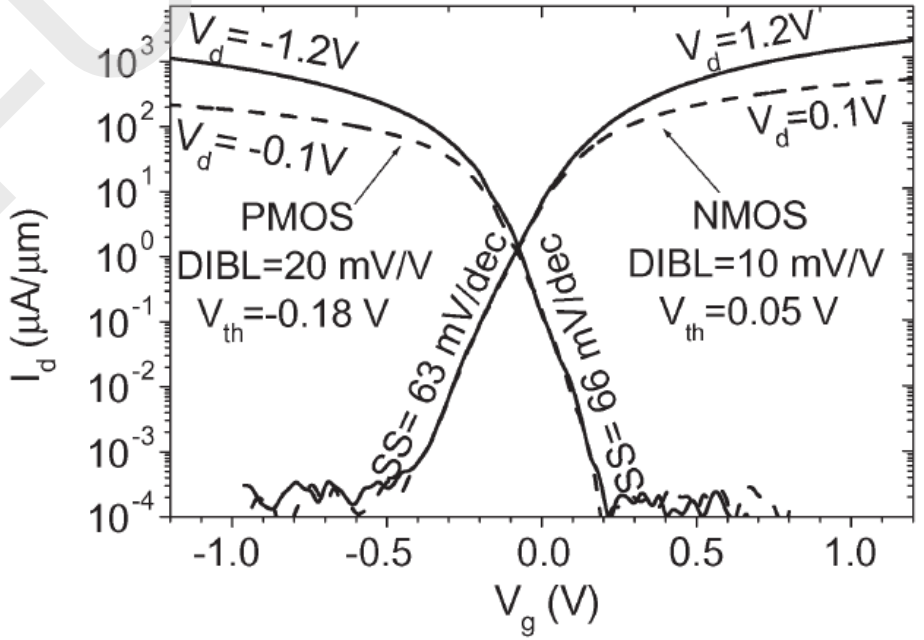
θ=1 in a triple-gate MOSFET
θ=0 in a FinFET

where I_{Do} is the current of a planar, single-gate transistor occupying the same area; μ_o is the mobility at the top interface, μ_1 is the sidewall mobility.

Nanowire FET
IEEE EDL 2006





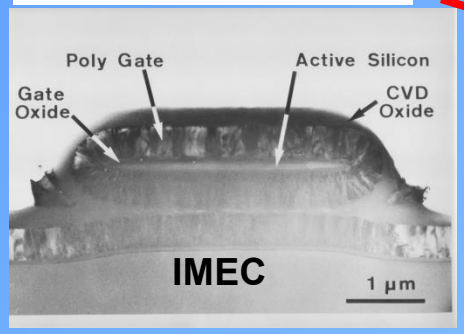


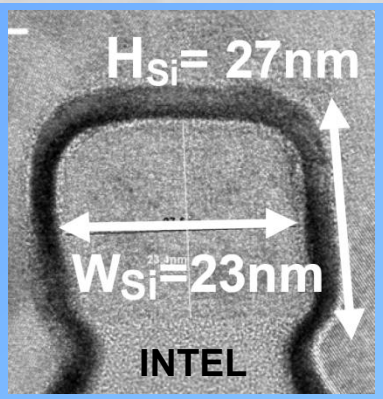
"High-performance fully depleted silicon nanowire (diameter /spl les/ 5 nm) gate-all-around CMOS devices", Singh, N.; Agarwal, A.; Bera, L.K.; Liow, T.Y.; Yang, R.; Rustagi, S.C.; Tung, C.H.; Kumar, R.; Lo, G.Q.; Balasubramanian, N.; Kwong, D.-L., IEEE Electron Device Letters, Vol. 27, no. 5, pp. 383- 386, 2006

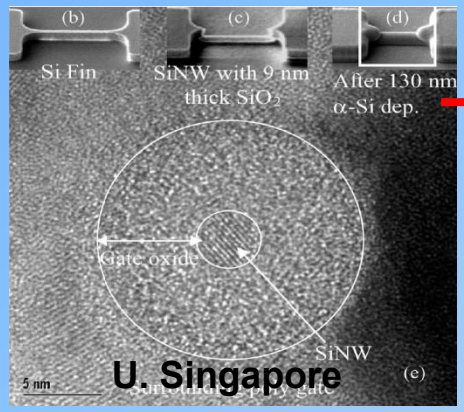
U. Singapore

Multi-Gate MOSFET Structures

University of Sao Paulo







Double gate

GAA, SON

MIGFET

FinFET

Triple gate

Trigate FET

Π-gate FET

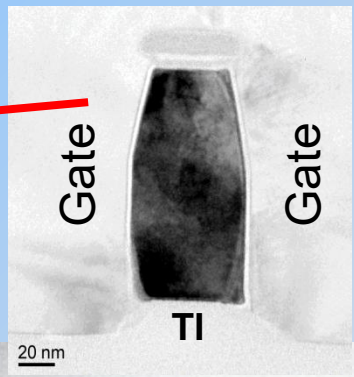
Ω-gate FET

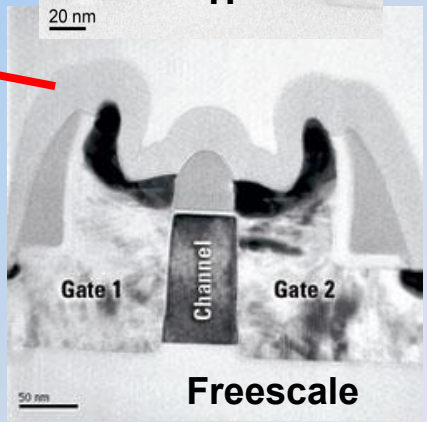
Surrounding gate

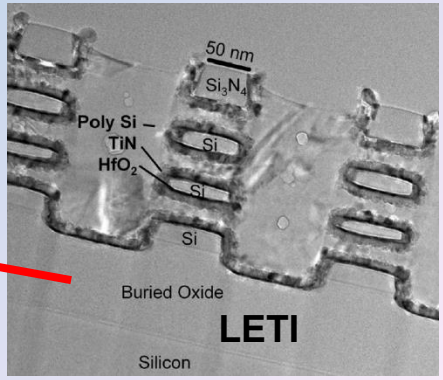
Quadruple gate FET

Cylindrical FET

Multi-bridge/stacked nanowire FET

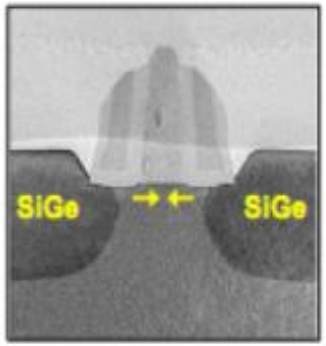
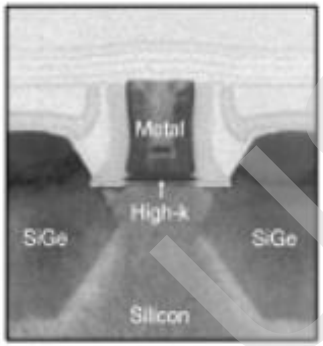
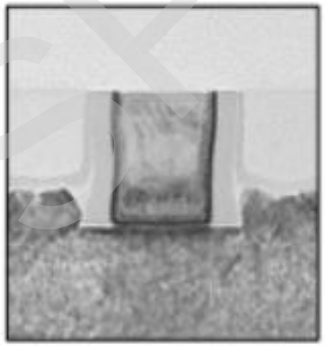
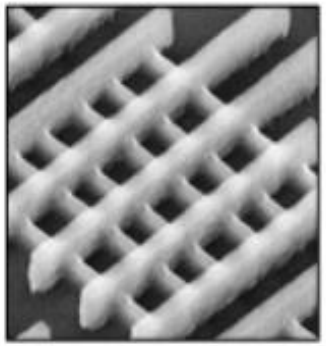






* Jean-Pierre Colinge

Intel Transistor Leadership

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm
				
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

High-k Metal Gate

Tri-Gate

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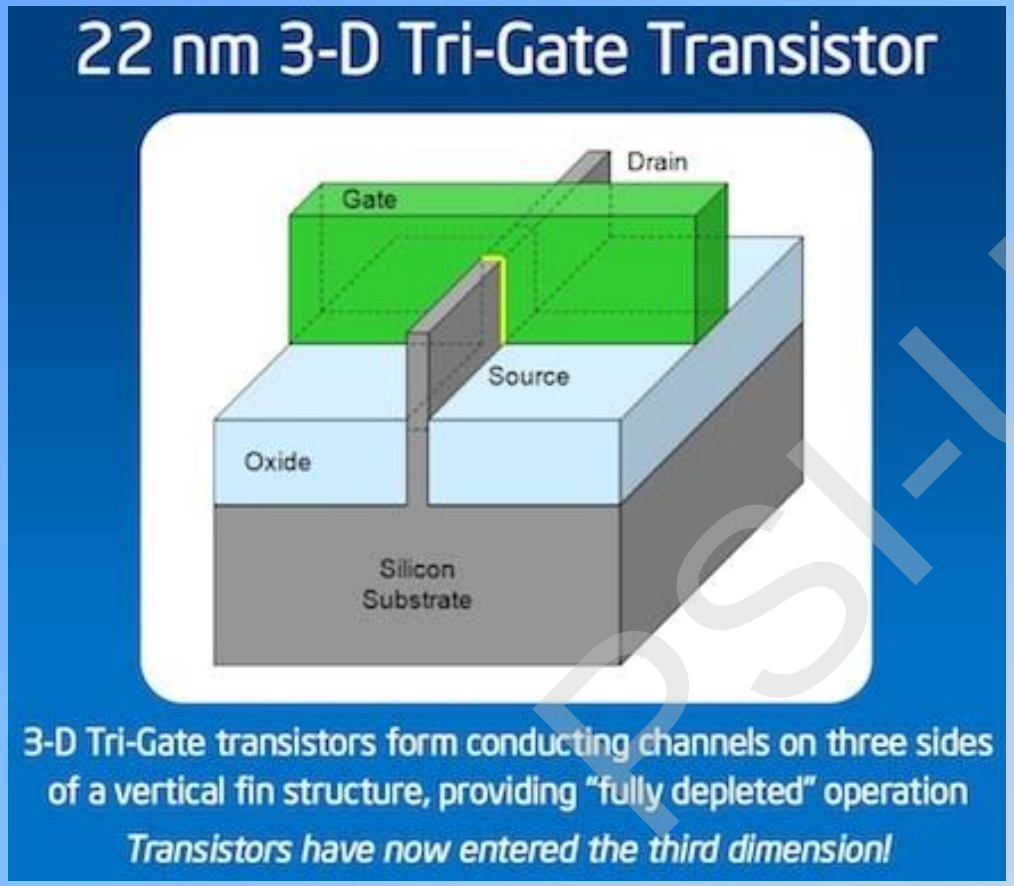
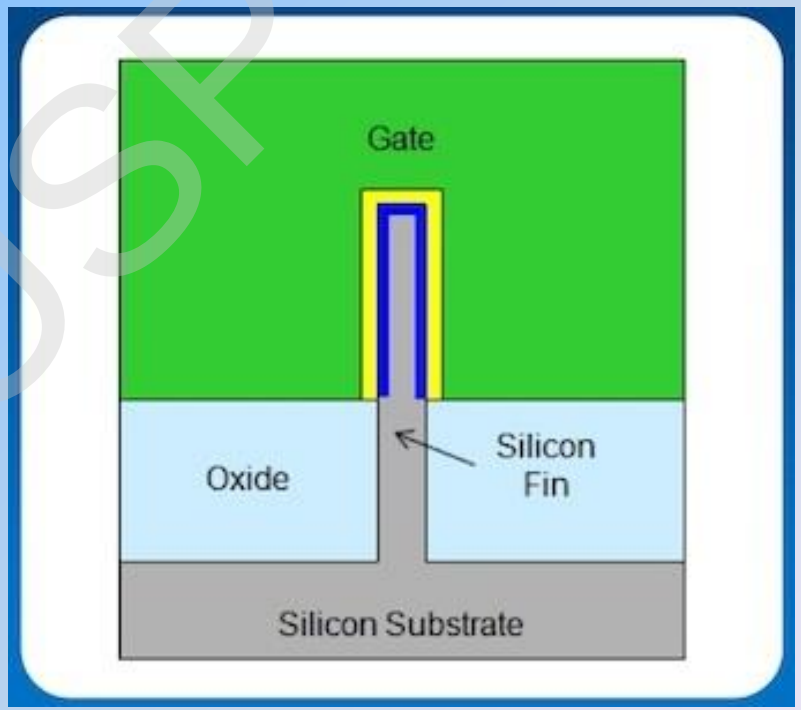
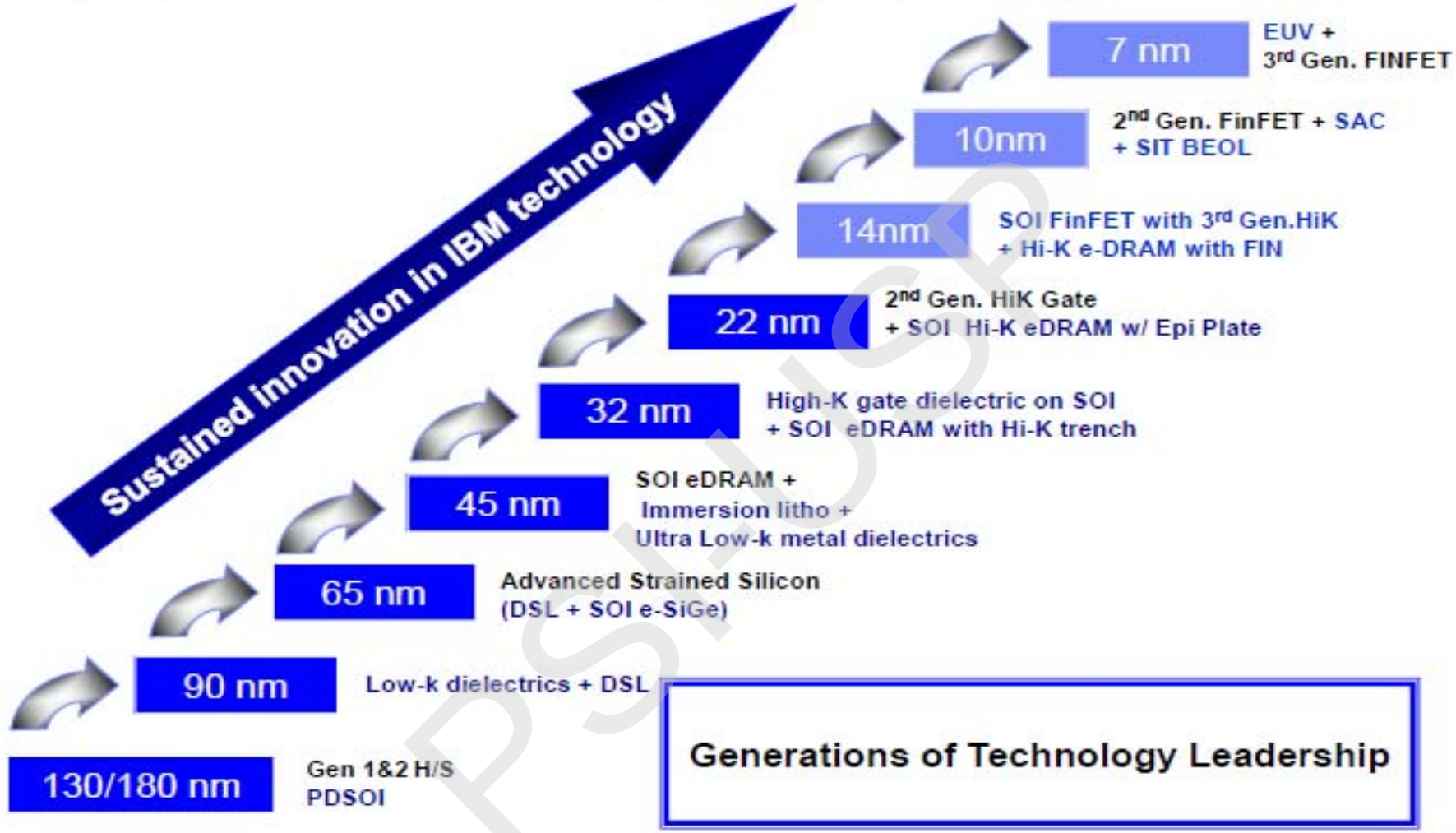
Bulk FinFET – Intel (Triple Gate or 3D)





Intel Microprocessor Ivy Bridge uses 22-nanometer technology

Ten Generations of IBM SOI Technology

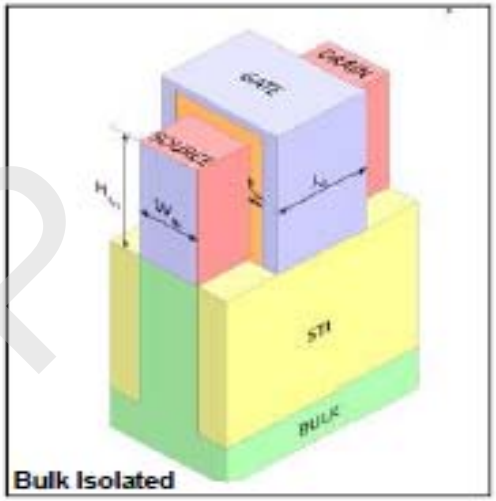


Why FINFET

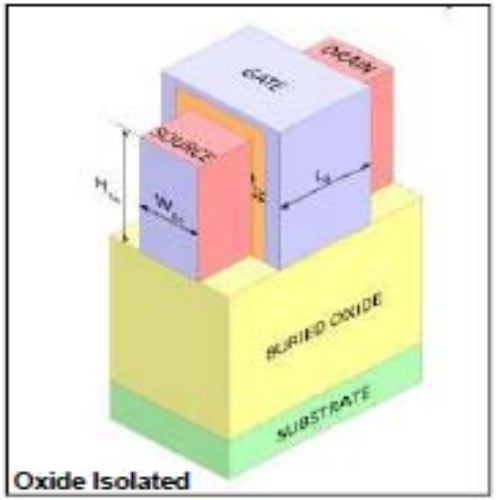
IBM

Many *intrinsic* advantages in FinFET

- **Enhanced control of Short Channel Effect (SEC)**
  - Multiple gates control the channel SCE in FF
  - Doping controls the SCE in bulk
- **Significant DIBL reduction**
  - With fully-depleted device capability
  - Better electrostatics
- **Excellent low Vdd performance**
  - Performance roll-off with Vdd not as significant as bulk
  - Potential for lower power operation
- **Scalability for many generations once isolation is fixed**

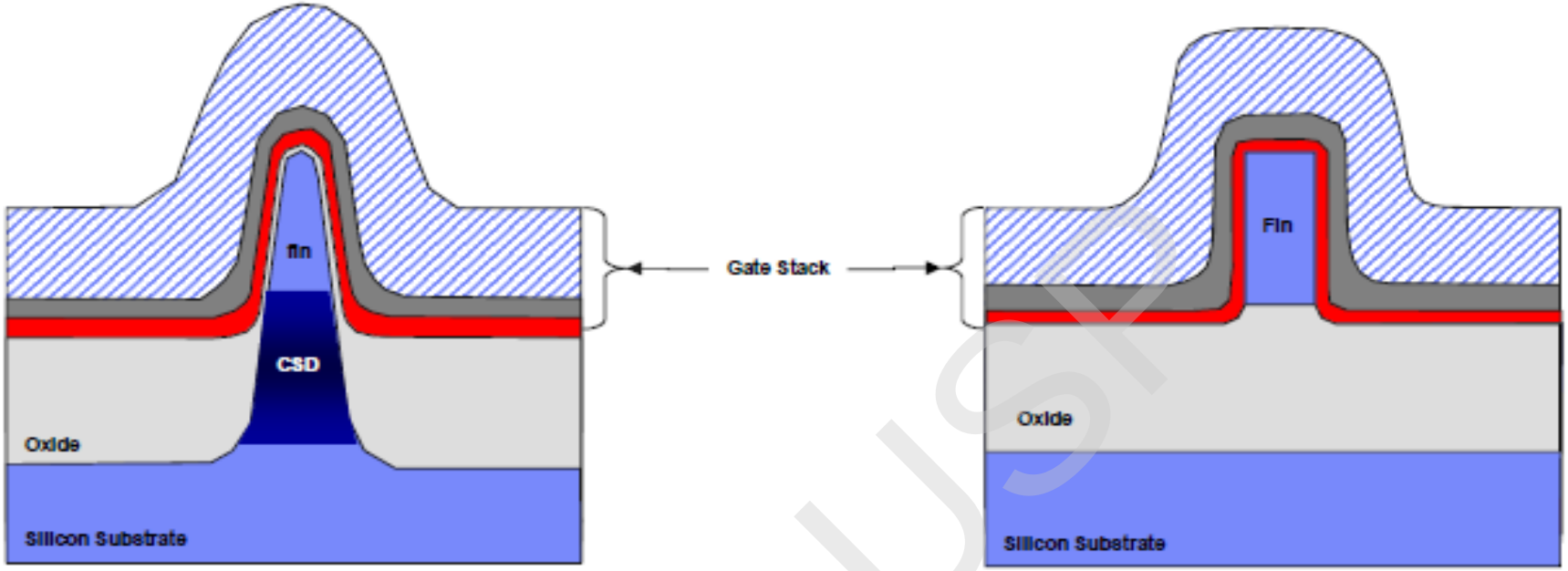


Bulk Isolated



Oxide Isolated

Current FinFETs : Bulk Isolated vs Oxide Isolated



- **Bulk isolated**
  - Process more expensive than oxide isolated
  - Process integration scheme has process control challenges
  - Bulk starting wafer with Channel Stop Implants
- **First introduced at 22nm**
  - Challenging bring up
  - First generation performance lacking
  - Expect second generation improvement
- **Foundries following 22nm lead for 14/16nm**
  - Major foundry FINFET introduction will be bulk isolated
  - 10nm needs to address some of the bulk challenges

- **Oxide isolated**
  - Isolation process simpler less expensive
  - Many control issues improved over bulk isolated FinFet
  - SOI starting wafer
- **IBM choice for internal clients**
  - Lower risk
  - Better power/performance
- **IBM 10nm JDA investigating both options**
  - IBM internal 14/10nm is SOI FINFETs

Comparison

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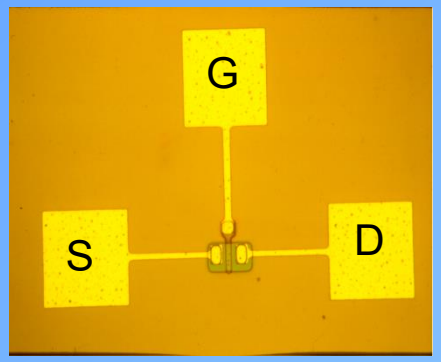
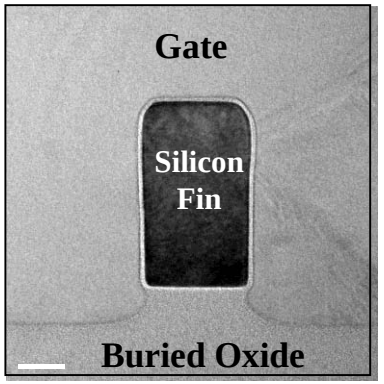
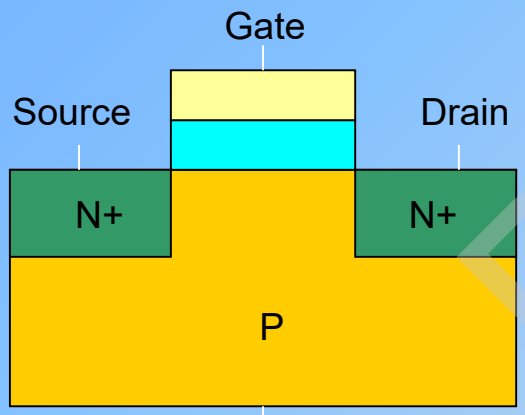
Evolution of MOSFET (main steps)

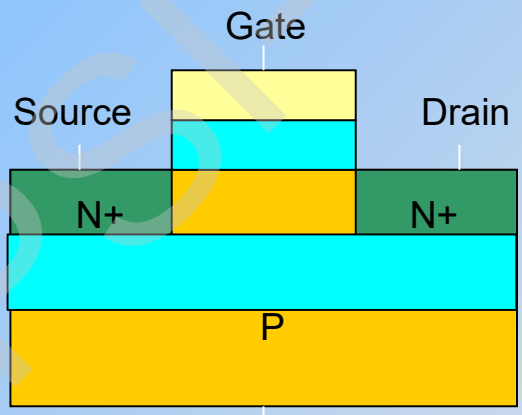






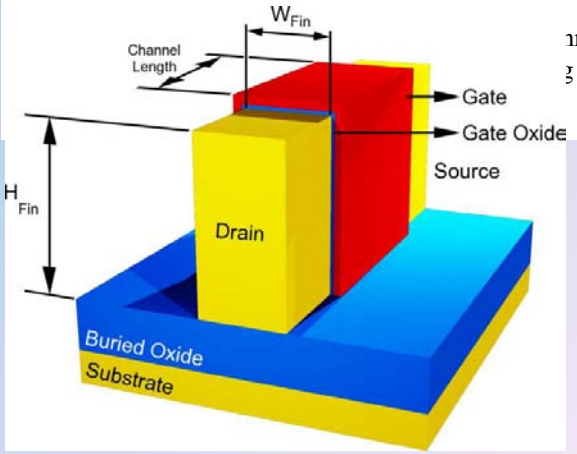
1 Gate "Single Gate"

Bulk – MOSFET (Planar)



1 Gate "Single Gate"

SOI MOSFET (Planar)



2 or 3 Gates "**FinFET**"

(Vertical-3D)

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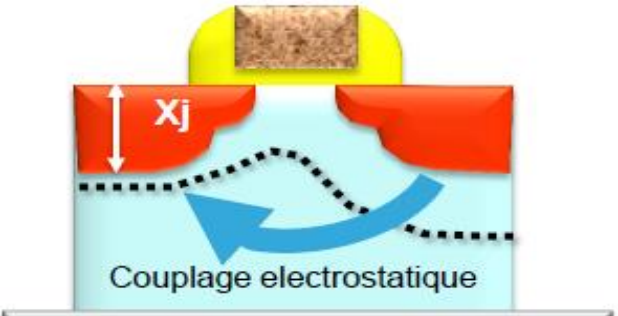
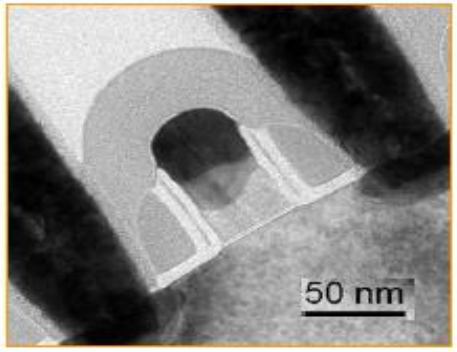
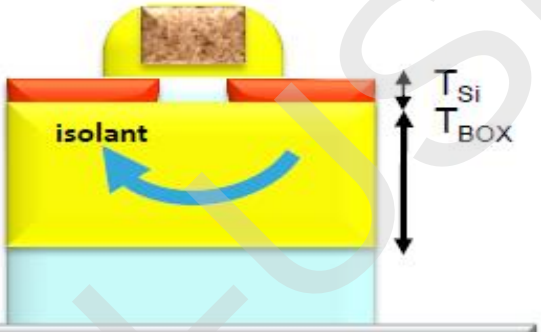
Planar option: UTBB FD SOI

From Bulk to Thin-Silicon Channels

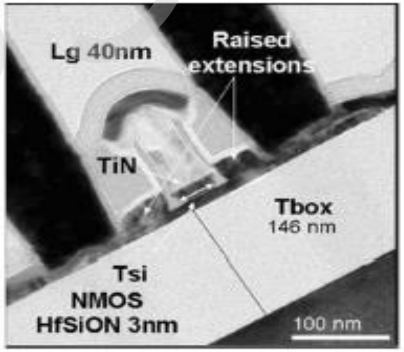


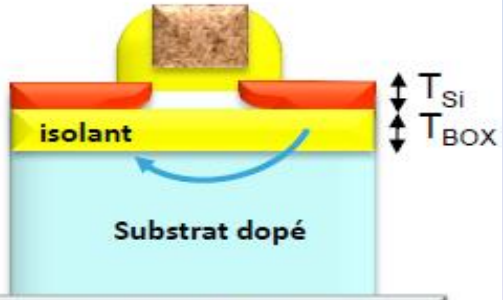
Bulk Silicon
Strong Parasitic Effects



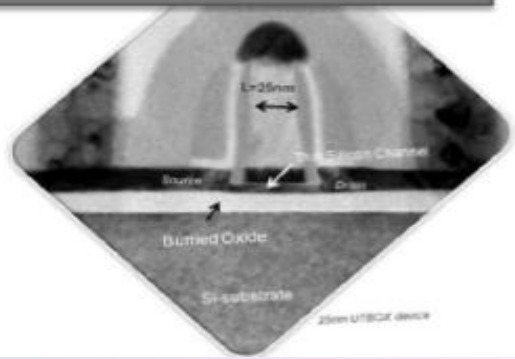


FDSOI/UTB with thick BOX
Reduced Parasitics





FDSOI UTBB : Thin BOX
Parasitics Suppressed



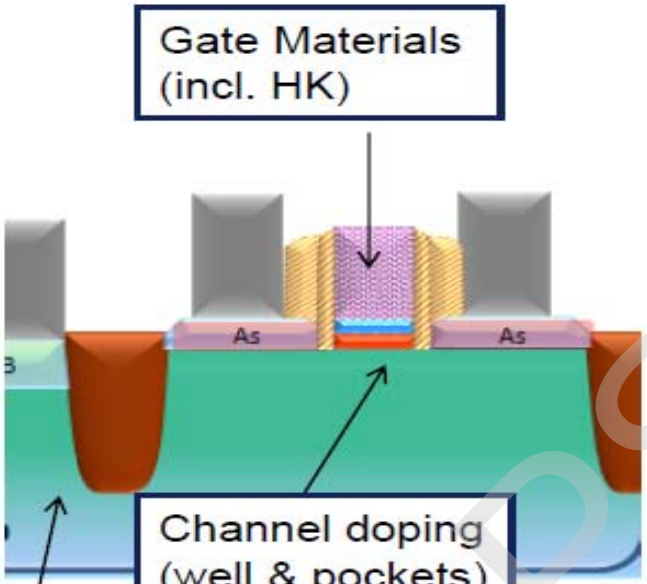
leti
life.augmented

Planar option: UTBB FD SOI

Threshold Voltage Control

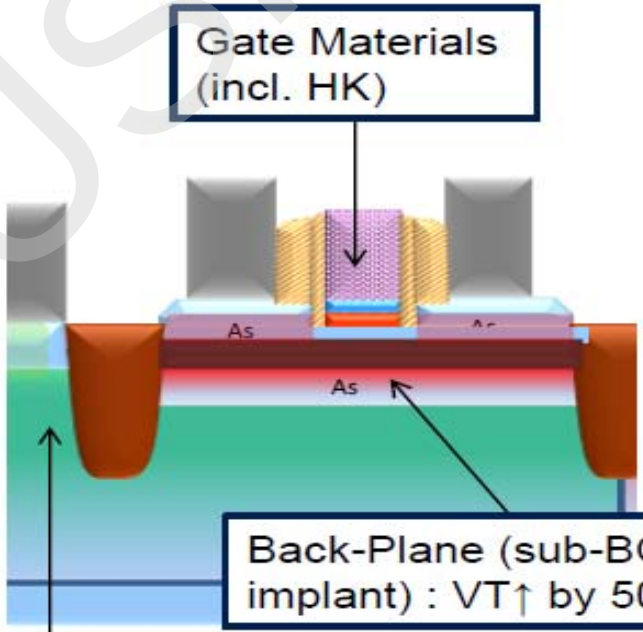
BULK

Doped channel



FDSOI

Undoped channel



Planar option: UTBB FD SOI

UTB-FDSOI Demonstrations

F.Andrieu et al. VLSI 2006

sSOI UTB

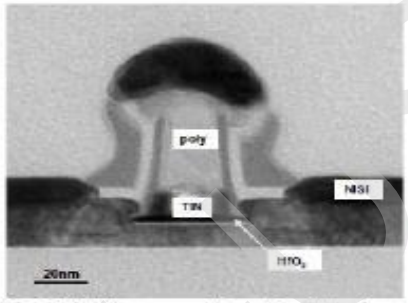
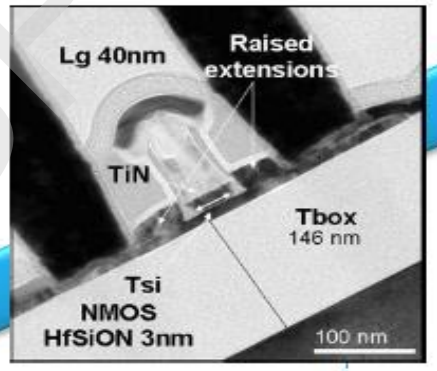


Fig. 3: TEM cross section of a 30nm long FDSOI transistor.



Fenouillet et. al, IEDM 2007

45nm UTB devices

Utlra scaled MOSFET

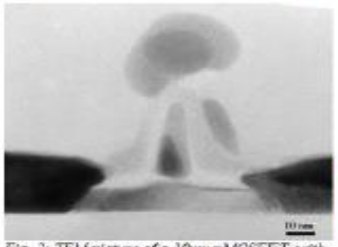


Fig. 2: TEM picture of a 10nm nMOSFET, with a 12nm channel thickness

J.Lolivier et al. SOI conf 2004

1st HiK-Metal 300mm UTB

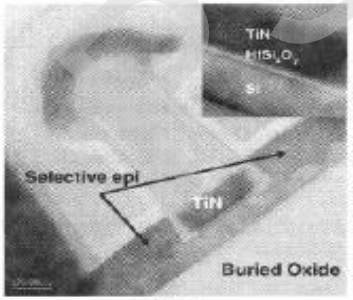


Fig. 1.

A. Vandooren et al. SOI conf 2005

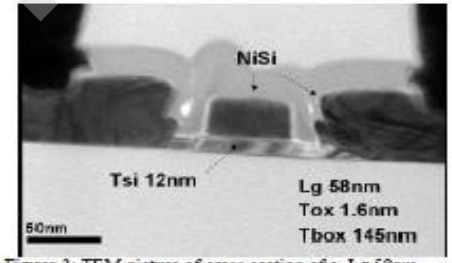


Figure 3: TEM picture of cross section of a Lg 58nm PMOS transistor

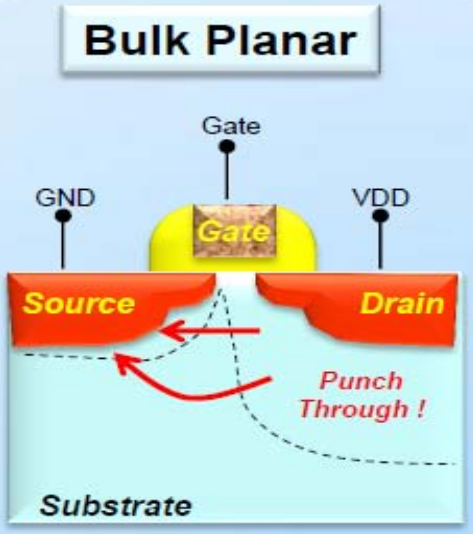
Fenouillet et. al, ESSDERC 2006

University of Sao Paulo

Planar option: UTBB FD SOI

FDSOI/UTBB Technology Benefits

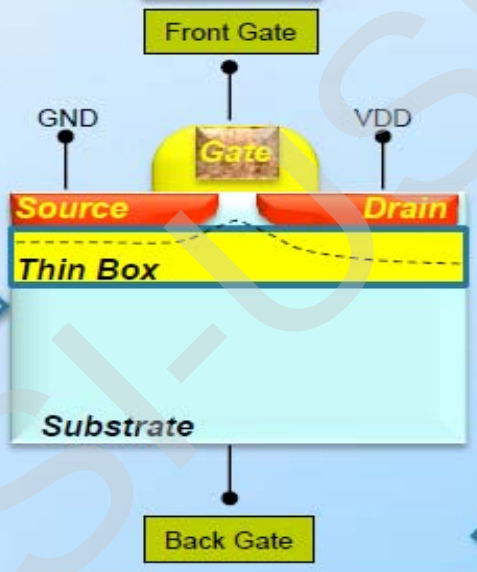
Bulk Planar



Electrostatic issues
☹ High Sub-VT slope
☹ High DIBL

Electrostatic issues
☹ Low Body Biasing Efficiency

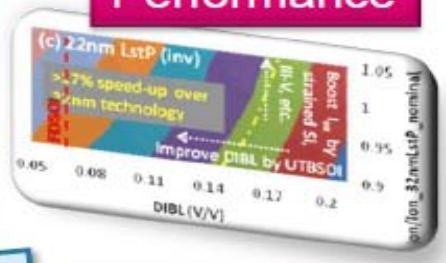
UTBB



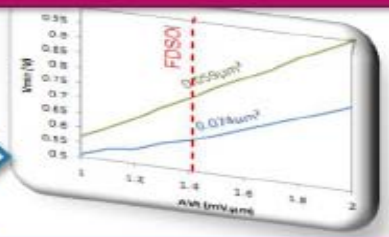
Electrostatic Recovery
☺Low Sub-VT slope
☺ Low DIBL

Back Gate Biasing scheme
☺ High Body Biasing Efficiency

Performance



Improved Variability



Design Flexibility

leti
life.augmented

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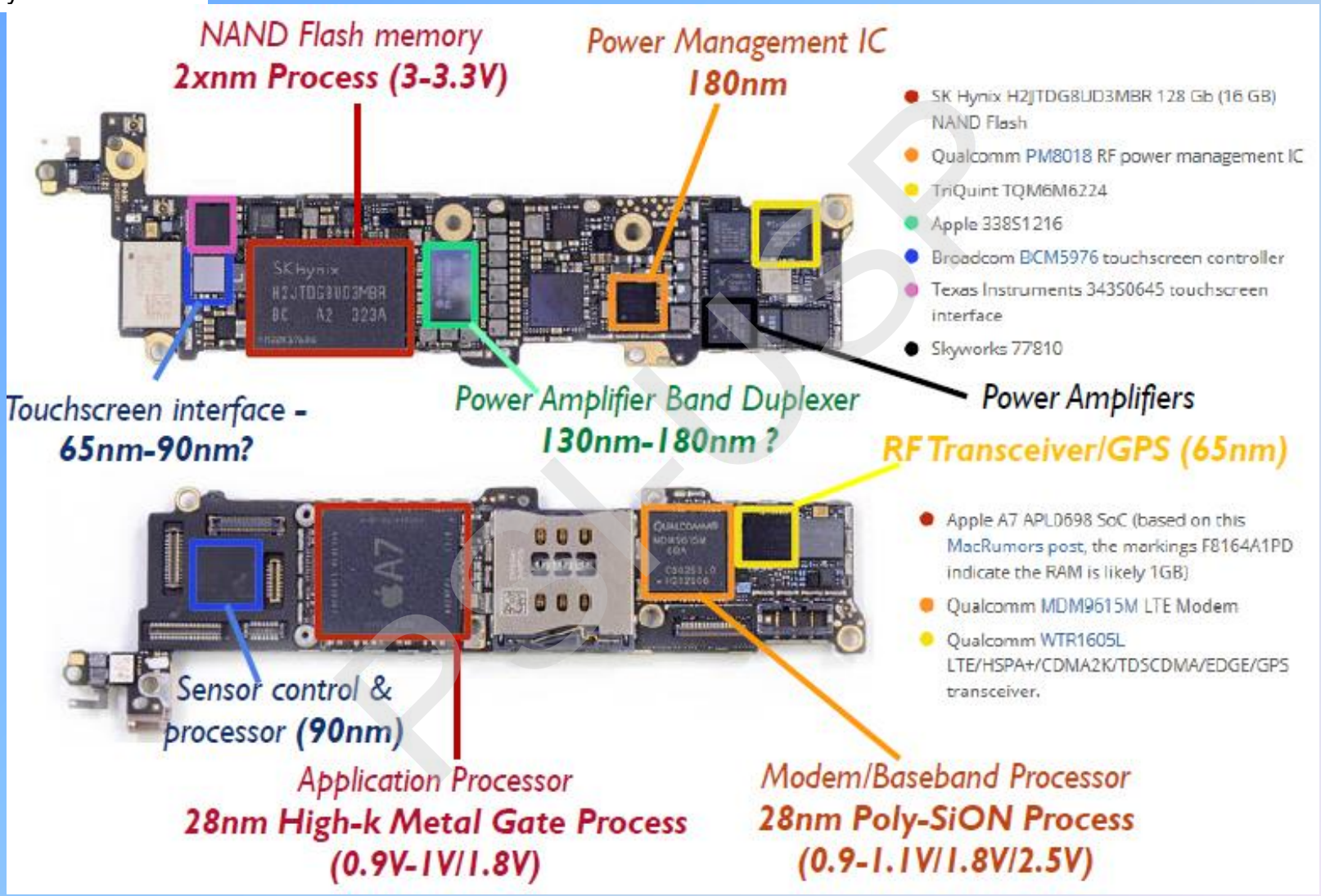
smart mobile applications
A mix of advanced and mature technologies



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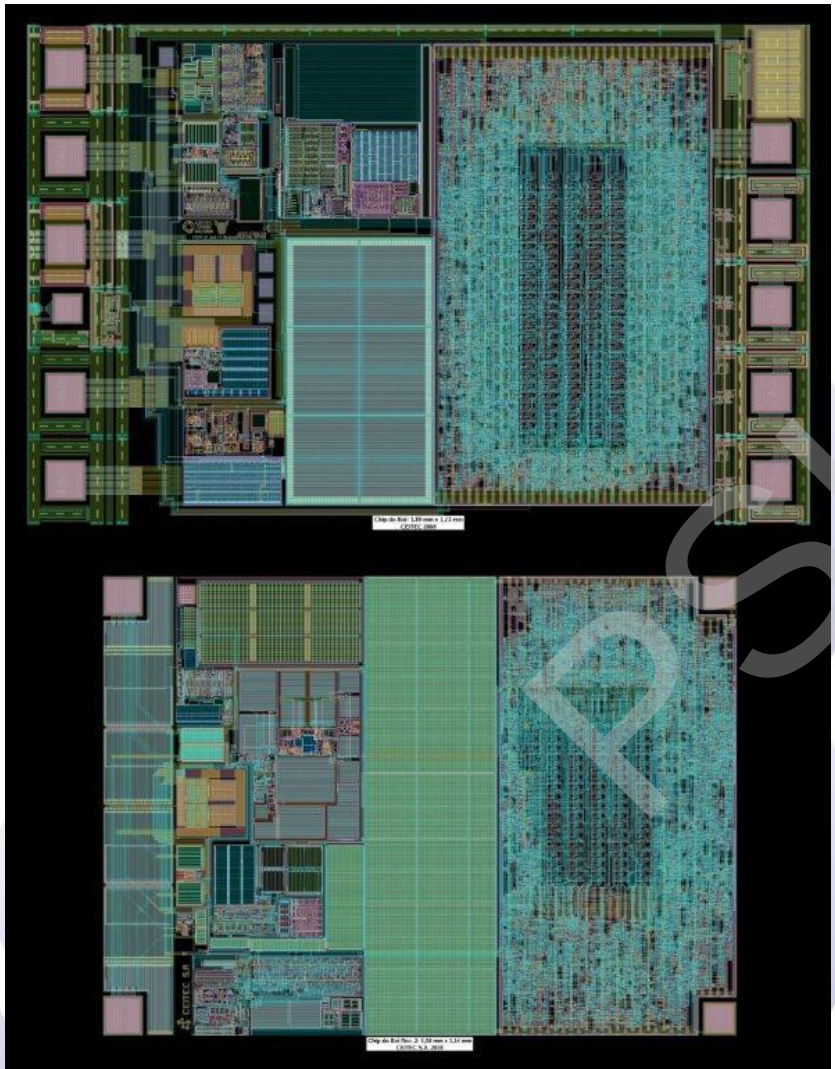
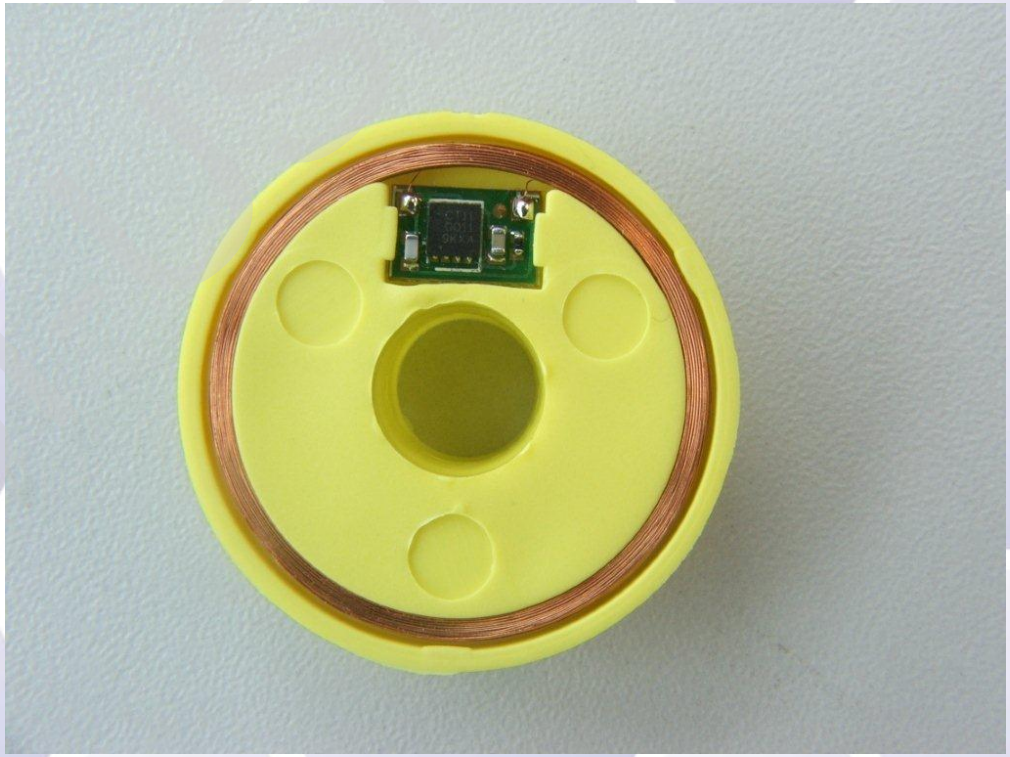
DH´s - Examples of IC's - CEITEC

- Chip do Boi – V1, CMOS 0,6 µm
- BNDES



- Brinco Chip do Boi

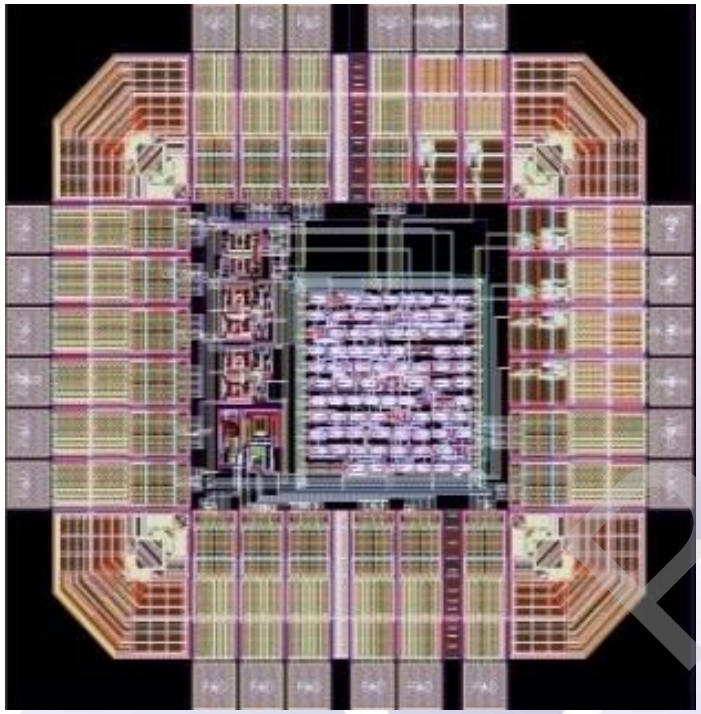
(Ox Chip Earring)

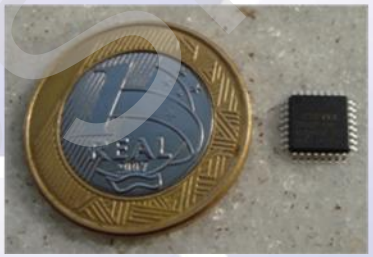


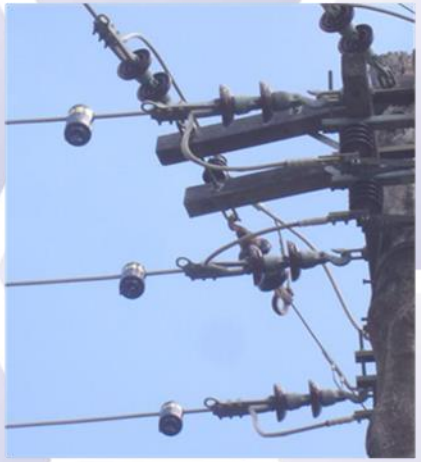
Universidade de São Paulo

DH´s - Examples of IC's - LSITec

1. Failure detector/signalizer on high-voltage transmission lines
   - CPFL

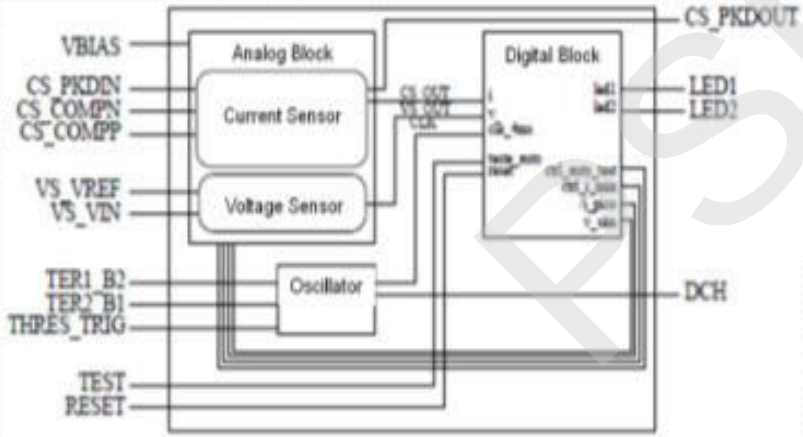




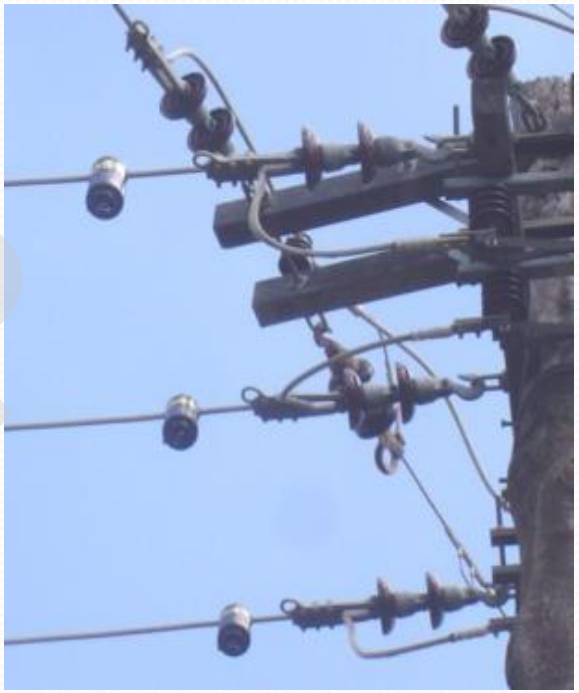


LSI-TEC – IC Design House
Projects in Production Stage

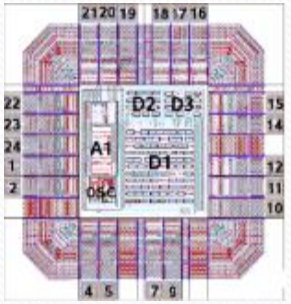
Customer	*CPFL/Expertise*
Design expertise	*Mixed mode, low voltage & low power*
Technology	*CMOS 0.6-micron*



Fault Signalyzer



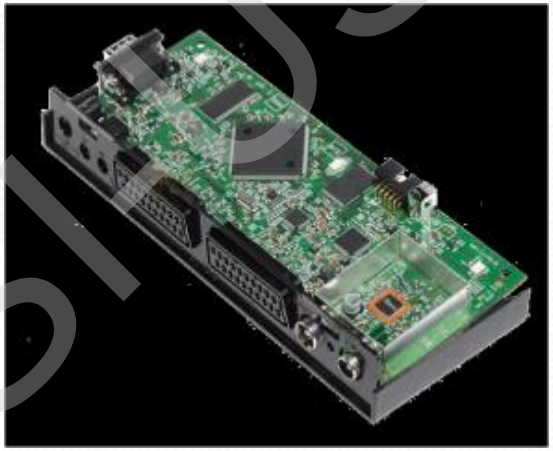
Fault Signalyzer instalation on Distribution network

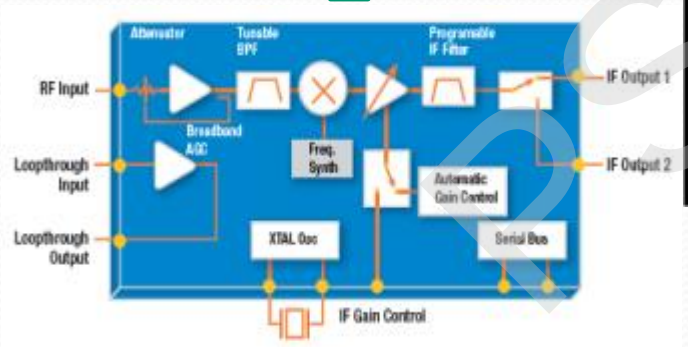


LSI-TEC – IC Design House
Projects in Production Stage

Customer	*Entropic (USA)*
Design expertise (1M+ transistors)	*VLSI digital design*
Technology	*CMOS 0.18-micron*

Set Top Box





Silicon Tuner

Standards :

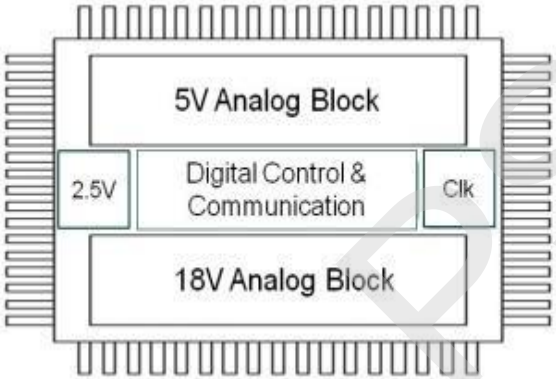
- ATSC (Revision C) and A/74
- NorDig Unified version 1.0.3
- OpenCable
- DVB-C
- DVB-T
- ISDB-T
- NTSC
- PAL
- SECAM
- DOCSIS 2.0
- DTMB

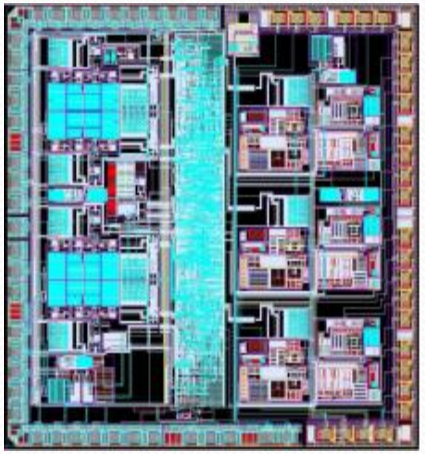
LSI-TEC – IC Design House
Projects in Production Stage

Customer	*Treetech*
Design expertise	*Mixed-signal, high voltages)*
Technology	*CMOS 0.6-micron*

Industrial instrumentation & Distribution network and transformer monitoring

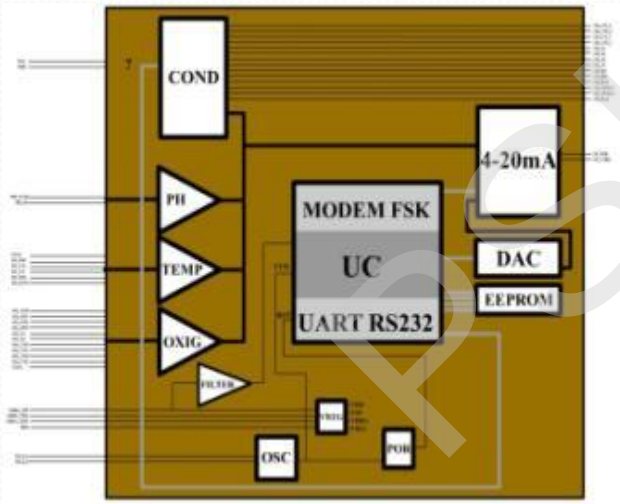
Digitally configurable multi-instrumentation controller





LSI-TEC – IC ASIC & FPGA Design House
Projects in Development

Customer	*Digimed*
Design expertise	*Mixed-signal, low voltages, low power*
Technology	*CMOS 0.6-micron*
Dev Status	*Eng. Samples*

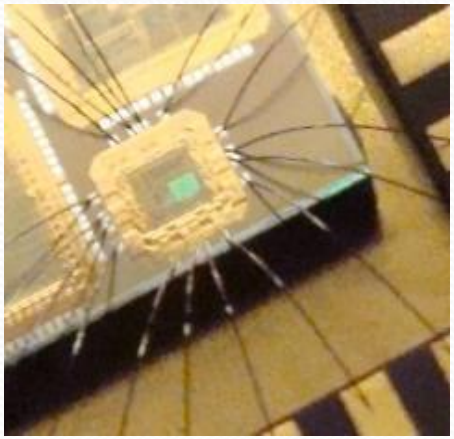


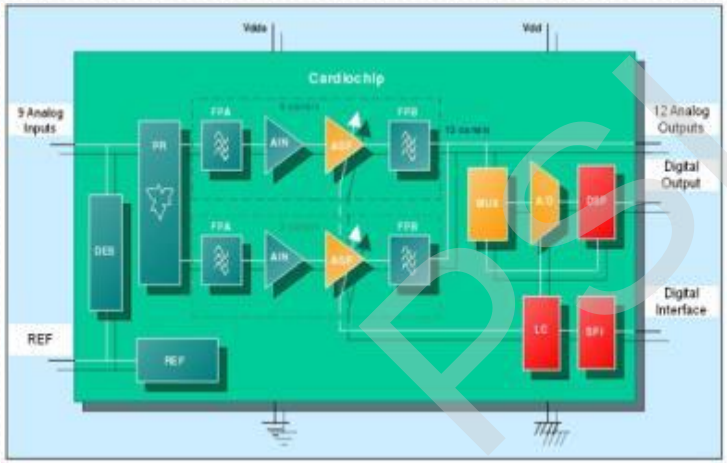
Test Prototype(PCB)

Sensors:
- PH
- Oxigen
- Temperature
- Conductivity

LSI-TEC – IC Design House
Projects in Development

Customer	*CardioWeb*
Design expertise	*Mixed-signal, low voltages, low power*
Technology	*CMOS 0.35-micron*
Dev Status	*Near Tape-out*

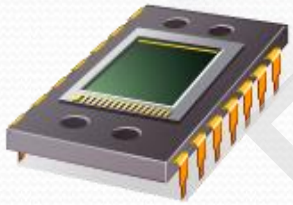




- Portable, low cost ECG monitors up to 12 channels
- Remote diagnostic
- Cost Reduction for Public health.

LSI-TEC – IC Design House
Projects in Development

Customer	*Confidential*
Design expertise low power	*very low voltages,*
Technology	*CMOS 0.18-micron*
Dev Status	*Specification*



Under Development chip

Transceiver chip IEEE 802.15.4 Standard / ZigBee

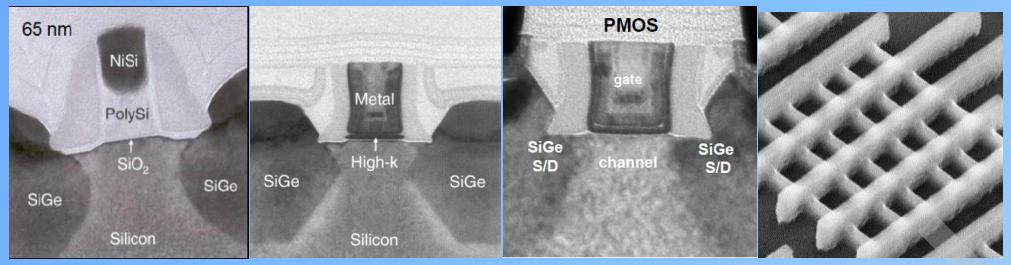
Industrial, medical and home sensors networks applications

More Moore to More More Moore

Technology node

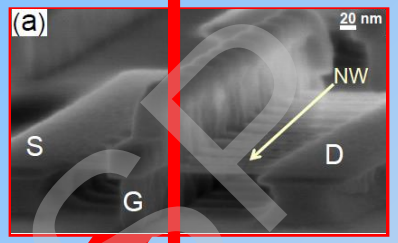
65nm | 45nm | 32nm | 22nm

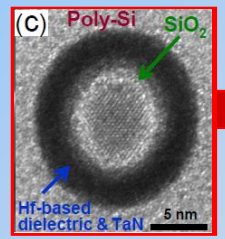
L_g 35nm | L_g 30nm



Now | Future

14nm | 10nm, 7nm, 5nm, 3.5nm



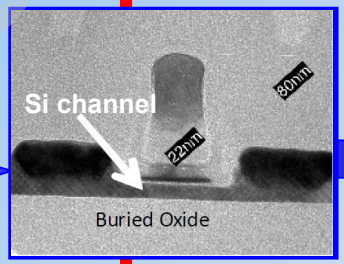


Main stream
(Fin,Tri, Nanowire)

Si

Planar

Tri-Gate



Alternative

(FDSOI)

FD: Fully Depleted

Others

Alternative (III-V/Ge) Channel FinFET

Emerging Devices (TFETs…)

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)

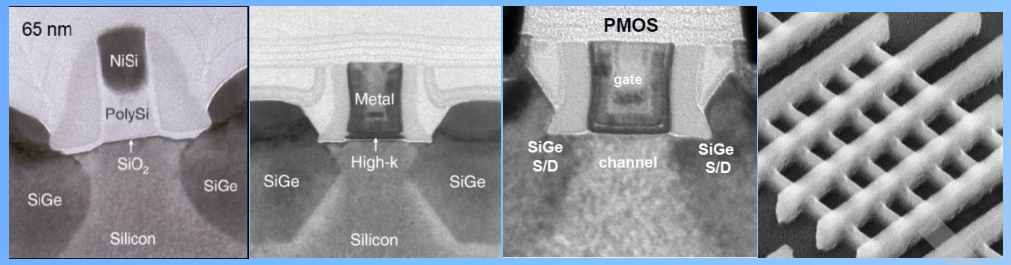
* Hiroshi Iwai

More Moore to More More Moore

Technology node

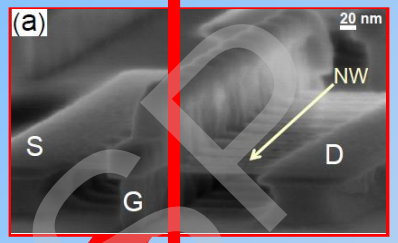
65nm | 45nm | 32nm | 22nm

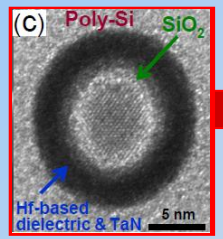
L_g 35nm | L_g 30nm



Now | Future

14nm | 10nm, 7nm, 5nm, 3.5nm





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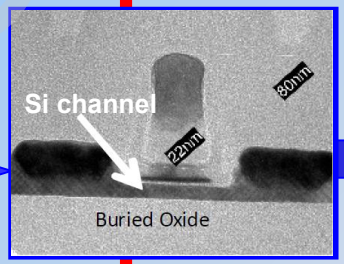

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T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)

* Hiroshi Iwai

University of Sao Paulo

Scaling and power crisis

MOSFET: Drift-Diffusion conduction mechanism (>60mV/dec)

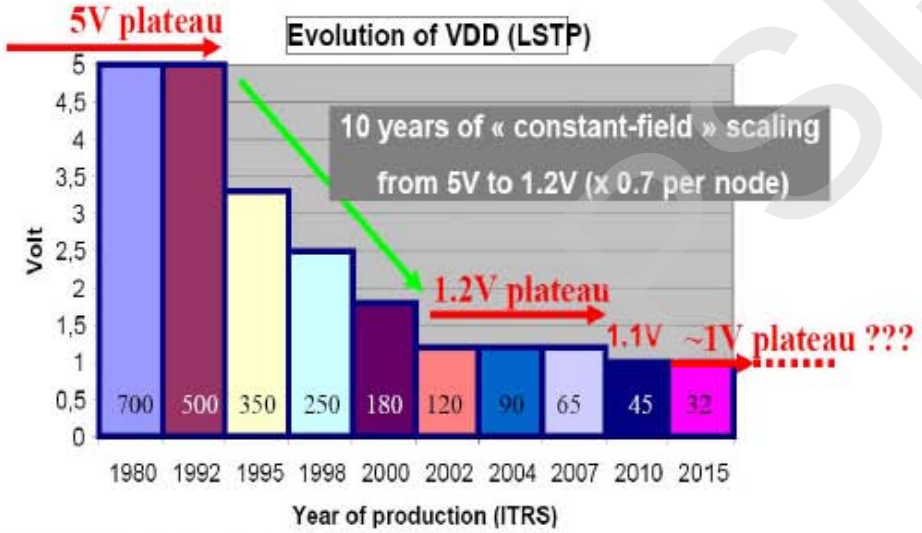
$$P_{total} = P_{dynamic} + P_{static}$$

$P_{dynamic}$: Power dissipated during switching $\sim C_{total} V_{dd}^2 f$

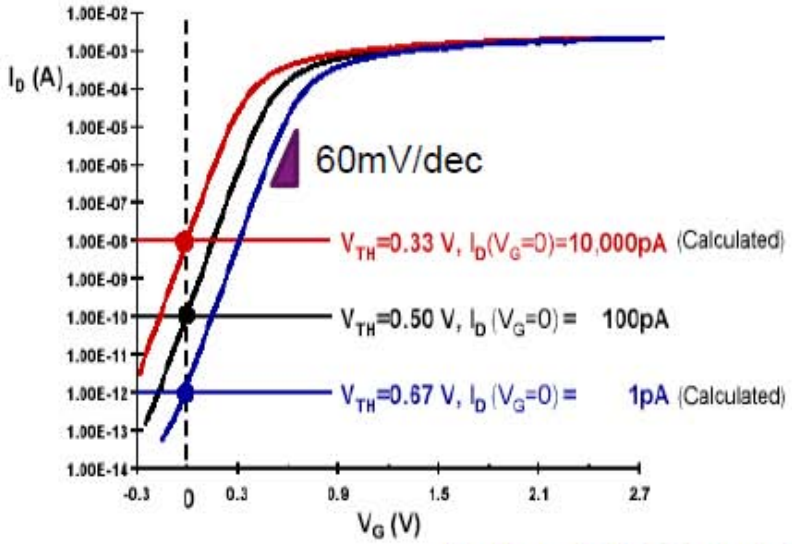
P_{static}: Power dissipated due to leakage of imperfect switch $\sim I_{off} V_{dd}$

Need of

New OPERATION PRINCIPLE



W.Kuzmicz, IDESA tutorial, 2007



D. Cox, IRPS Tutorial 2004

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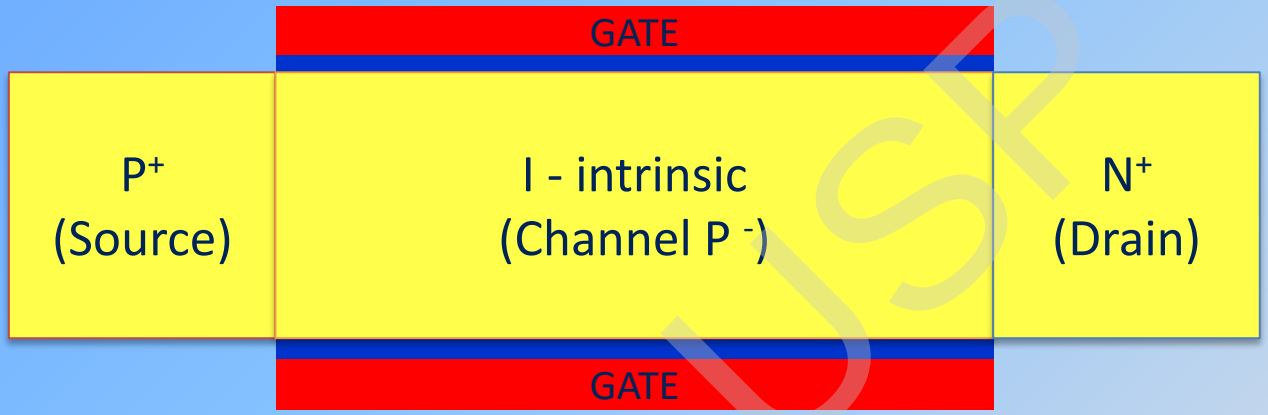
TFET

Tunnel Field Effect Transistor - nTFET



- Based on PIN Diode technology;
- Reduced short-channel effects,
- Lower subthreshold swing;
  -
  -

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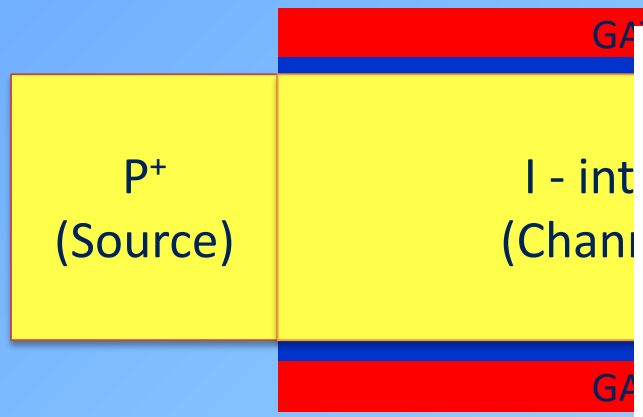
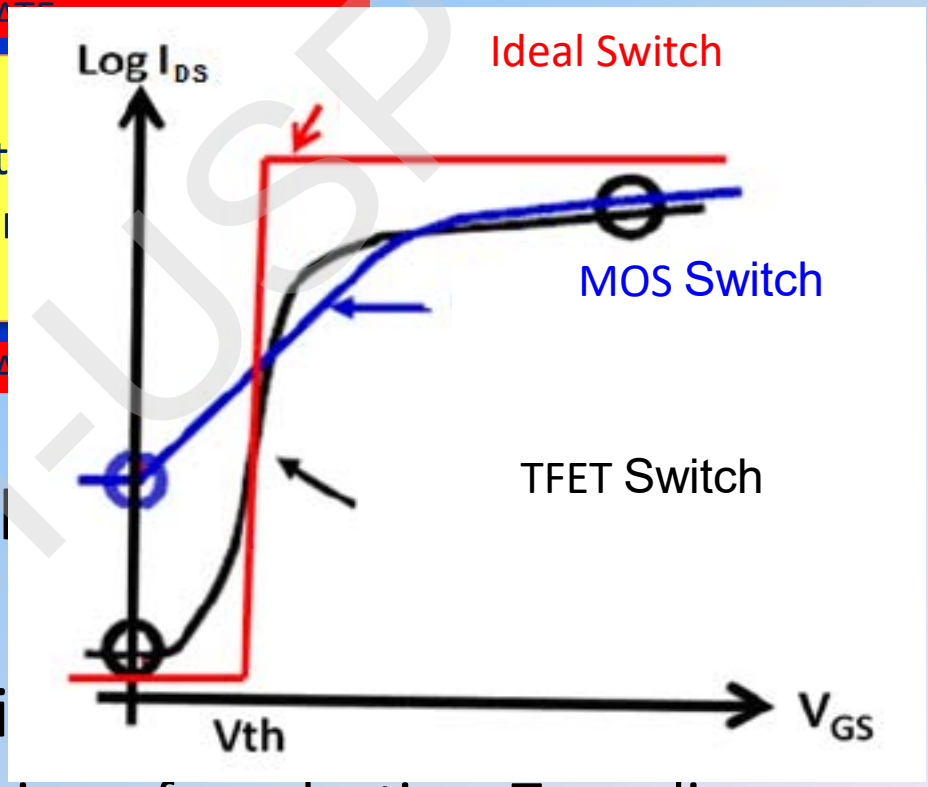
TFET

Tunnel Field Effect Transistor - nTFET





- Based on PIN Diode tec
- Reduced short-channel
- Lower subthreshold swi
  - Due to different mechanism of conduction: Tunneling;
  - May be less than 60 mV/dec.

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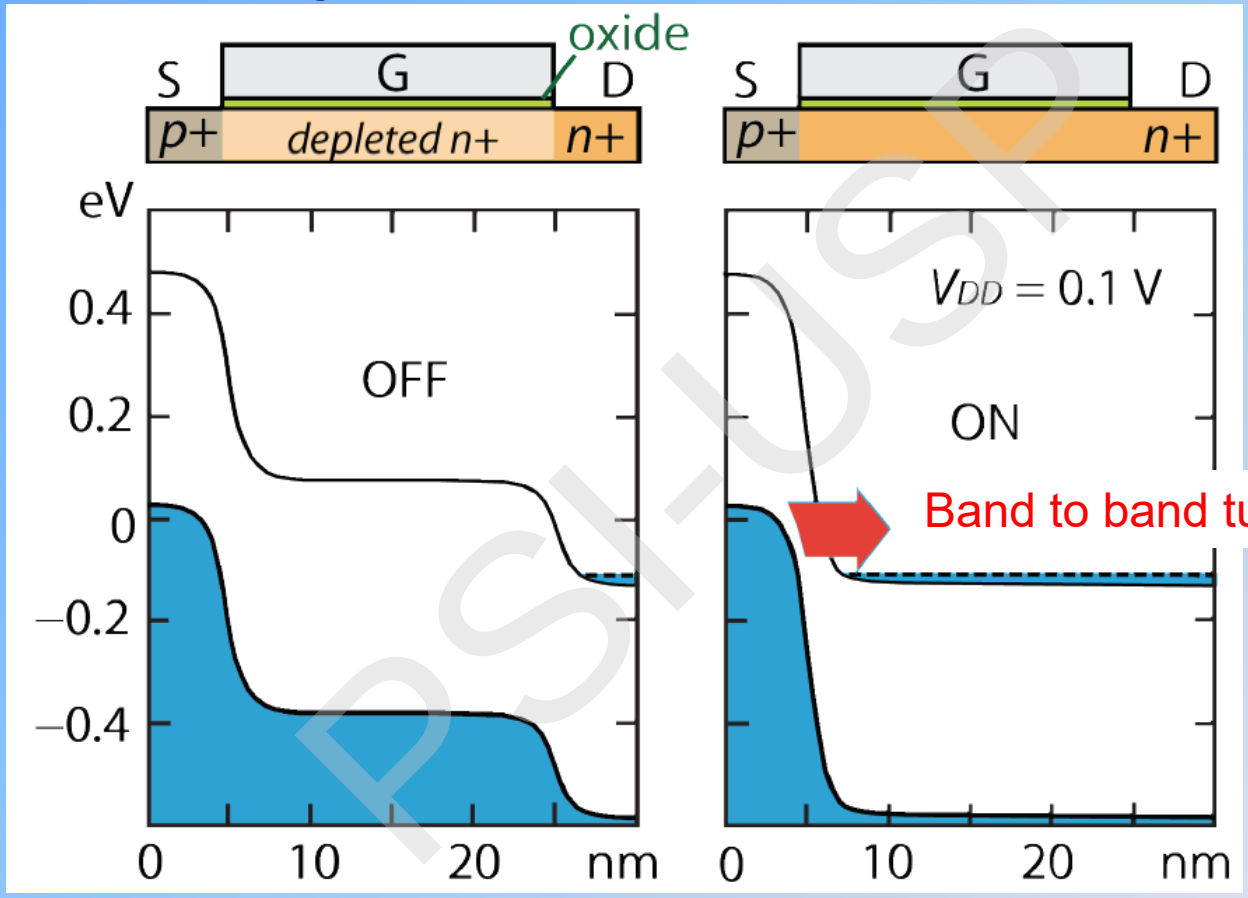
nTFET

OFF
$V_G = 0V$

ON
$V_G > 0V$

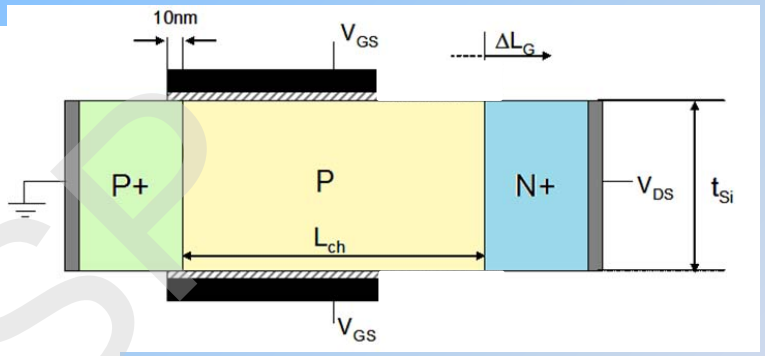


Low I_{OFF}, Low V_{DD}, SS<60mV/decade

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

University of Sao Paulo

Channel/Drain Underlap



78mV/dec

46 mV/dec

Underlap ↑

I_{ON} is not influenced

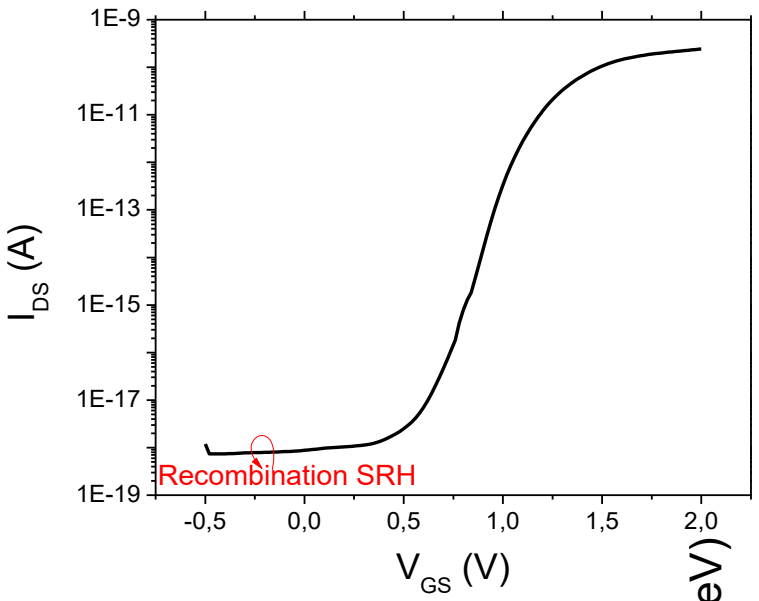
I_{OFF} ↓

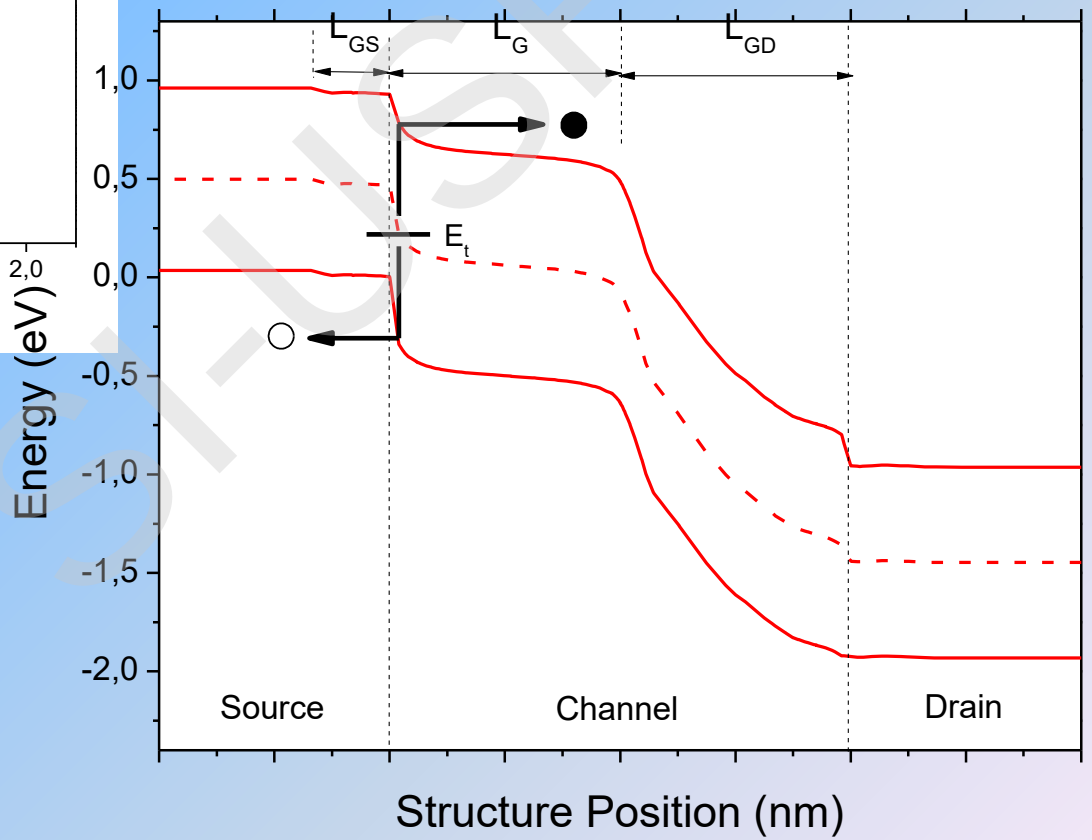
I_{ON}/I_{OFF} ☺

SS ☺

*Agopian, P.G.D., et all – SSE 2012

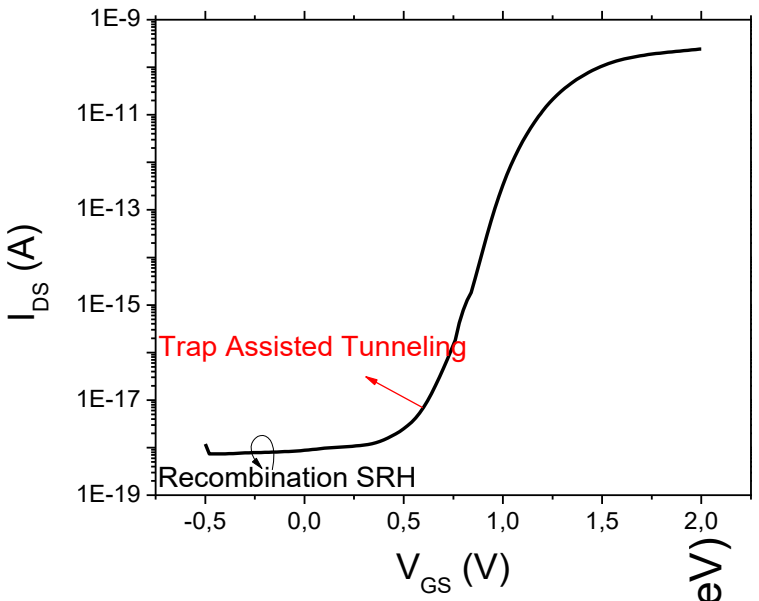
Conduction Mechanism

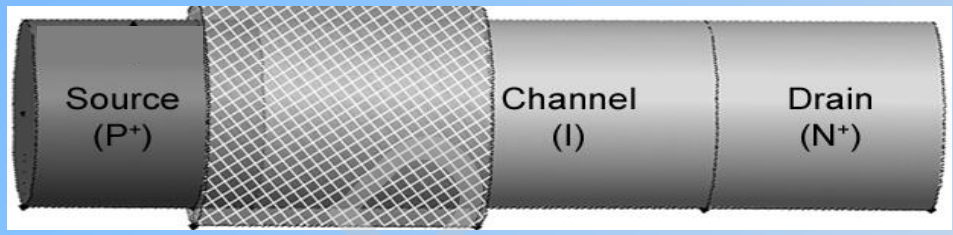




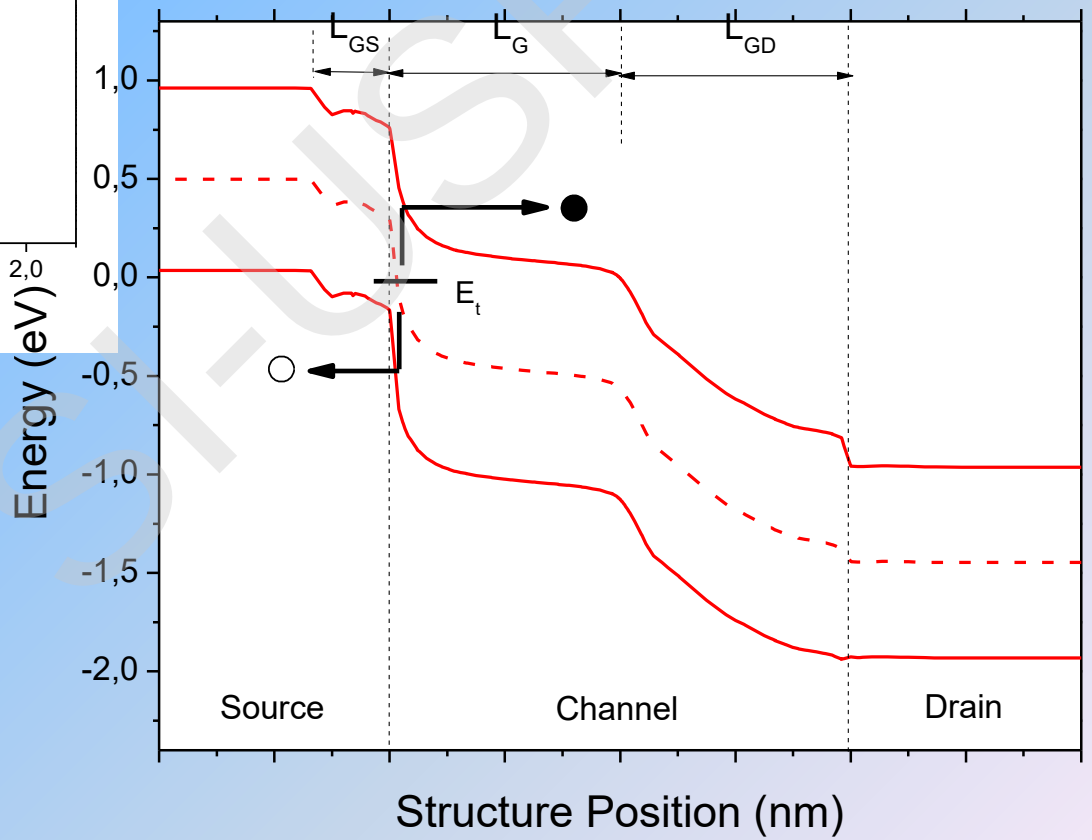
$$J_{SRH} \propto C_1 . e^{\left(-\frac{\frac{E_g}{2}+\Delta E_t}{k.T}\right)}$$

Conduction Mechanism

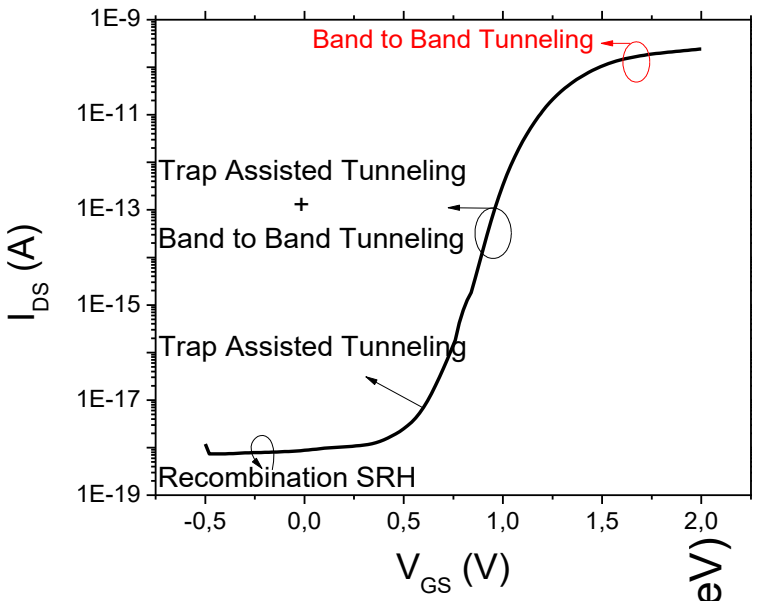


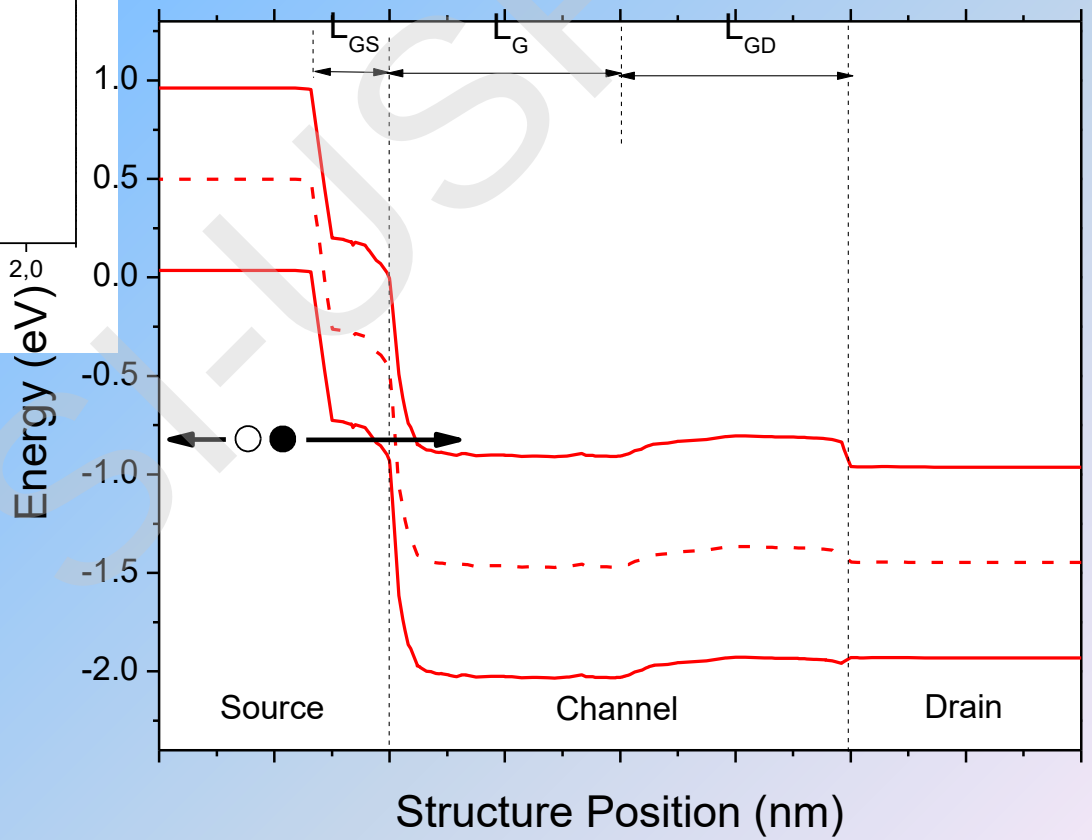


$$J_{TAT} \propto C_2 . e^{\left(-\frac{\frac{E_g}{2}+\Delta E_t}{k.T}\right)}$$



Conduction Mechanism





$$J_t \propto e^{\left(-C_3 \cdot \frac{Eg^{3/2}}{\xi}\right)}$$

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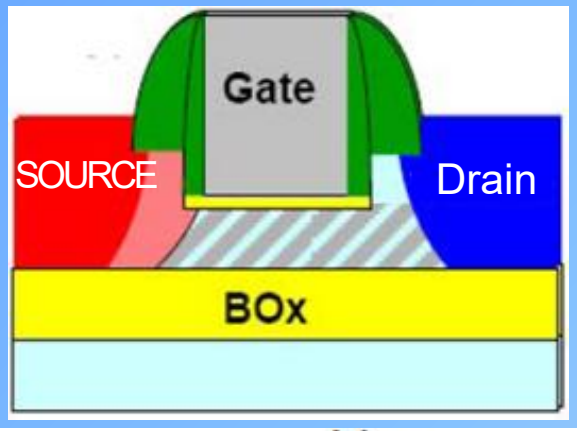
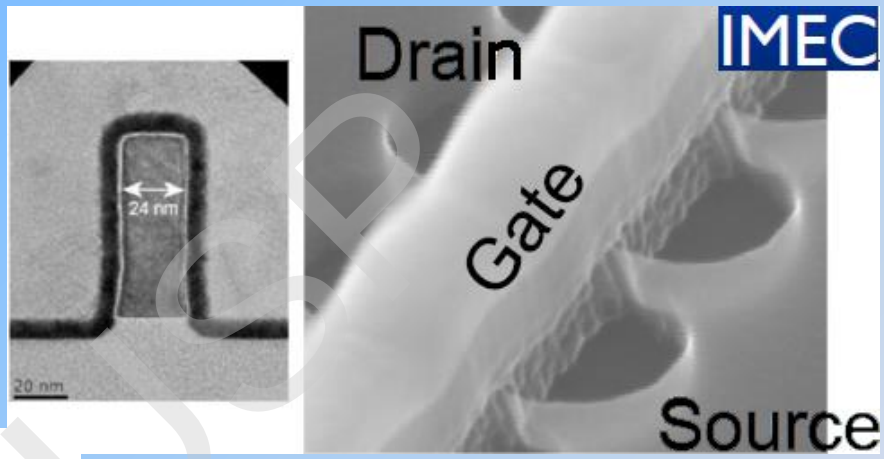
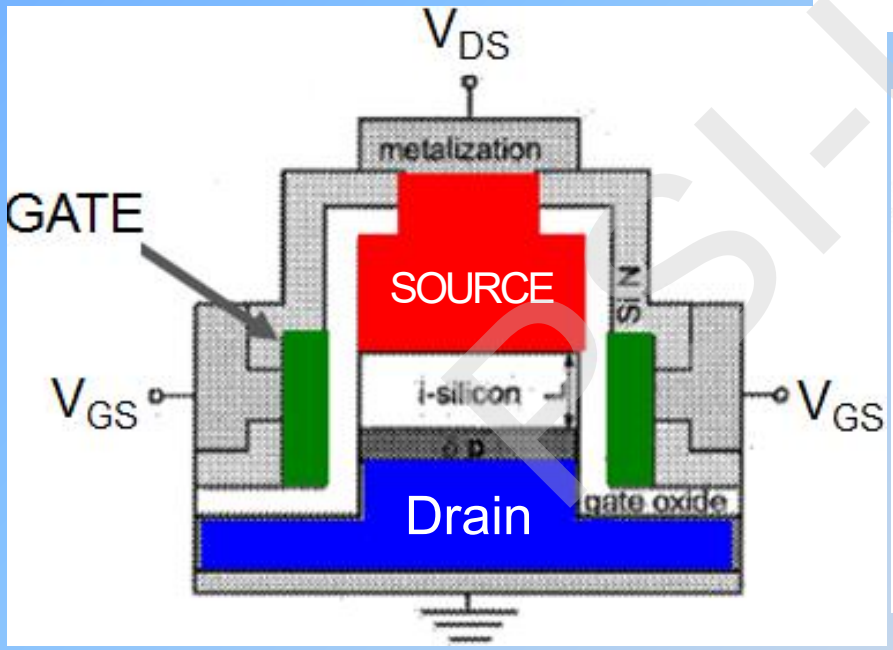
TFET

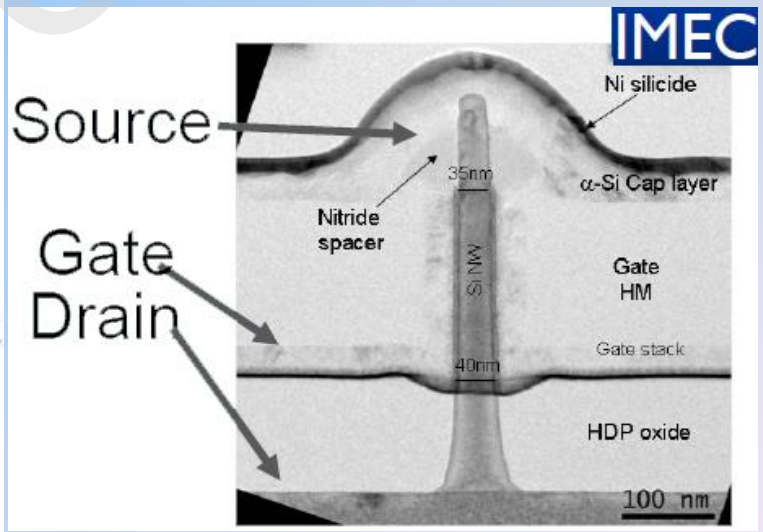
Horizontal





Vertical





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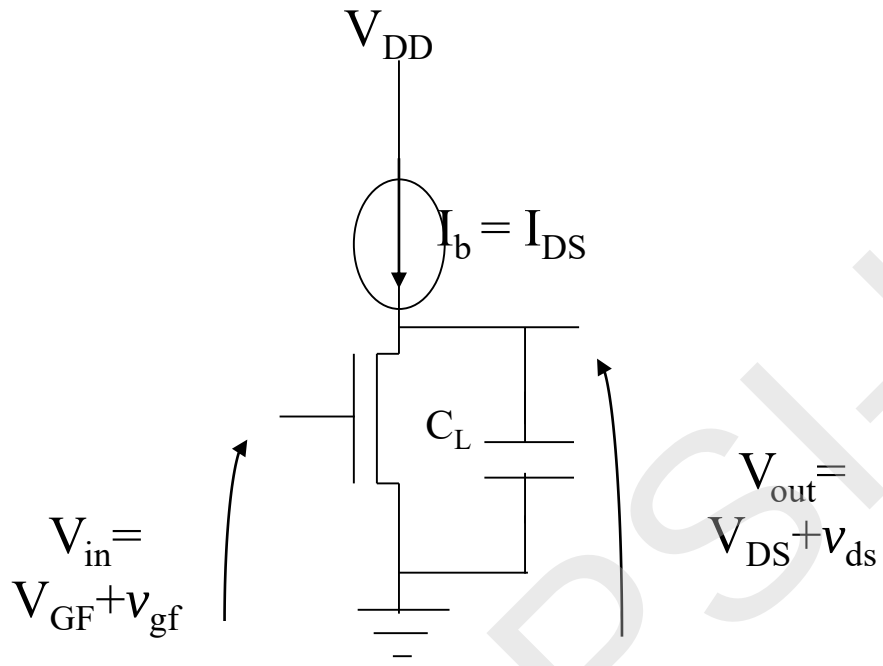
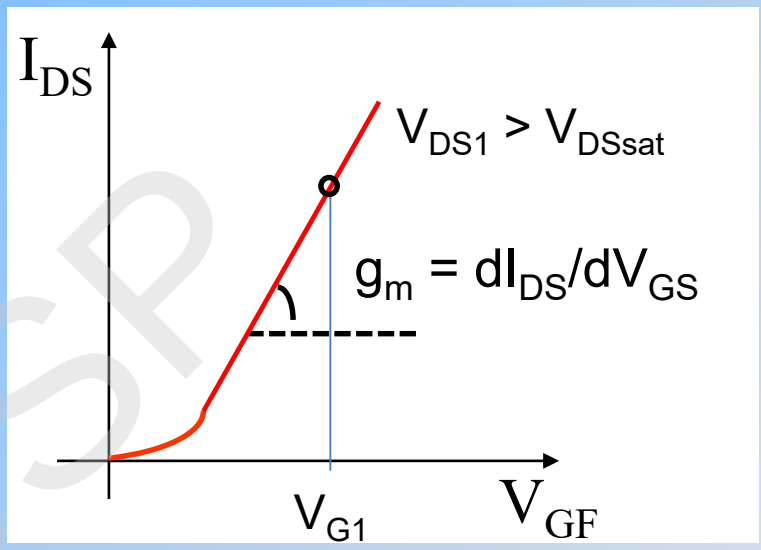
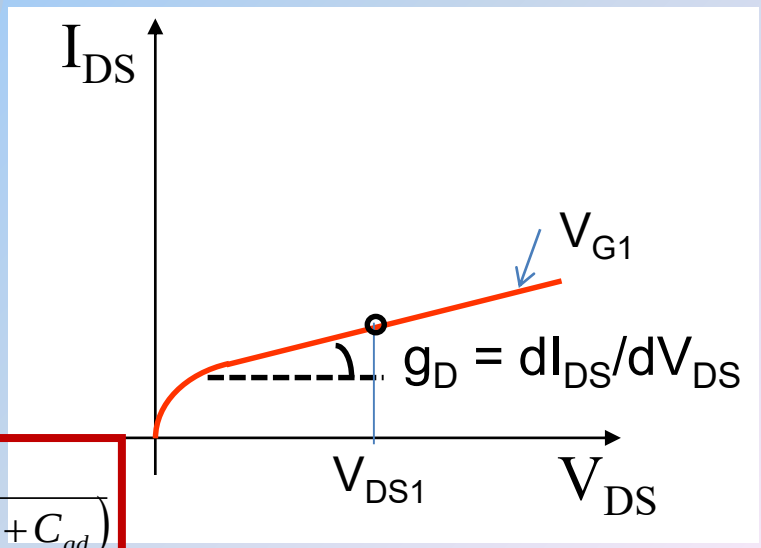
Analog Performance

Single-Transistor Amplifier







$$|A_V| = \frac{V_{ds}}{V_{gf}} = \frac{g_m}{g_D} = \frac{g_m}{I_{ds}} \cdot V_{EA} \qquad f_T = \frac{gm}{2 \cdot \pi \cdot (C_{gs} + C_{gd})}$$

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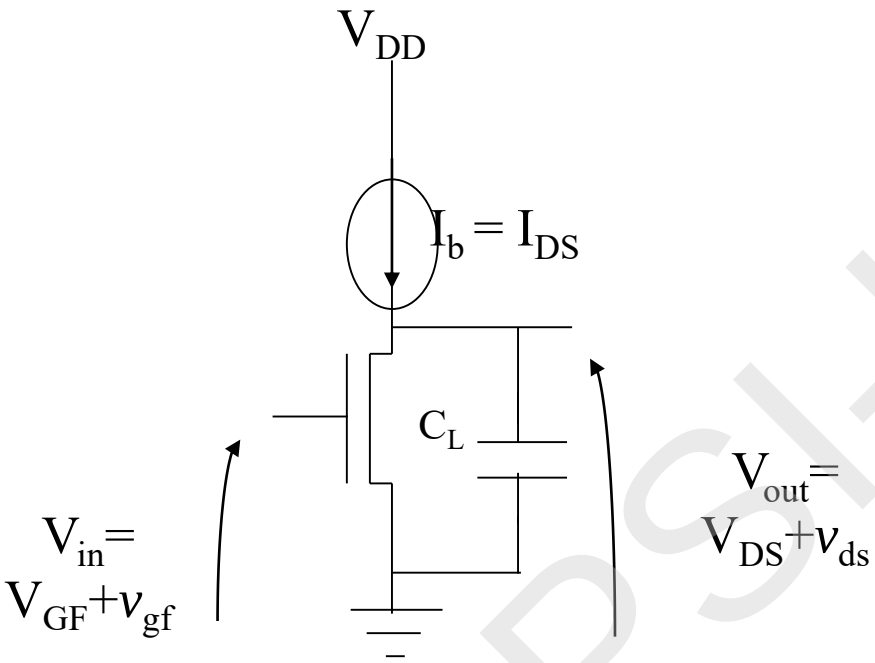
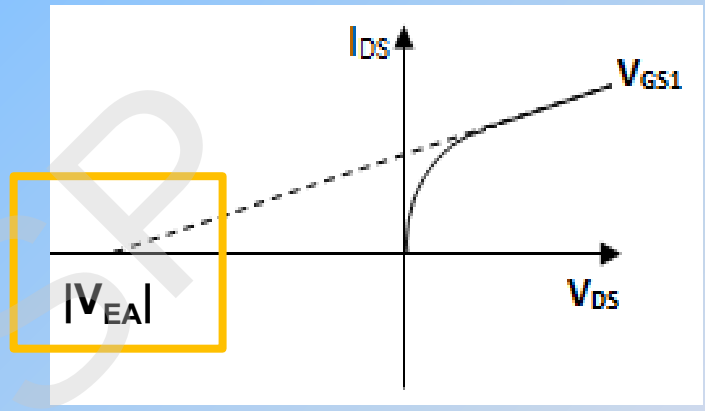
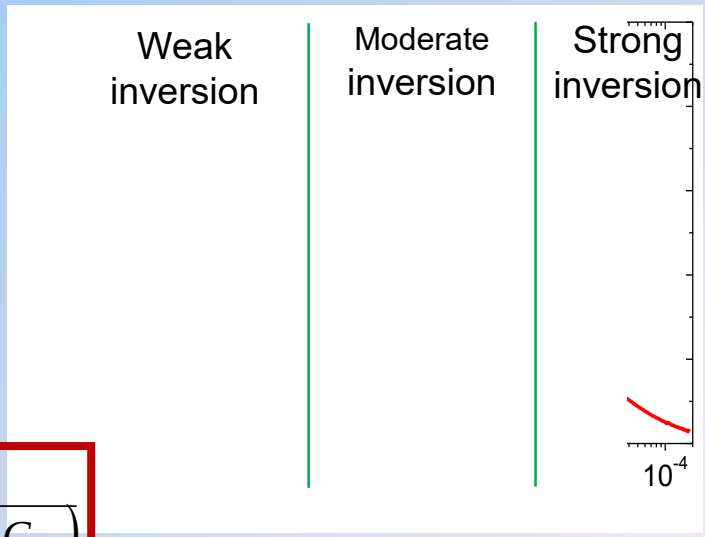
Analog Performance

Single-Transistor Amplifier







$$|A_V| = \frac{V_{ds}}{V_{gf}} = \frac{g_m}{g_D} = \frac{g_m}{I_{ds}} \cdot V_{EA}$$

$$f_T = \frac{gm}{2 \cdot \pi \cdot (C_{gs} + C_{gd})}$$

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Description of Devices

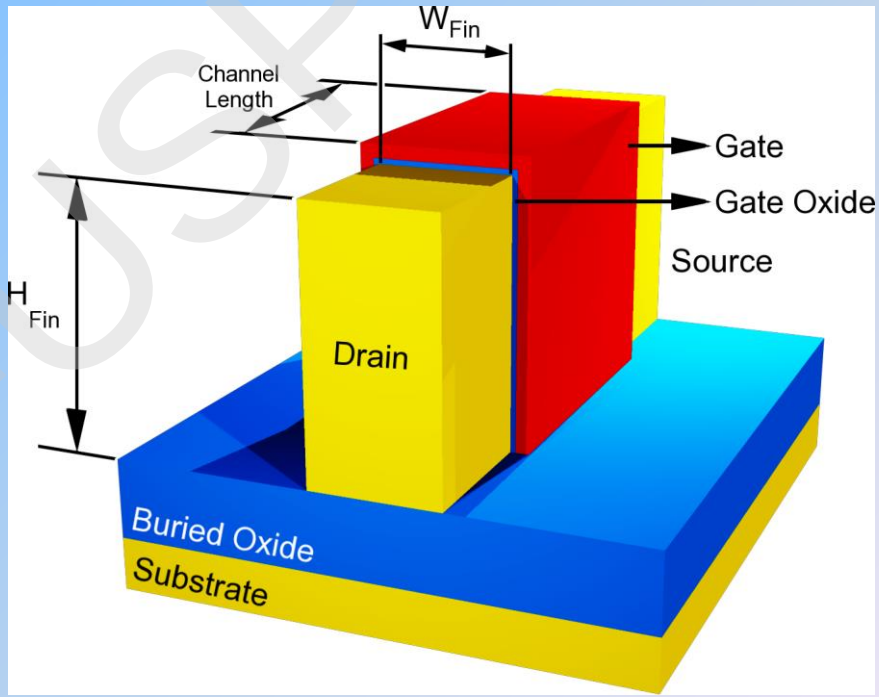
Fabricated at IMEC, Belgium

Triple Gate MuGFETs

Undoped channel
($N_A = 1x10^{15}\ cm^{-3}$)

Physical dimensions:

H_{Fin} = 65 nm
Gate oxide = HfO_2(2nm) + SiO_2(1nm)
t_{box} = 145 nm
L = 250 nm
W_{Fin} = 40nm and 250nm



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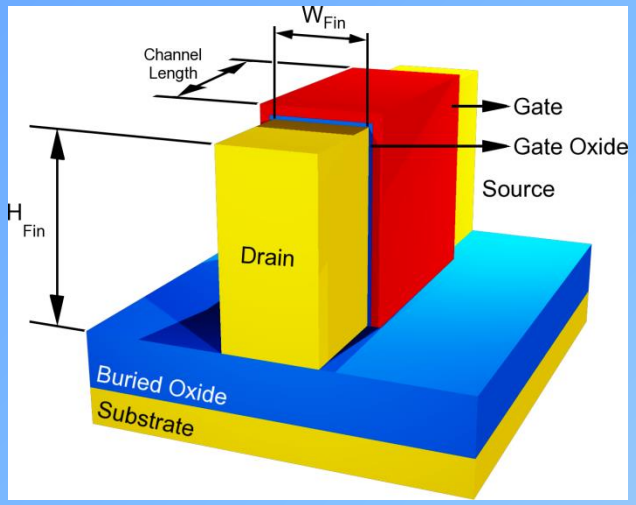
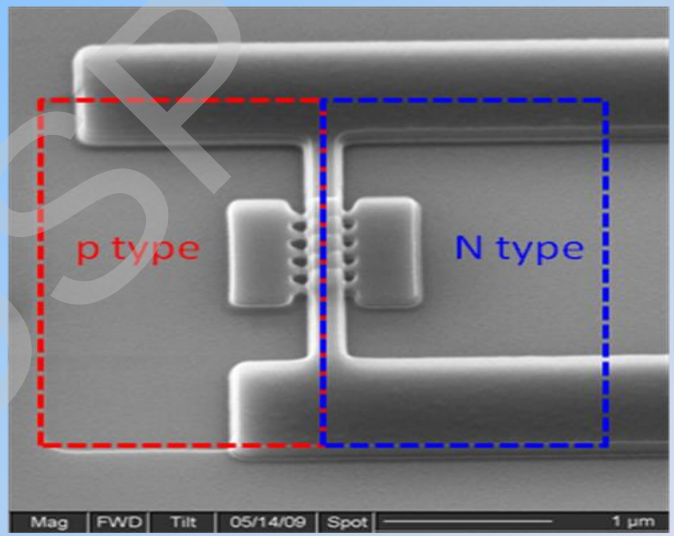
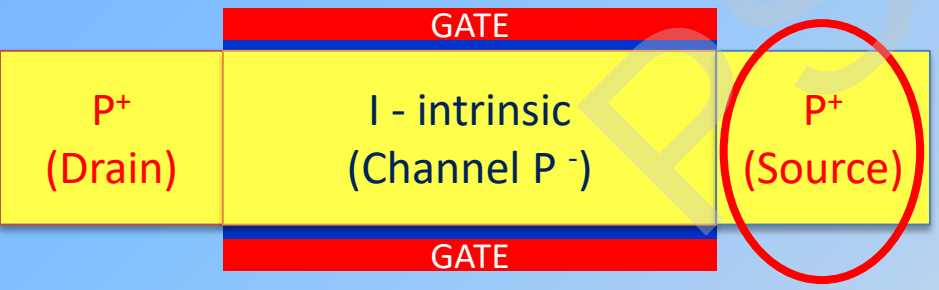
Analog Performance

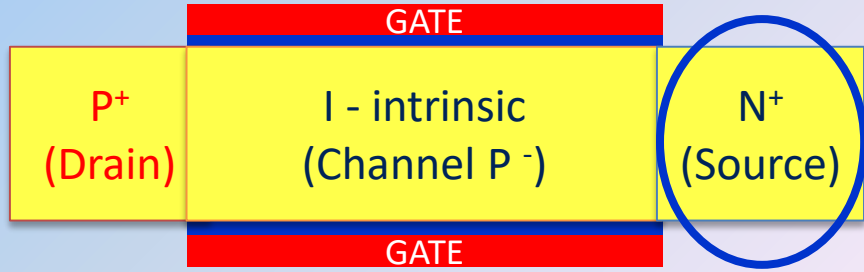
pFinFET



pTFET







* Agopian et al, *Trans. Elec. Dev.*, 2012

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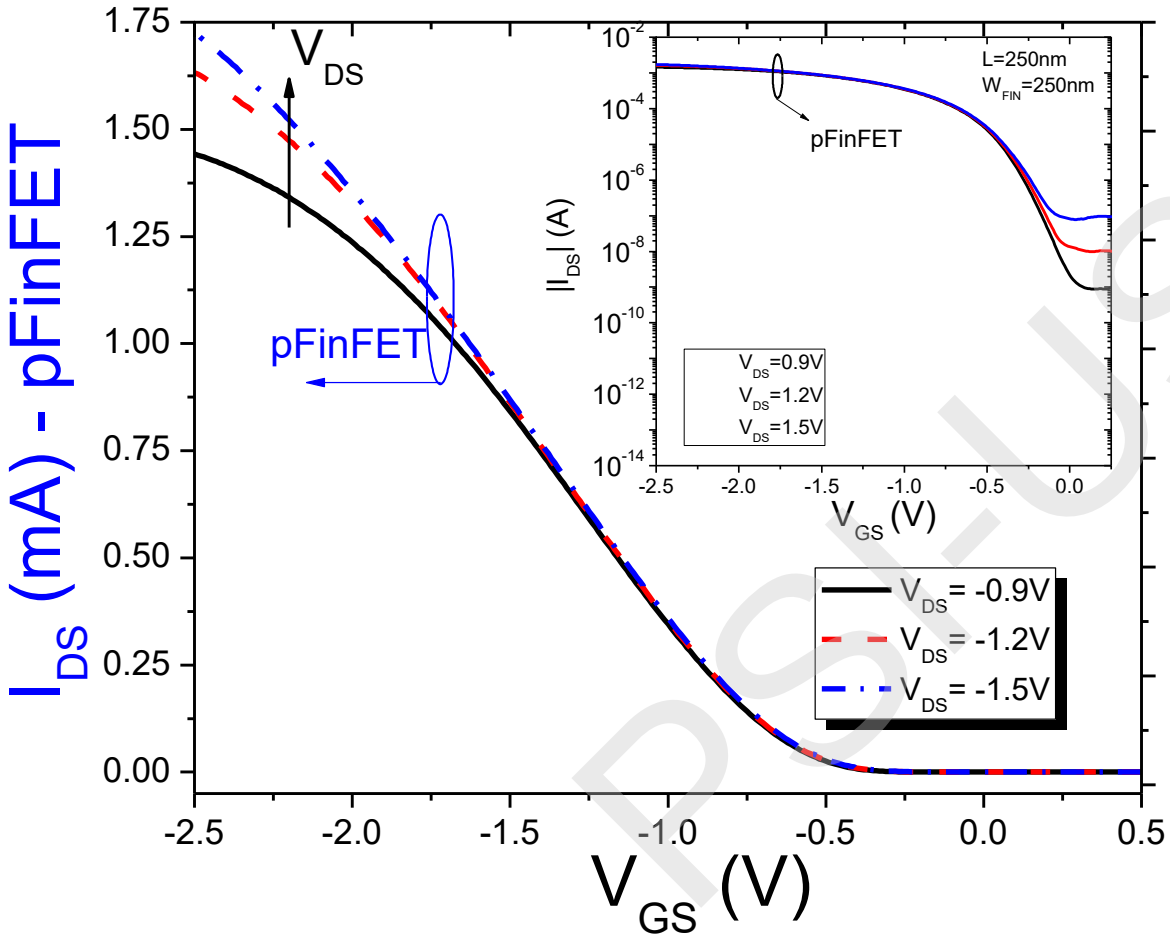
Drain Current



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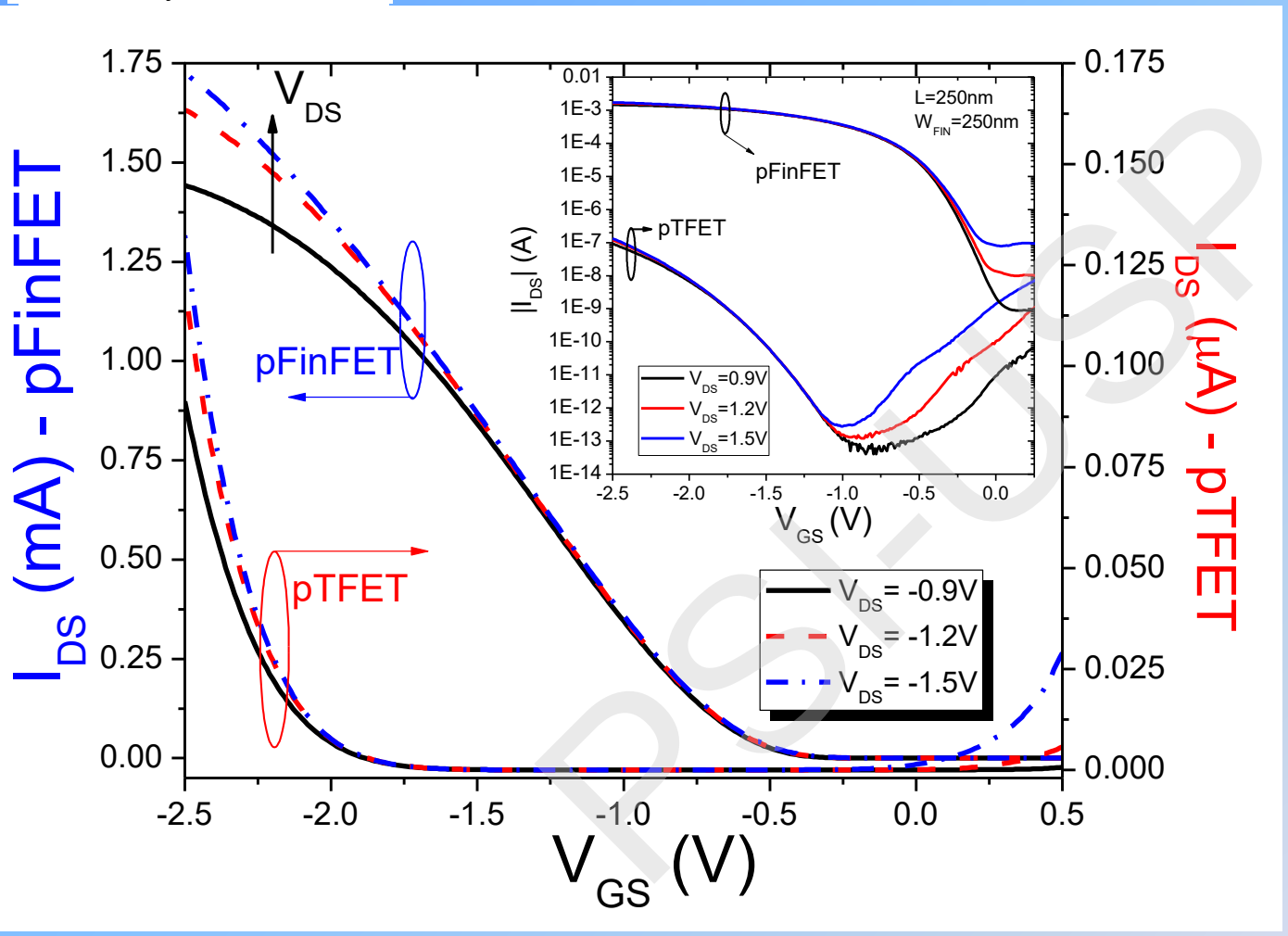
Drain Current



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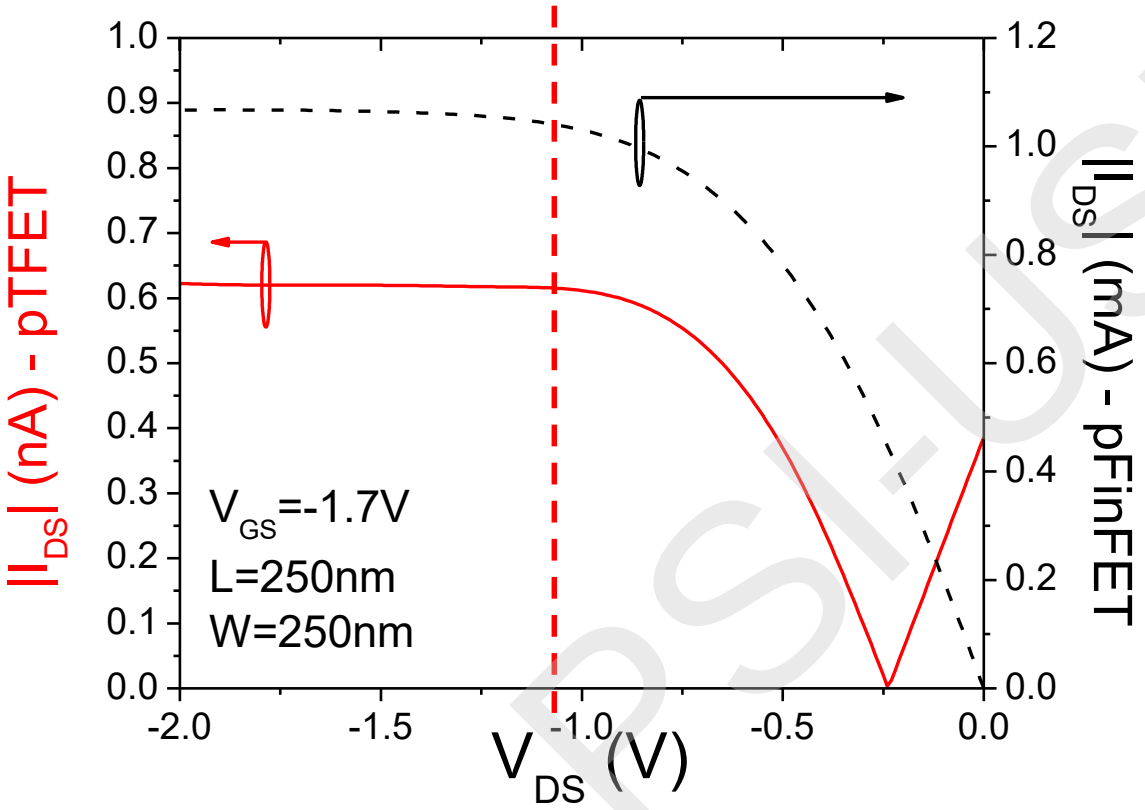
Drain Current



Both TFET and FinFET reach the "saturation" region almost at the same V_{DS} (≅-1.1V)

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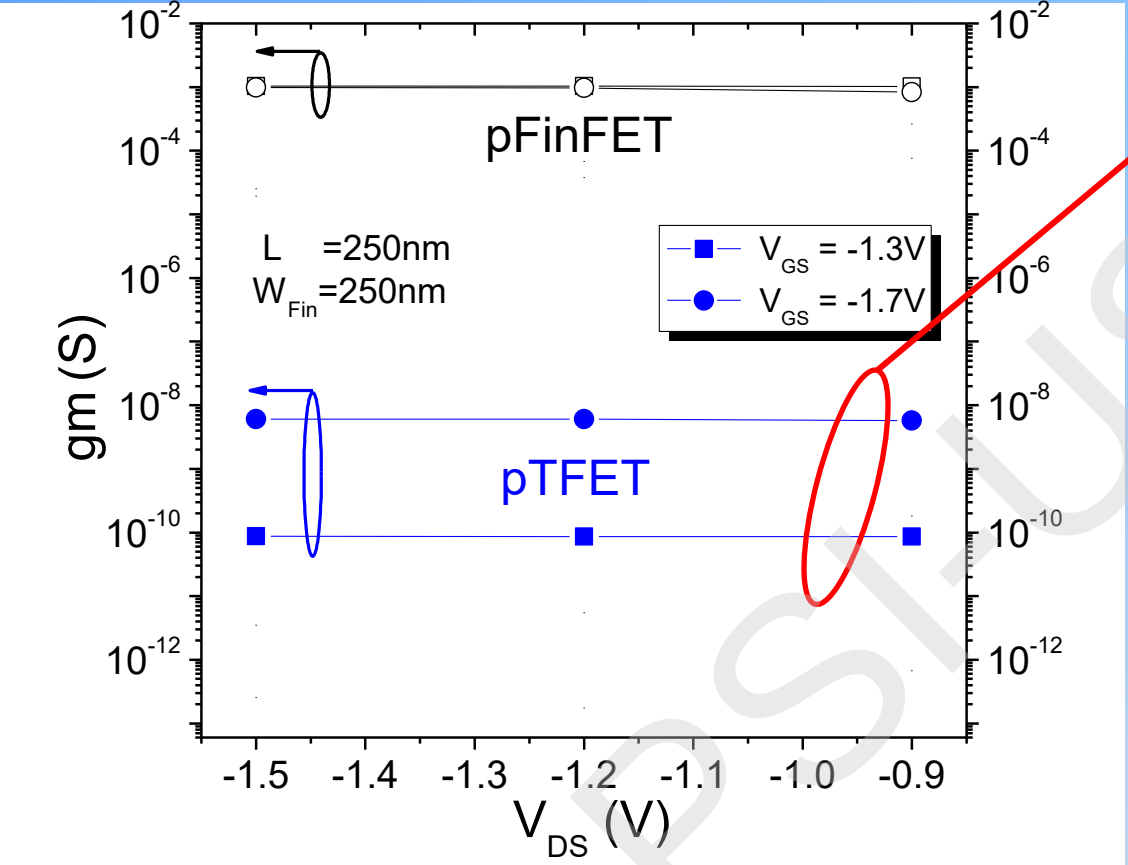
Transconductance



Strong influence of V_{GS} on gm

⇩

direct dependence of the tunneling current at the source/channel junction with V_{GS}

gm_{pTFET} << $gm_{pFinFET}$

gm: FinFET better than TFET

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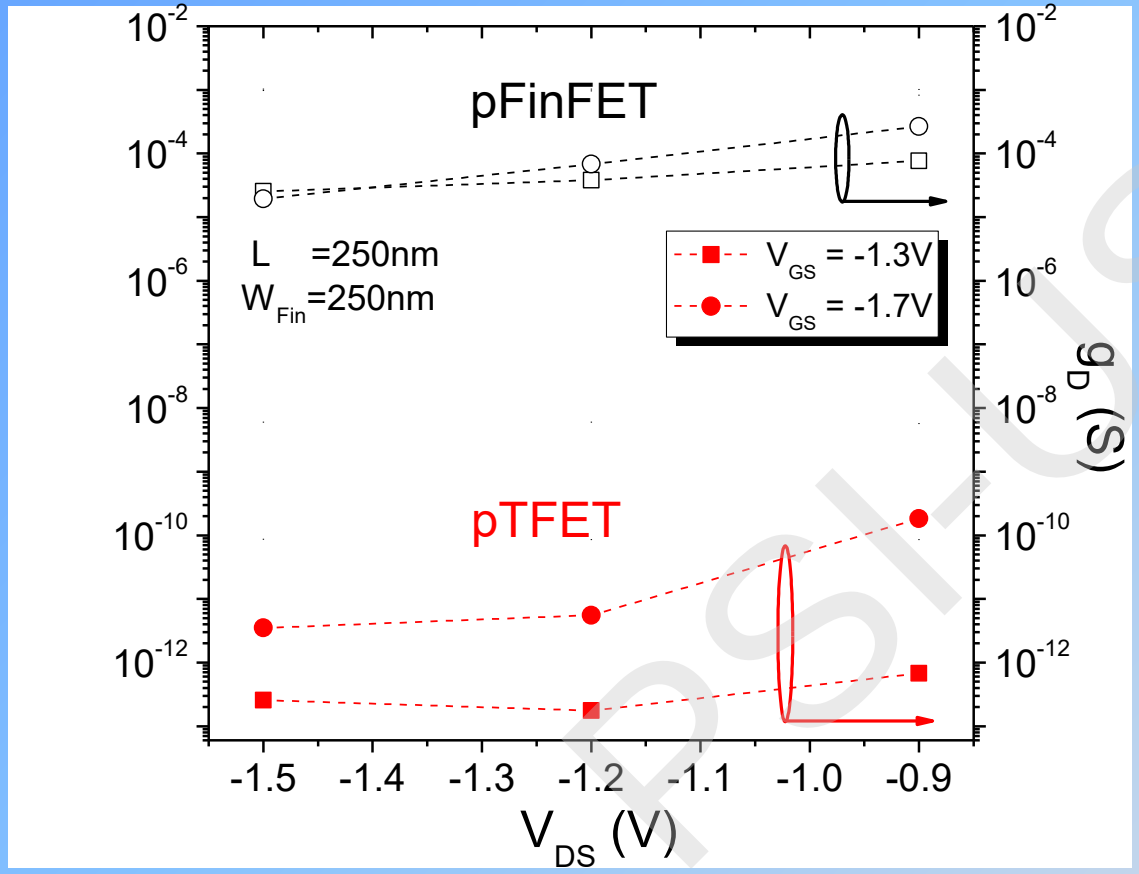
Output Conductance



TFET
Lower influence of V_{DS} on g_D

(no influence on tunneling mechanism excepted on DIBT)

g_D: TFET better than FinFET

g_D for pTFETs is at least 6 orders of magnitude smaller (better) than for pFinFETs

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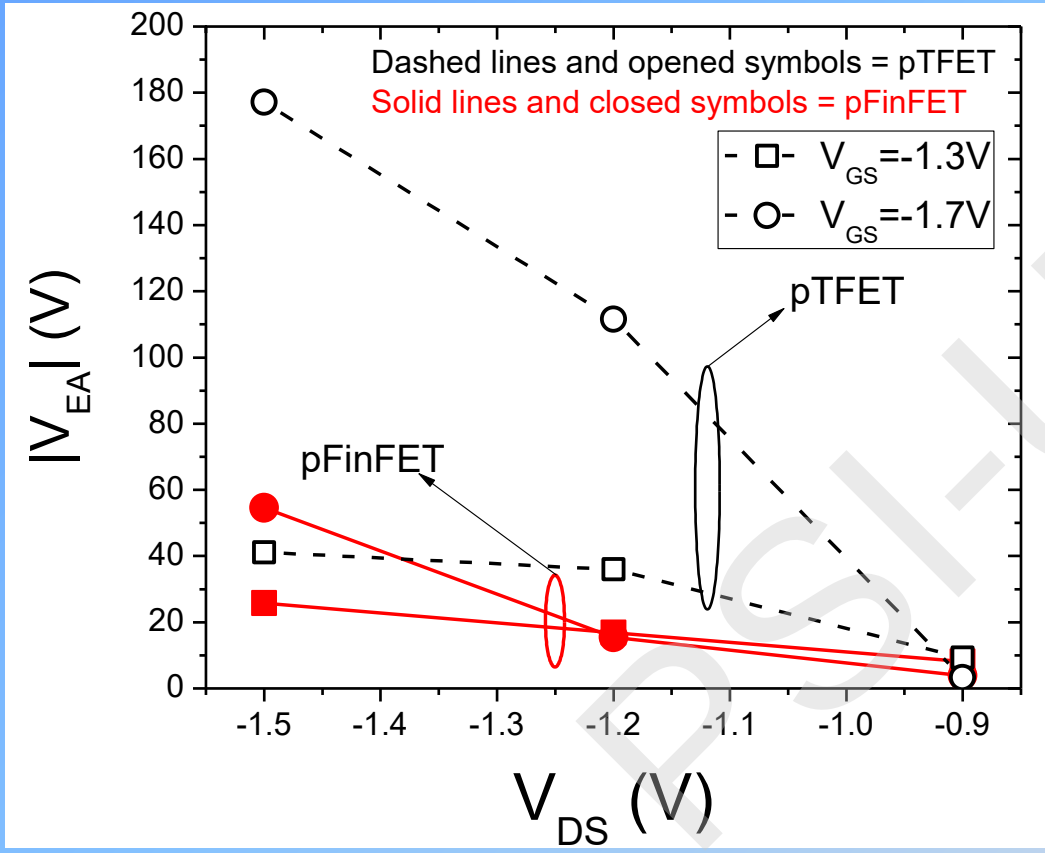
Early Voltage



pTFET

Tunneling mechanism

↓

Better I_{DS} x V_{DS} plateau

↓

Higher V_{EA}

V_{EA}: TFET better than FinFET

For V_{DS}= -0.9V the V_{EA} values were degraded for both pTFET and pFinFET because for this bias condition the transistors do not reach a saturation plateau

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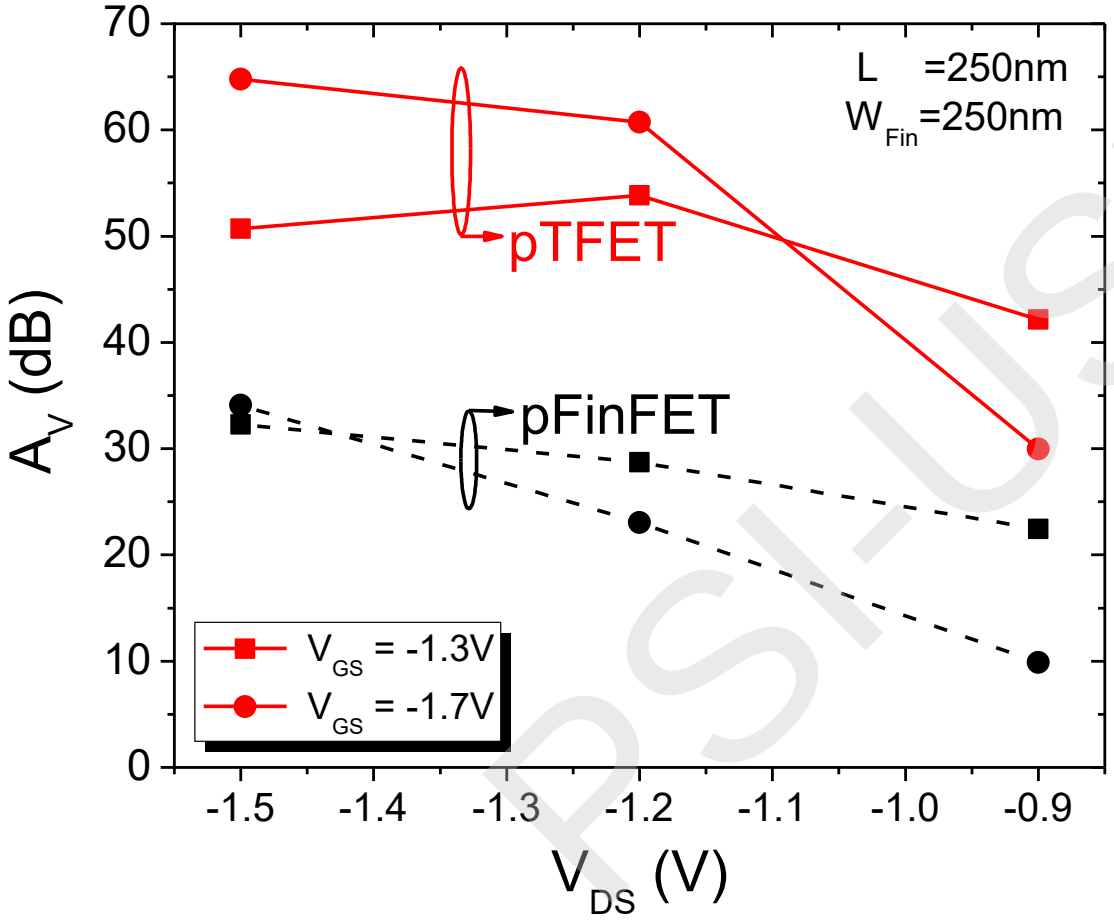
Intrinsic voltage gain



$A_V = gm/g_D$

g_D dominates the A_V behavior

A_V: TFET better than FinFET

TFET is promising for analog applications

* Agopian et al, TED, 2012

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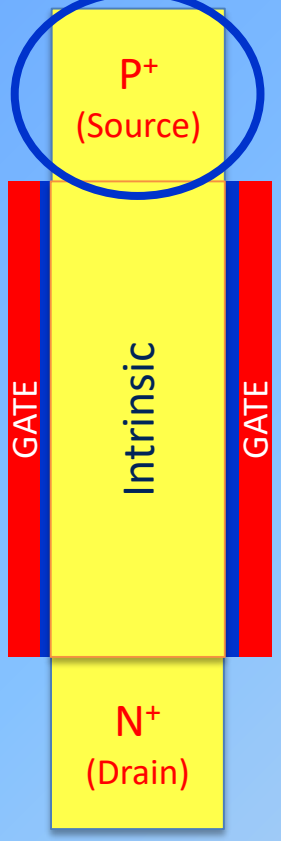
TFET x MOSFET technology

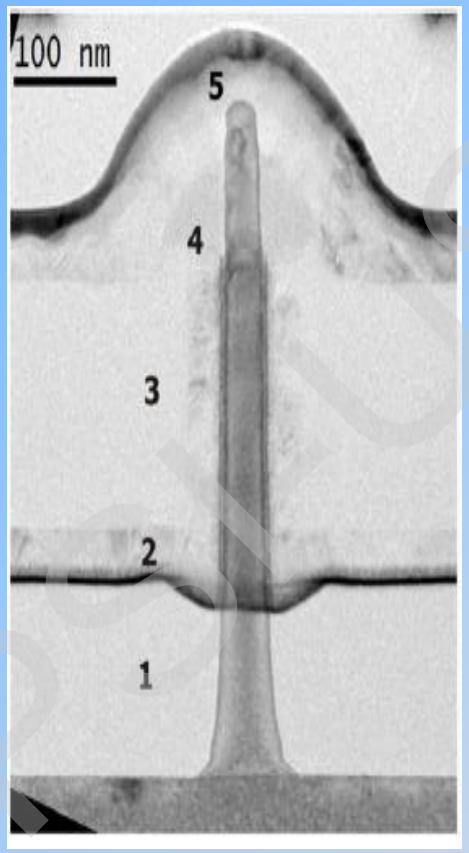
Fabricated at IMEC, Belgium

TFET

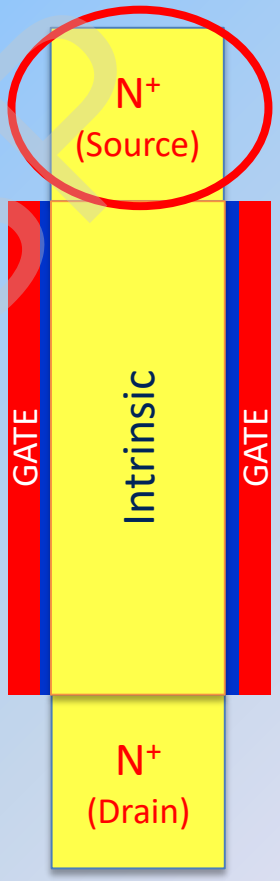
Si source



Si - Nanowire



MOSFET



* Agopian et al, ULIS/EUROSOI 2015

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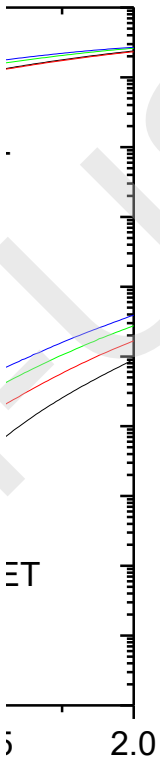
TFET x MOSFET technology

I_{ON} (MOSFET) >> I_{ON} (TFET)



MOSFET x TFET

Many orders of magnitude higher

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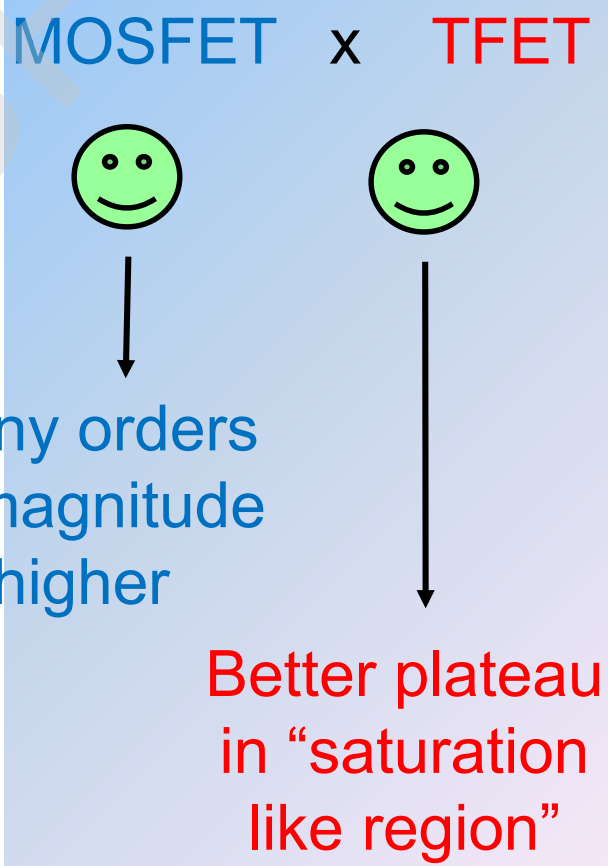
TFET x MOSFET technology

I_{ON} (MOSFET) >> I_{ON} (TFET)



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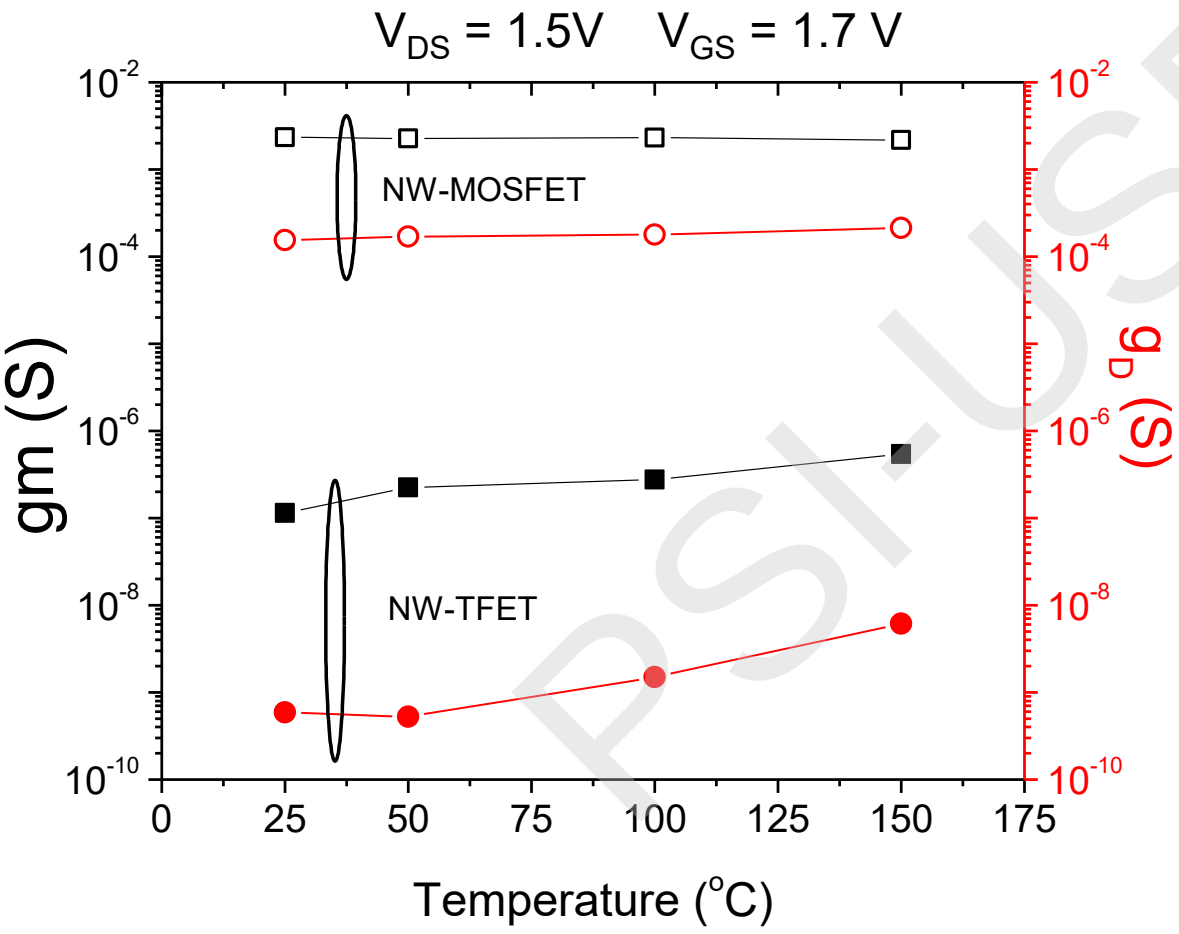
TFET x MOSFET technology

Analog Parameters



gm

MOSFET x TFET

At least **4** orders of magnitude higher

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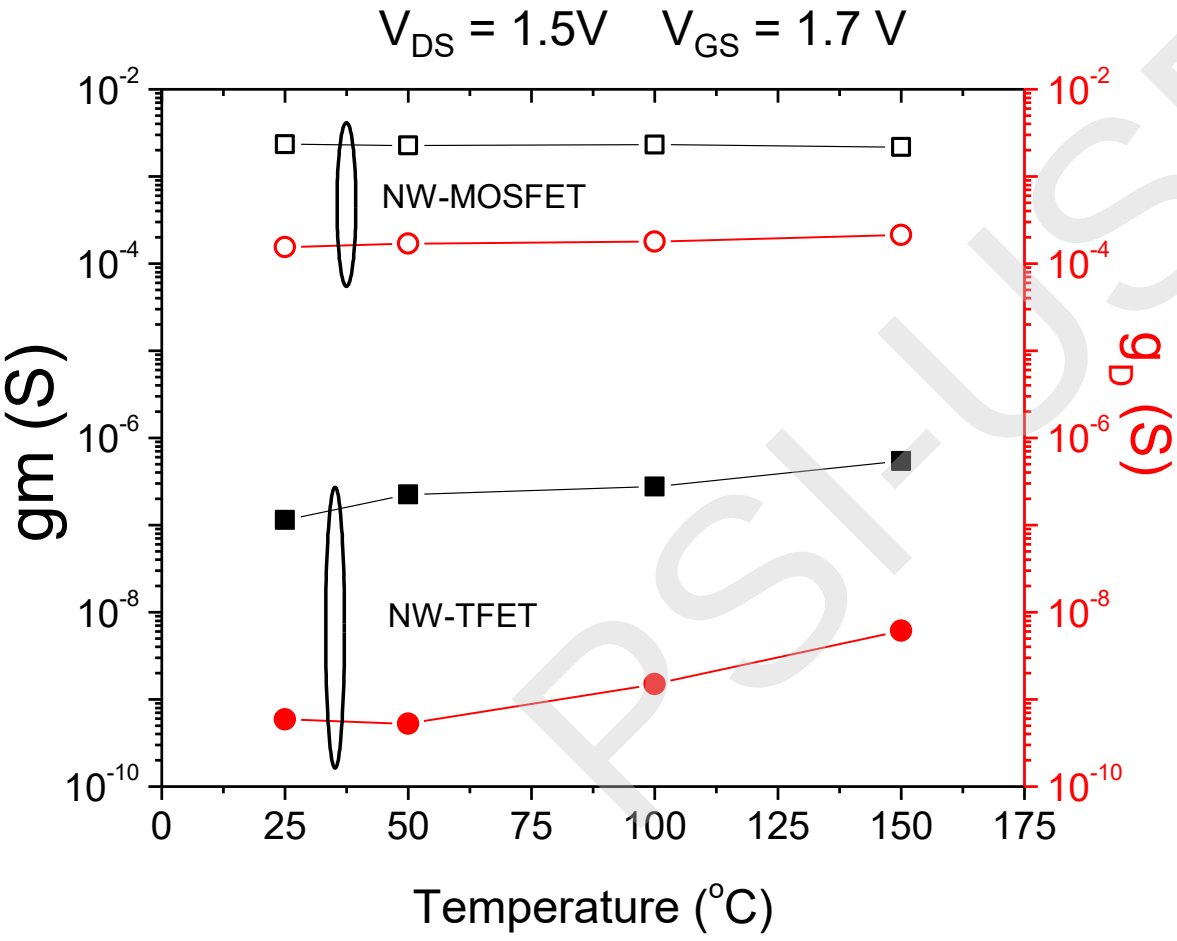
TFET x MOSFET technology

Analog Parameters



g_D

MOSFET x TFET

At least **5** orders of magnitude better

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TFET x MOSFET technology

Analog Parameters

High V_{GS} ensures BTBT

High V_{DS} ensures plateau

$$|A_V| = 20.\log(gm/g_D)$$

TFET is better than **MOSFET** for all studied temperature range

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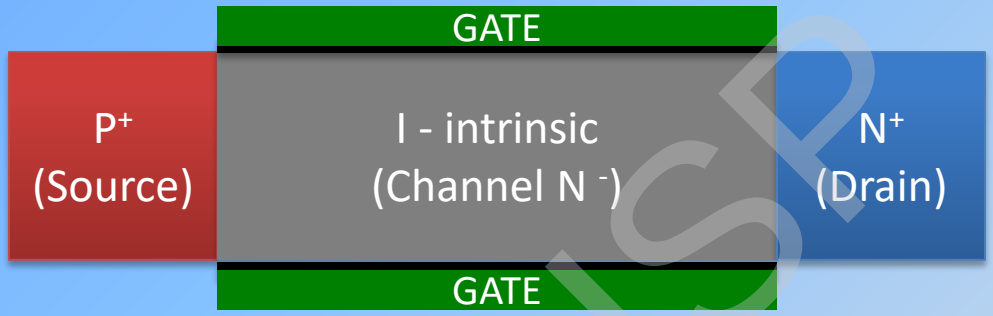
Ge Influence

Tunnel Field Effect Transistor - TFET



- Low drive current (I_{ON}) capability for Si;
  - Use of Ge at the source to improve tunneling mechanism;
  - Ge introduces some defects in the structure, increasing the interface trap density.

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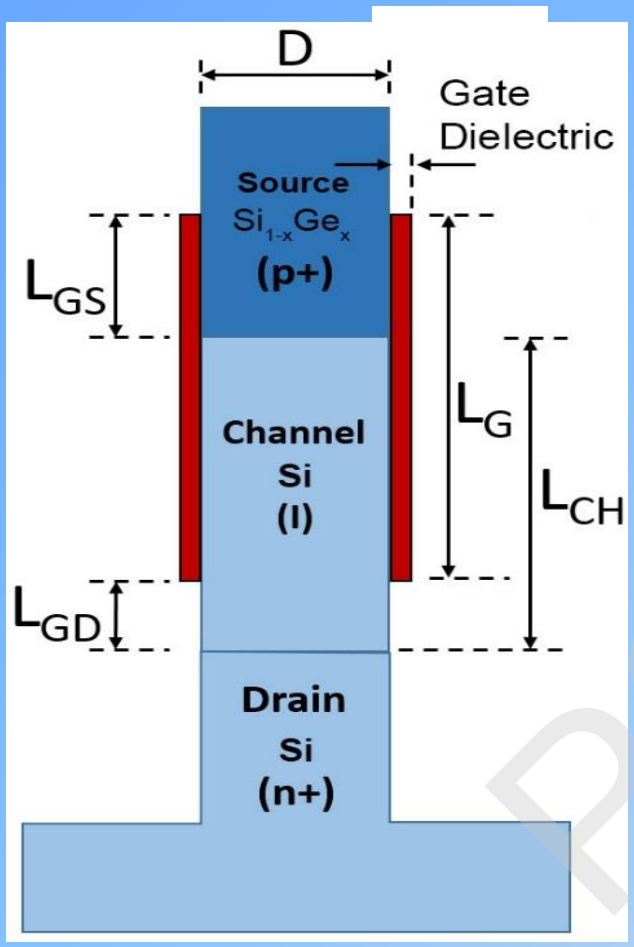
Device Characteristics



Dimensions:

Diameter (D) = 200nm;
Channel Length (L_{CH}) = 200 nm;
Physical Gate Length (L_G) = 240 nm;
Gate/Source overlap (L_{GS}) = 80 nm;
Gate/Drain underlap (L_{GD}) = 40 nm.

Source: 1.10^{20} at/cm^{-3}
Channel: 1.10^{16} at/cm^{-3}
Drain: 1.10^{19} at/cm^{-3}

Gate oxide = SiO_2 (1nm)+HfO_2 (3nm)

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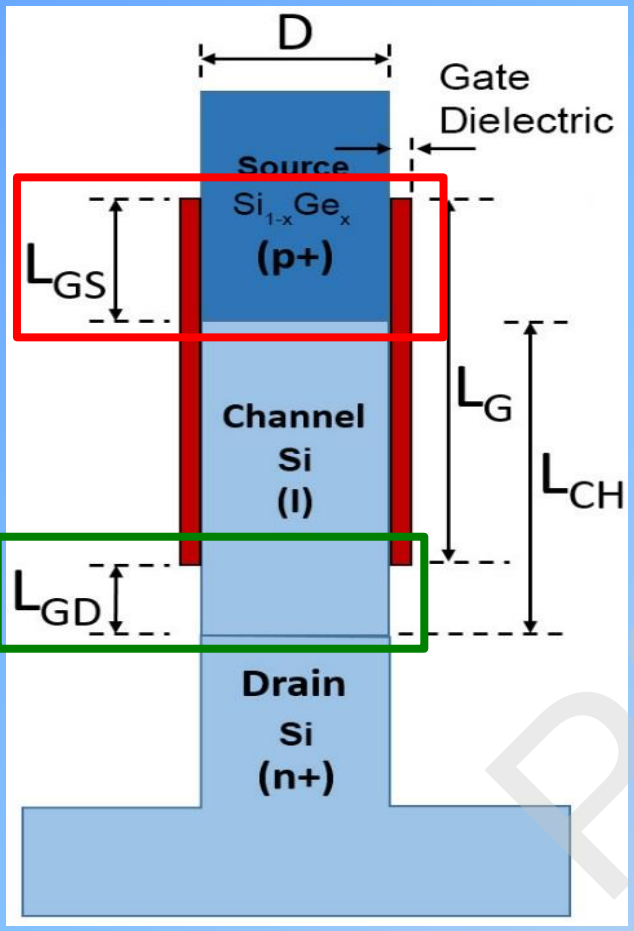
Device Characteristics



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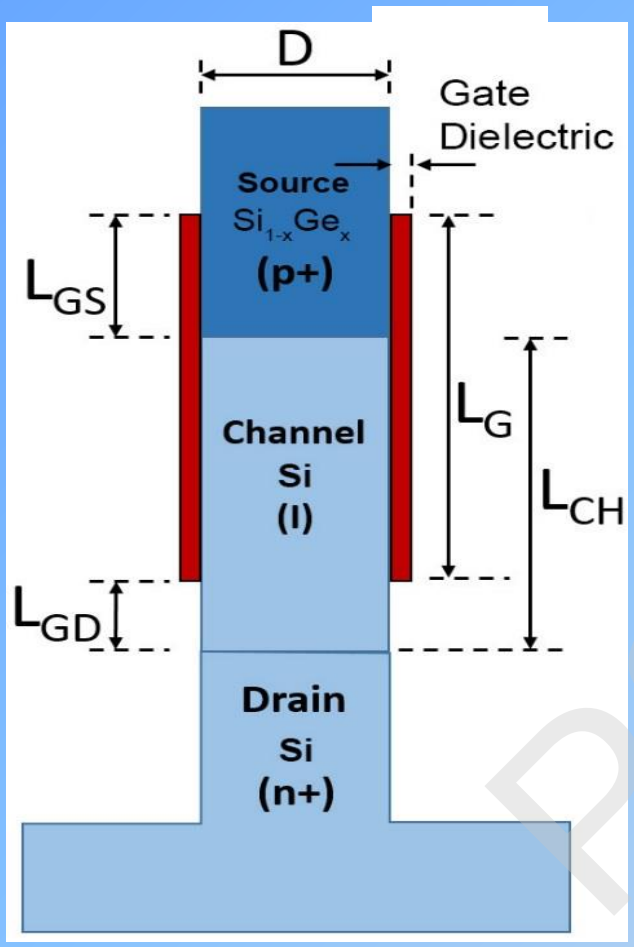
Device Characteristics



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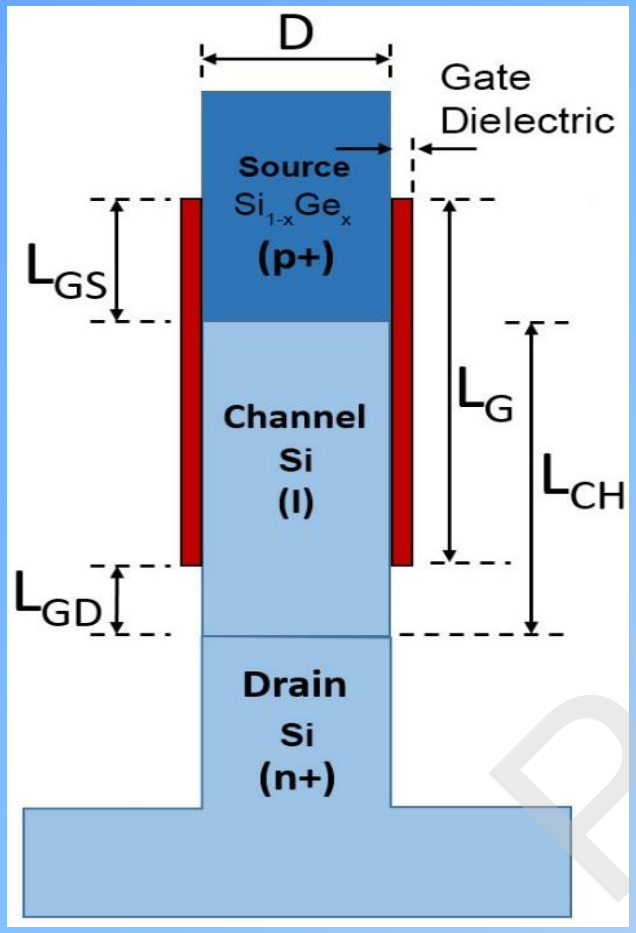
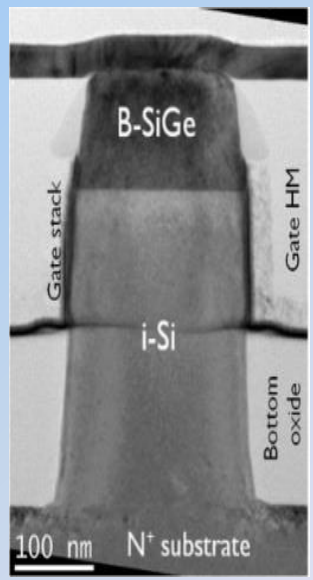
Device Characteristics



- Different source characteristics:
  - Si (100%)
  - $Si_{0.73}Ge_{0.27}$
  - $Si_{0.54}Ge_{0.46}$
  - Ge (100%)



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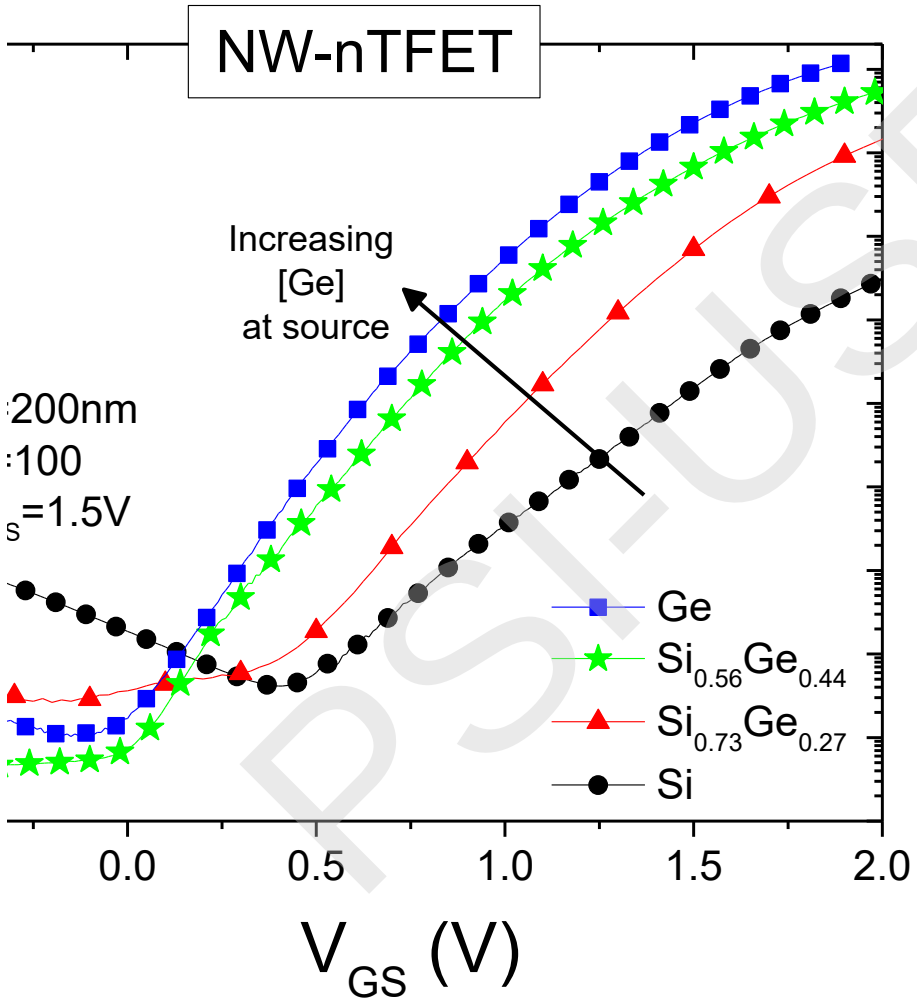
Drain Current



Ge ↑

E_G ↓

I_{ON} ↑

$V_{GS(on\text{-}set)}$ ↓

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Transconductance

Ge ↑ E_G ↓

I_{ON} ↑ gm ↑

(BTBT)

Weak positive T dependence

$gm_{(TFET)} = f(T)$: Inverse of MOSFET

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Output conductance

Ge ↑ BTBT ↑ g_D ↑

similar relative variation with temperature

- Degradation of g_D with temperature increases with BTBT

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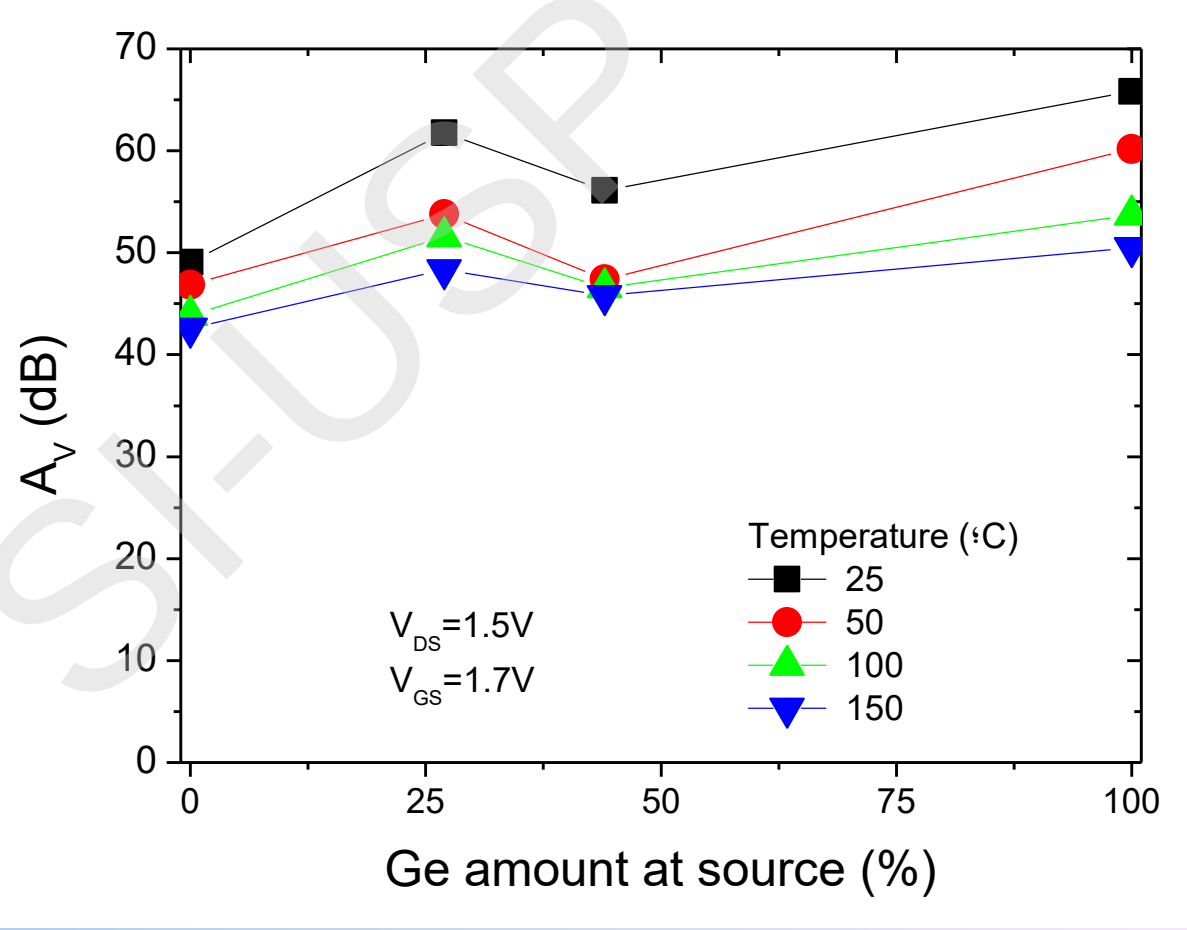
Intrinsic Voltage Gain

$|A_V| = 20.\log(gm/g_D)$

Ge ↑ BTBT ↑ A_V ↑

when T increases

g_D ↑ A_V ↓



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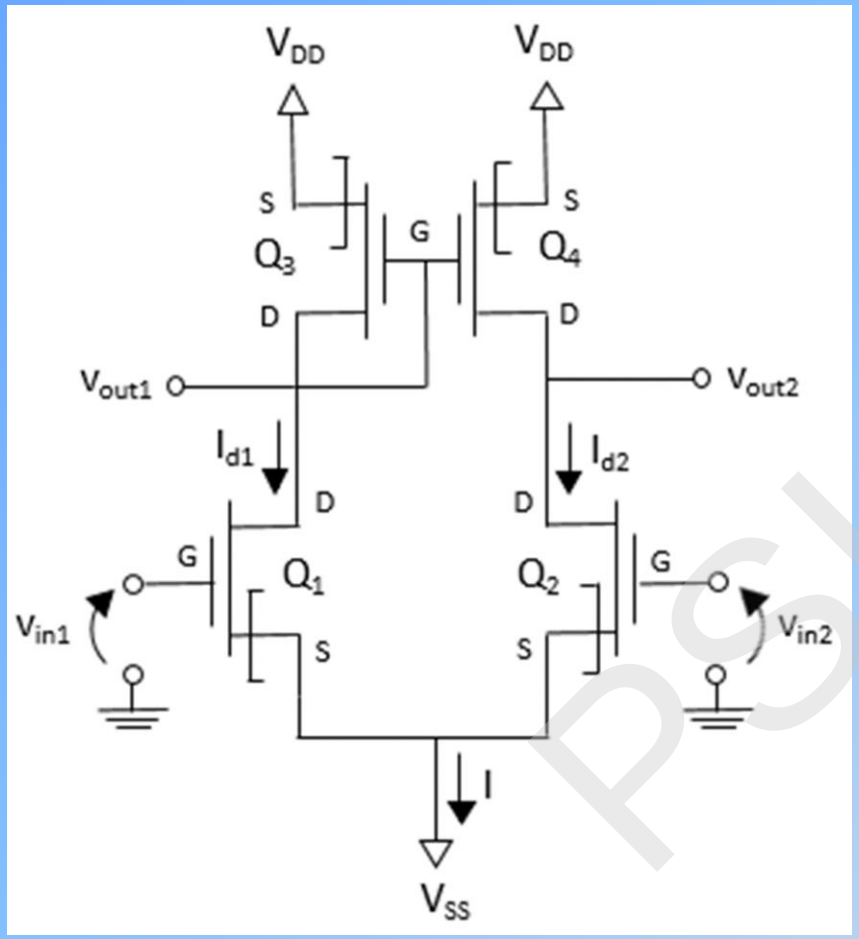
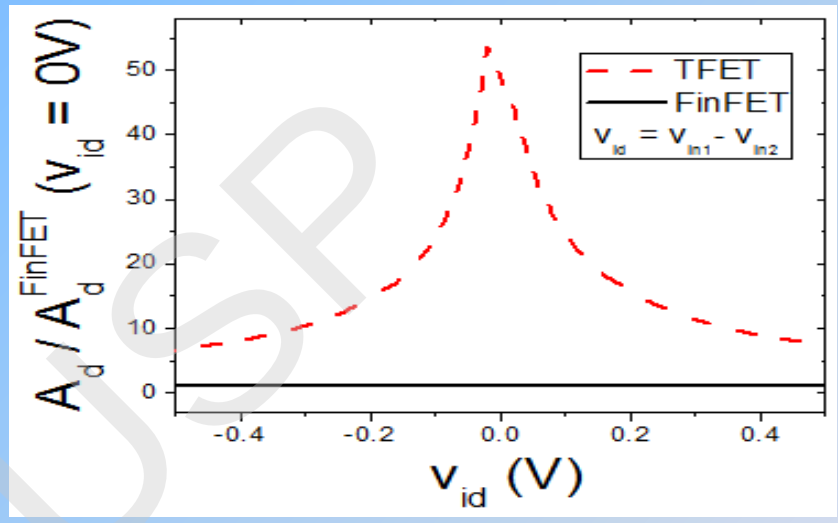
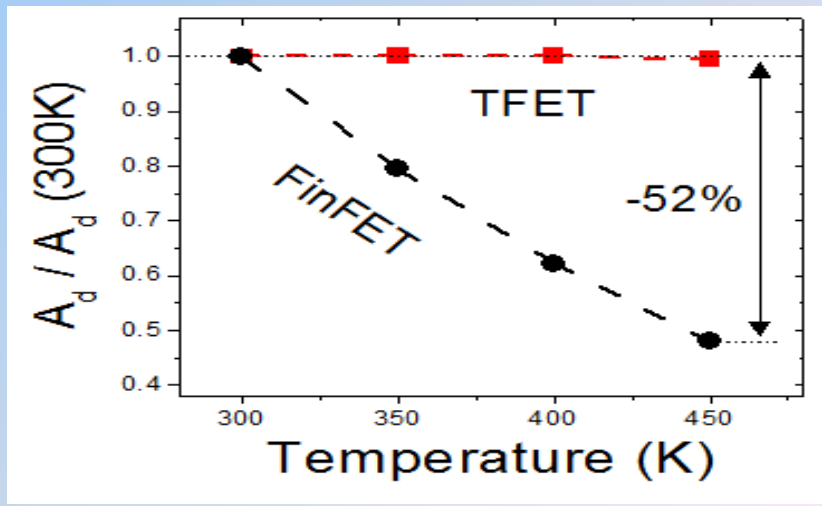
Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K



*Martino et al., EUROSOI/ULIS, 2016



A_d(TFET) > 50 A_d(FinFET)



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Conclusion

- ✓ FET: History: past, present, future
- ✓ MOSFET, SOI MOSFET, GC SOI MOSFET,

Bulk and SOI FinFET, UTBB SOI….. TFET

- ✓ Experimental and Simulation results
- ✓ **About the Moore's Law….**

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Past and future downsizing trends

*Hiroshi Iwai, EUROSOI/ULIS, 2016

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm→

0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →

90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012)

→ 14 nm (2014)

Fig.2 *Past downsizing trend*

Year	2013	2015	2017	2019	2021	2023	2025	2027
Commercial name (nm)	14	10	7	5	3.5	2.5	1.8	1.3
Half pitch (HP) (nm)	40	32	25.3	20	15.9	12.6	10	8
L_g (nm)	20.2	16.8	14.0	11.7	9.7	8.1	6.7	5.6

Fig.4 *Future downsizing trend by ITRS2013*

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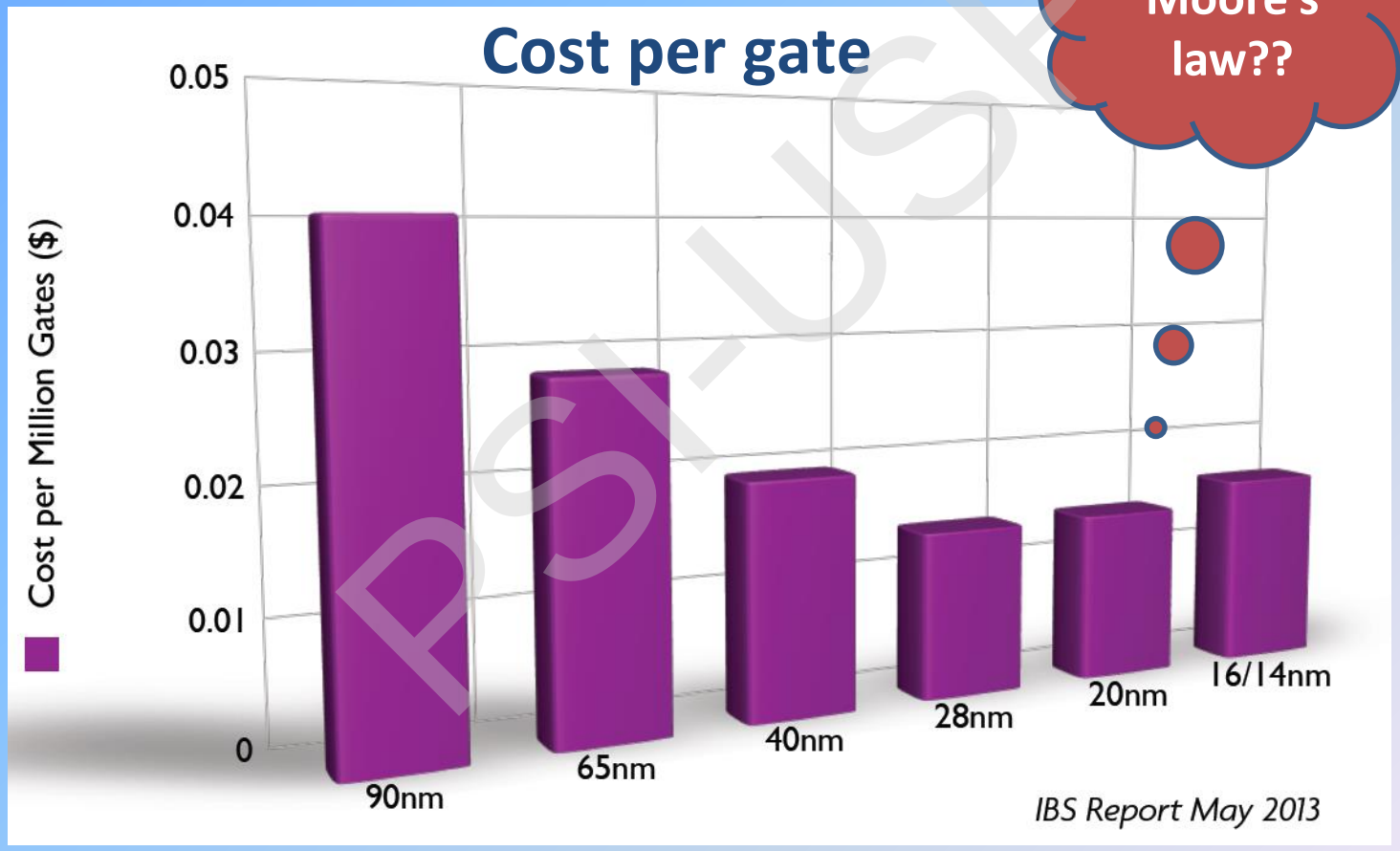
Conclusion

✓**About the Moore's Law….**



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Acknowledgments

SOI CMOS GROUP at USP - 2016

All my present students and researchers of SOI CMOS Group (USP)

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Acknowledgments

SOI CMOS GROUP – All Generations

All Generations of my students and researchers of SOI CMOS Group

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Prof. Dr. Jean-Pierre Colinge (TSMC)

Prof. Dr. Sorin Christoloveanu (Minatec/France)

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You are all welcome to visit us…

Dank u
Merci
Thank you
Obrigado

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