Lab session on 
pixel front-end characterization

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Focus of the lab

- **Pixel front-end ASICs** are located at the very beginning of the **signal processing chain** in pixel based detectors used in many fundamental and applied research fields.

- **Experimental characterization** of front-end circuits in advanced microelectronic technologies is an **integral part** of the implementation of modern radiation detection systems.

- The focus of the lab will be the **characterization of a front-end channel** for pixel detectors in a **65 nm CMOS technology**.

- The circuit under test is prototype for the **CMS phase 2 upgrade** in the framework of the Italian CHIPIX65 and the international RD53 collaborations.
Pixel front-end specs for HL-LHC

- In the phase 2 upgrade of the ATLAS and CMS experiments at the LHC, the inner layers of the pixel trackers will have to face some serious challenges:
  - very high hit rates: 1 - 2 GHz/cm² ➔ need of intelligent pixel level data processing
  - very high radiation levels: 1 Grad total ionizing dose, $10^{16}$ neutrons/cm² fluence
  - very high trigger rates: 1 MHz
  - small pixel cells: 50x50 μm² (or 25x100 μm²) ➔ improve resolution and reduce occupancy
  - small power dissipation: ~10 uW per cell (including analog and digital sections)

- Optimum front-end design requires a trade-off between noise, area, speed, power dissipation, amount of in-pixel functions

- The 65 nm CMOS process in its low power (LP) flavor is optimized for a reduced leakage and a small power consumption (at the price of a lower speed)
Front-end channel for ToT measurements

- Readout channel implementing the time over threshold (ToT) technique
- Charge preamplifier followed by a high speed, low power current comparator (transconductor + TIA)
- Designed for a ToT clock of 80 MHz
- 5 bit counter → 400 ns maximum time over threshold
- Also includes a 4 bit DAC for threshold correction
The Time over Threshold (ToT) technique provides a direct amplitude-to-time conversion; the signal at the shaper output is compared to a fixed voltage at the input of a threshold discriminator; the signal at the output of the discriminator is a digital pulse, whose duration is equal to the time during which the signal at the shaper output exceeds the threshold; digitization is easily achieved by computing the logic AND between the discriminator pulse and a reference clock and by counting the number of clock pulses.

If the signal at the shaper output returns to the baseline with a constant slope, then a linear relationship exists between the peak amplitude at the shaper output and the ToT duration (the rise time of the shaper output signal is assumed to be negligible).

\[ \text{ToT} = \frac{V_{\text{peak}} - V_{\text{th}}}{\frac{dV_{\text{shaper}}}{dt}} \]
Chip layout

DUTs

array of 12x8 channels

other test structures

array of 12x8 channels
Circuit layout

- Preamplifier output read out through an integrated analog buffer (also available for dedicated tests)
- Bias circuits
- Preamplifier with MOSFET feedback capacitor (channel 1)
- Preamplifier with MIM feedback capacitor (channel 2)
Some details on the DUT

- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to 10 - 20 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
Test setup

- 2 mm x 2 mm chip including two different versions of a charge preamplifier with Krummenacher-style feedback network

- Chip on a small daughter board mounted on a test PCB, including dip switches for channel configuration: gain, time to baseline, input capacitance for detector emulation
Power

+12 V (236 mA)
-12 V (195 mA)
GND
Bias currents and voltages

2 uA across 100 k
bias current for the folded cascode branch (FC_BIAS)

30 uA across 10 k
bias current for the preamplifier input branch (IREF_VI)

16 uA across 10 k
reference current for the chip-wide DAC threshold

1.6 uA across 100 k
reference current for the in-pixel DAC threshold

300 mV
reference voltage for the Krummenacher feedback network (RIF_KRUM)
Gain stage based on a **folded cascode configuration**

- Amplifier schematic

- **IREF_VI**: 30 uA
- **10 k**: 10:1
- **OUT**: total power dissipation is about 3.6 uW (not considering power in the reference branch of the mirror - the same reference branch can be used for all the pixels in an array)

**external components**

- **100 k**: 10:1
- **FC_BIAS**: 2 uA
channel 1 output

channel 2 output

channel 3 output

channel 4 / analog buffer output (to be selected on the daughter board)

channel output available through an on board, non inverting 2x amplifier (AC coupled to the chip and AC and 50 Ohm coupled to the LEMO connector)

test points (channel output accessible through probes)

input selector: INJ-EXT=1 (ON), all others=0

input connector (50 Ohm coupled) - inject signal at the $C_{\text{inj}}$ capacitor (30 fF) or at the analog buffer input, according to the selection on the daughter board
Channel configuration

A few bits need to be programmed to configure the channel

charge sensitivity (gain selection)
- 0 → high gain ($C_F=10 \text{ fF}$)
- 1 → low gain ($C_F=20 \text{ fF}$)

recovery current in the Krummenacher network (SUB_NOISE)
- 0 → low recovery current ($I_K=12.5 \text{ nA}$)
- 1 → high recovery current ($I_K=25 \text{ nA}$)

detector emulating capacitor (ANAOUT_EN,DIGOUT_EN)
- 00 → $C_D=0$
- 10 → $C_D=50 \text{ fF}$
- 01 → $C_D=100 \text{ fF}$
- 11 → $C_D=150 \text{ fF}$

Nominal configuration (for operation @5 bit/80 MHz) is
- high gain (0)
- low recovery current (0)
- $C_D=100 \text{ fF}$ (01)
Channel configuration

JP23
1 - SEL_C2F (LSB of the threshold DAC, also RS0 on the side)
2 - ANAOUT_EN (bit for detector capacitance selection)
3 - DIGOUT_EN (bit for detector capacitance selection)
4 - SUB_NOISE (select the current in the Krummenacher feedback)

CS3 - gain selection (select the gain of the charge preamplifier, not available as a dip switch)

JP22
1 - SEL_C4F (bit 1 of the threshold DAC)
2 - SEL_C50F (bit 2 of the threshold DAC)
3 - SEL_C100F (bit 3 of the threshold DAC)
4 - TOT_EN (1 to enable injection)

• keep SEL_C4F, SEL_C50F, SEL_C100F to 1, use SEL_C2F to control the gain (connect RS0 to CS3)
Input/output selection on the daughter board

input selector:
- 1 to 4 - channel 1 to 4
- B - analog buffer

A_OUT4 selector:
- PA4 - channel 4
- BUF - analog buffer
Instrumentation and prerequisites

- Simple bench top instrumentation is required for measuring gain, ENC, response of the channel in presence of a leakage current: power supply, digital scope, arbitrary function generator.

- No previous experience in pixel front-end characterization is required.

- Basic knowledge on electronic circuit operation and standard electronic instrumentation is a prerequisite.
The expected signal at a charge preamplifier input is a current pulse - it can be obtained by differentiating a voltage step signal through the injection capacitance.

The actual input variable is the charge $Q = C_{inj} V_{step}$.
Characterization of the preamplifier response

Main signal parameters:

- amplitude (also as a function of the gain)
- peaking time (also as a function of the detector capacitance)
- slope on the falling edge (also as a function of the recovery current)
The peaking time is found to increase with $C_D$: to understand why assume $C_K \to \infty$ and a single pole approximation for the gain of the forward stage

$$A(s) = \frac{A_0}{1+s\tau}$$

The closed loop gain is

$$\frac{V_o}{V_{in}} \approx \frac{2sC_{inj}}{g_m 2s^2\tau C_T\sqrt{A_0g_m}/A_0 + 2s(C_T + A_0C_F)\sqrt{A_0g_m} + 1}$$

$C_T = C_D + C_{in} + C_F + C_{inj}$

In the high frequency regime, governing the response speed of the preamplifier

$$\frac{V_o}{V_{in}} \approx \frac{C_{inj}}{C_F s\tau C_T/A_0C_F + 1}$$

corresponding to an exponential response (of the $1-\exp(-t/\tau_F)$ kind) with time constant

$$\tau_F \approx \frac{C_D + C_{inj} + C_F + C_{inj}}{A_0C_F}$$
Charge sensitivity

- Is defined as
  \[ G_Q = \frac{dV_p}{dQ} \]

- As long as the circuit is operated in the linear region
  \[ G_Q = \frac{V_p}{Q} \propto C_F^{-1} \]

- To avoid the effects of local, slight non-linearities, \( G_Q \) can be measured by
  - measuring the amplitude for different values of the input charge
  - linearly interpolating the data points in the amplitude vs charge plot \( G_Q \) is the slope of the interpolating straight line
Noise and equivalent noise charge (ENC)

The main noise sources in the preamplifier are located

• in the preamplifier input device - can be represented through an equivalent series source ($e_n$) and includes a white thermal and a flicker term with power spectral density $S_w$ and $S_f$ respectively

$$\frac{d\overline{e_n^2}}{df} = S_w + \frac{S_f}{f}$$

• in the feedback network - can be represented through an equivalent parallel source ($i_n$), mostly with a white spectrum with power spectral density $S_p$

$$\frac{d\overline{i_n^2}}{df} = S_p$$
Noise and equivalent noise charge (ENC)

- Noise in the preamplifier is responsible for some degree of inaccuracy in the measurement of the signal amplitude at the circuit output.
- Noise at the channel output can be measured as the standard deviation of the signal when no stimulus is applied to the input.
- One can actually sample the voltage at the channel output and compute the standard deviation $\sigma_n$ as

$$
\sigma_n = \sqrt{\frac{1}{N} \sum_{i=1}^{N} x_i^2 - \left( \frac{1}{N} \sum_{i=1}^{N} x_i \right)^2}
$$

$x_i$=i-th sample

$N$=# of samples

which is easily done by using the statistical functions available in virtually all digital storage scopes.
Noise and equivalent noise charge (ENC)

Equivalent noise charge is defined as the charge to be injected at the input to have an output signal with an amplitude $V_p$ equal to the noise $\sigma_n$, or the input charge needed to have a unit signal-to-noise-ratio at the output:

$$\frac{G_Q \cdot \text{ENC}}{\sigma_n} = 1 \Rightarrow \text{ENC} = \frac{\sigma_n}{G_Q}$$

So, to measure the ENC you need measure:

- the noise at the preamplifier output
- the charge sensitivity

The ENC is a charge and is measured in Coulomb, but is seldom expressed in electrons:

$$\text{ENC}[\text{in electrons}] = \frac{\text{ENC}[\text{Coulomb}]}{1.602 \cdot 10^{-19} \text{C}}$$
A quite general expression for the ENC is the following, accounting for the different noise contribution:

\[
\text{ENC}^2 = C_T A_1 S_w \frac{1}{\tau} + C_T A_2 S_f + A_3 S_p \tau
\]

- \(C_T = C_D + C_{\text{in}} + C_F + C_{\text{inj}}\)
- \(A_1, A_2, A_3 = \text{shaping coefficient}\)
- \(\tau = \text{shaping time (has some relationship with } t_p)\)

The effect of the series noise source on the overall noise performance gets more pronounced as \(C_T\) (the capacitance shunting the circuit input terminal) increases.

The slope of the ENC vs \(C_D\) is a figure of merit telling us how the noise performance of the circuit degrades as the detector capacitance increases.
ENC, gain and recovery current

Play with the gain (high or low) and/or the recovery current (high or low) configuration bits of the channel and try to anticipate the changes in the ENC before measuring it, or to explain them after measurement

• As far as the changes with gain are concerned, consider that the noise model proposed in the previous slides is incomplete - other, although less important, noise sources are present in the channel, whose effect at the output is only weakly (or not at all) dependent on the gain as compared to the series source $e_n$ and the parallel source $i_n$

• As far as the changes with recovery current are concerned, consider that the power spectral density of the parallel noise $i_n$ is

$$S_p \approx 16k_B T \Gamma g_m$$

where $g_m$ is the transconductance of the MOS transistors in the Krummenacher differential pair

$k_B$=Boltzmann’s constant
$T$=absolute temperature
$\Gamma$=channel thermal noise coefficient
Measurements in the presence of a leakage current

- The readout channel has to work correctly also in the presence of a leakage current at the input terminal.

- In the real application, this leakage current comes from the detector and may exceed 10 nA when the detector is exposed to very high ionizing radiation doses - ~1 Grad for 10 year operation is expected for the inner layers of the CMS detector at the HL-LHC.

- In the DUT, a capacitor ($C_{\text{inj}}$) is integrated at the preampli input for test purposes, the only way to access the input terminal - no DC current can be applied directly at the input terminal to emulate the leakage current from the detector.
Measurements in the presence of a leakage current

If a ramp signal is applied to the injection capacitance, a quiescent current will be flowing through the input terminal of the preamplifier (after an initial transient)

\[ I_{\text{leak}} = -C_{\text{inj}} \frac{dV}{dt} \]

time needed for recovery after large pulse injection (~20 us)

ramp start - expect a transient at the preampli output

very large pulse injected at the input - expect a long transient at the preampli output
Measurements in the presence of a leakage current

During each ramp, a step signal can be injected to test the response of the channel to a charge pulse - the step signal is superimposed to the ramp signal.

The maximum $I_{\text{leak}}$ depends on the allowed signal excursion and on the duration of the transient after the ramp start.

Both charge sensitivity and noise measurements can be performed in these conditions to evaluate the effect of a leakage current on the channel operation.
Analog voltage buffer

- Preamplifier output not directly available on the test board - the output stage of the preamplifier can drive only very small loads

- An analog voltage buffer in a white follower configuration is used at the preamplifier output, which can drive relatively large loads, like oscilloscope probes (~10 pF/1 MΩ) or discrete op amps (~pF) - anyway
  - its gain is not exactly 1 (it is ~0.85)
  - there is an offset of about 450 mV (the threshold voltage of a PMOS transistor) between the input and the output DC voltages

- A standalone version of the buffer is available in the chip - some measurements could be performed to verify that it does not degrade the properties of the signal from the preamplifier
  - step response (rise and fall time)
  - input/output trans-characteristic
  - frequency response (DC gain and cut-off frequency)