Lab session on pixel front-end characterization

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Intelligent Front-End Signal Processing for Frontier Exploitation in Research and Industry

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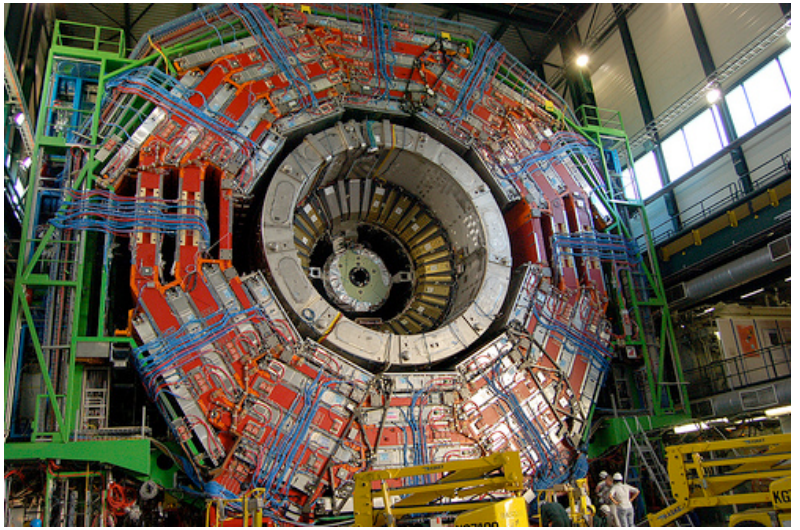
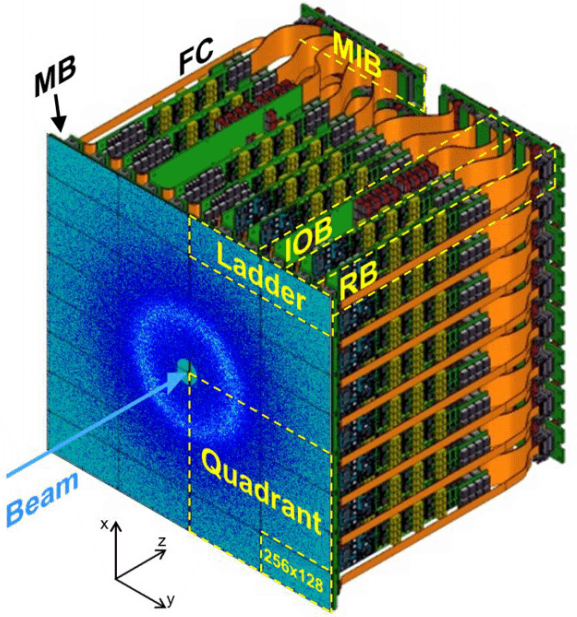
Focus of the lab

- Pixel front-end ASICs are located at the very beginning of the signal processing chain in pixel based detectors used in many fundamental and applied research fields
- Experimental characterization of front-end circuits in advanced microelectronic technologies is an integral part of the implementation of modern radiation detection systems
- The focus of the lab will be the **characterization of a front-end channel for pixel detectors in a 65 nm CMOS technology**
- The circuit under test was developed for the upgrade of the innermost layer of the CMS pixel detector – to be deployed at the future High Luminosity Large Hadron Collider (HL-LHC)

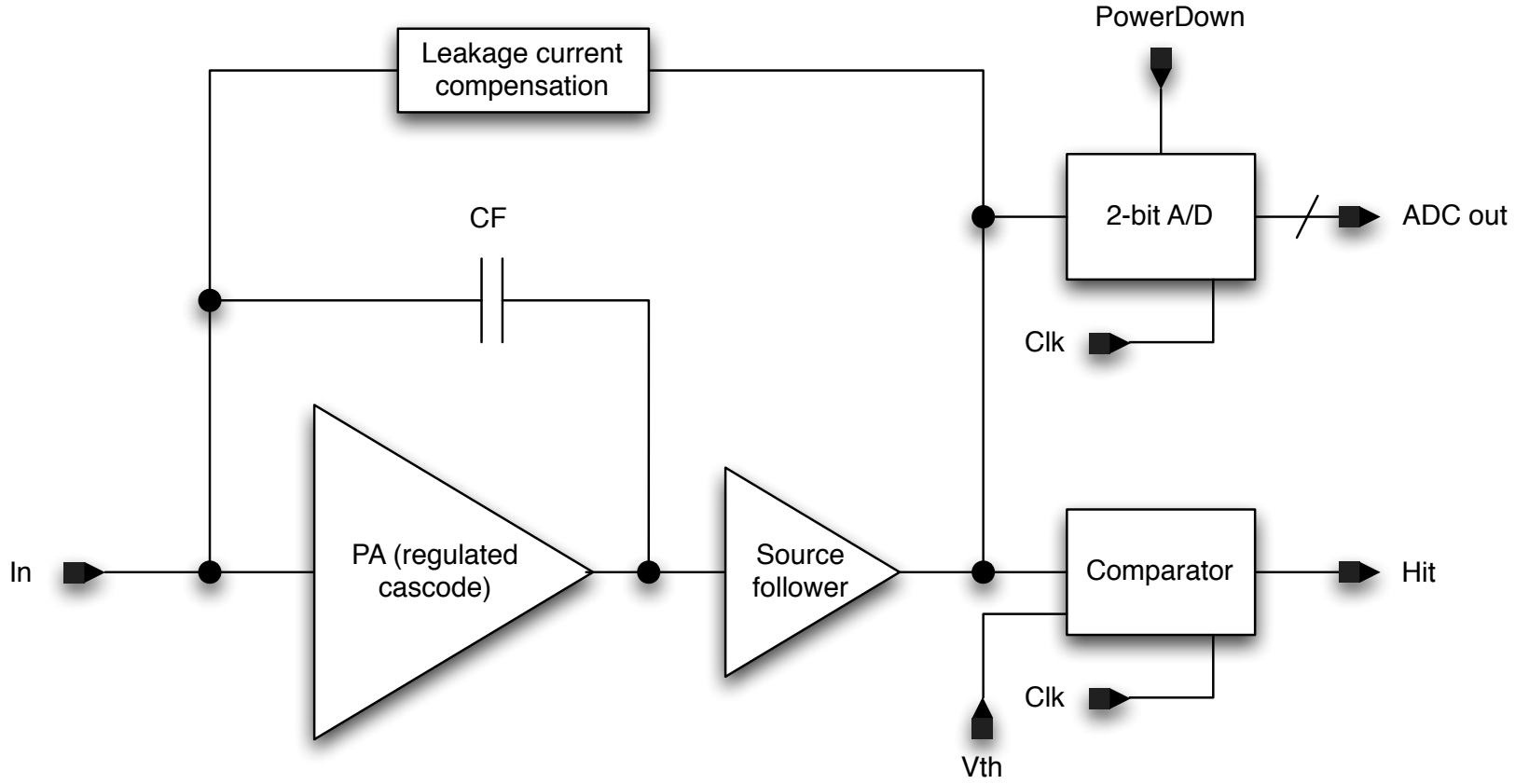




Pixel front-end specs for HL-LHC

- In the phase 2 upgrade of the ATLAS and CMS experiments at the LHC, the inner layers of the pixel trackers will have to face some serious challenges
  - very high hit rates: 1 – 2 GHz/cm^2 ➔ need of intelligent pixel level data processing
  - very high radiation levels: 1 Grad total ionizing dose, 10^{16} neutrons/cm^2 fluence
  - very high trigger rates: 1 MHz
  - small pixel cells: 50x50 um^2 (or 25x100 um^2) ➔ improve resolution and reduce occupancy
  - small power dissipation: ~10 uW per cell (including analog and digital sections)
- Optimum front-end design requires a trade-off between noise, area, speed, power dissipation, amount of in-pixel functions
- The 65 nm CMOS process in its low power (LP) flavor is optimized for a reduced leakage and a small power consumption (at the price of a lower speed)

iFCP65 Front-end channel



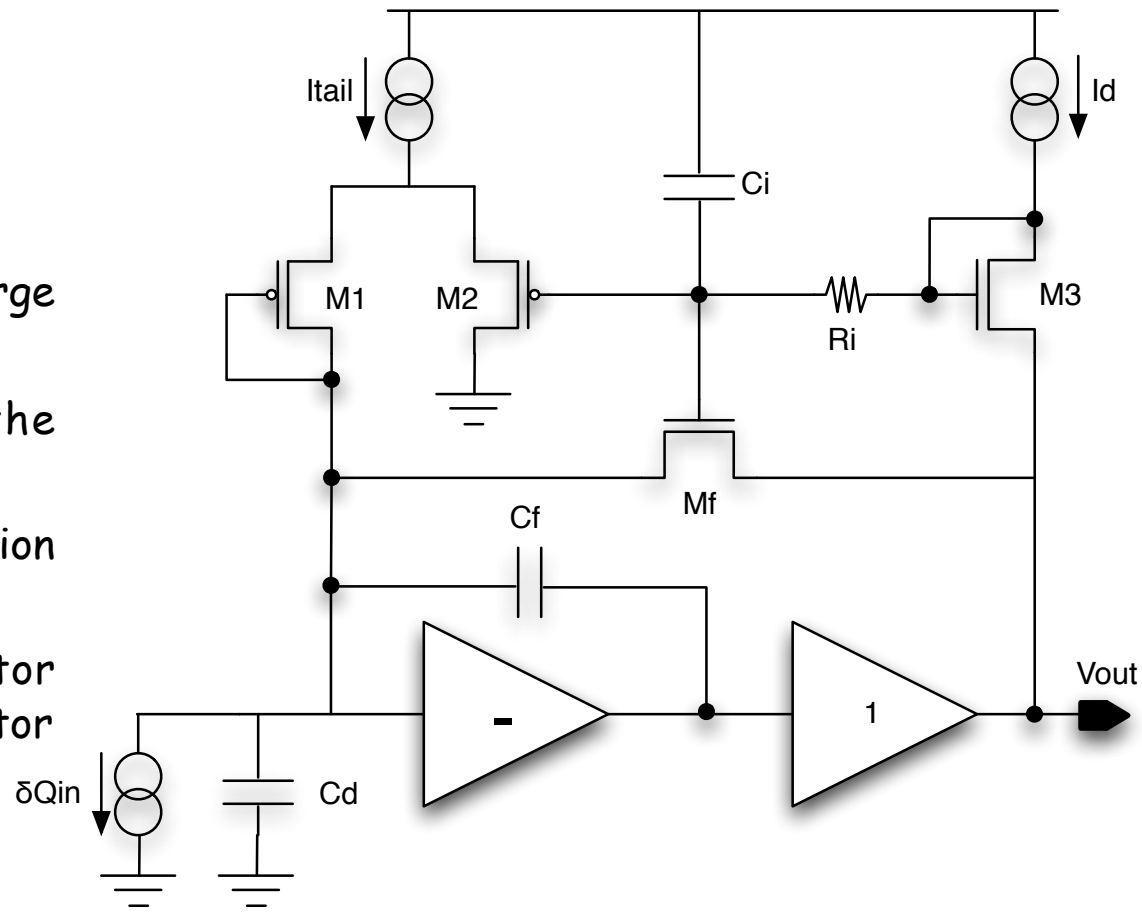
- Readout channel implementing a zero dead-time design – hit detection takes no more than 25 ns
- Leakage current compensation up to 10 nA
- Hit comparator based on "praying mantis" architecture – 12.5 ns reset phase + 12.5 ns comparison phase
- 2-bit flash ADC (3 discriminators, same as the hit comparator) for amplitude measurements

Charge preamplifier

- **Regulated cascode** design

- Active feedback transistor Mf:
  - **1/gm resistor** for small signals
  - **Constant current source** for large signals
  - M1 provides a DC path for the **detector leakage current**
  - Ri + Ci ensures low frequency operation of the leakage compensation circuit
  - Itail > sum of expected detector leakage and k Id (k = mirror factor between M3 and Mf)

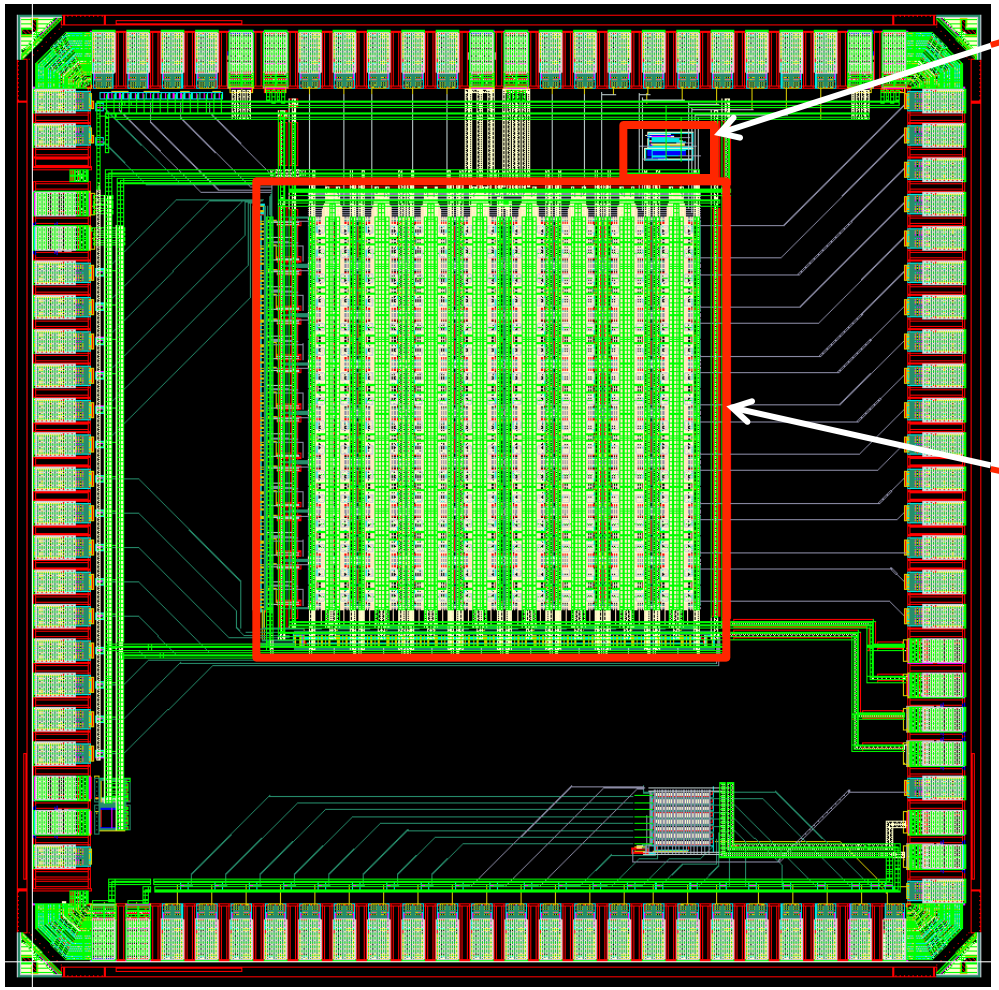
- **Current consumption** ~ 4.0 *μA*



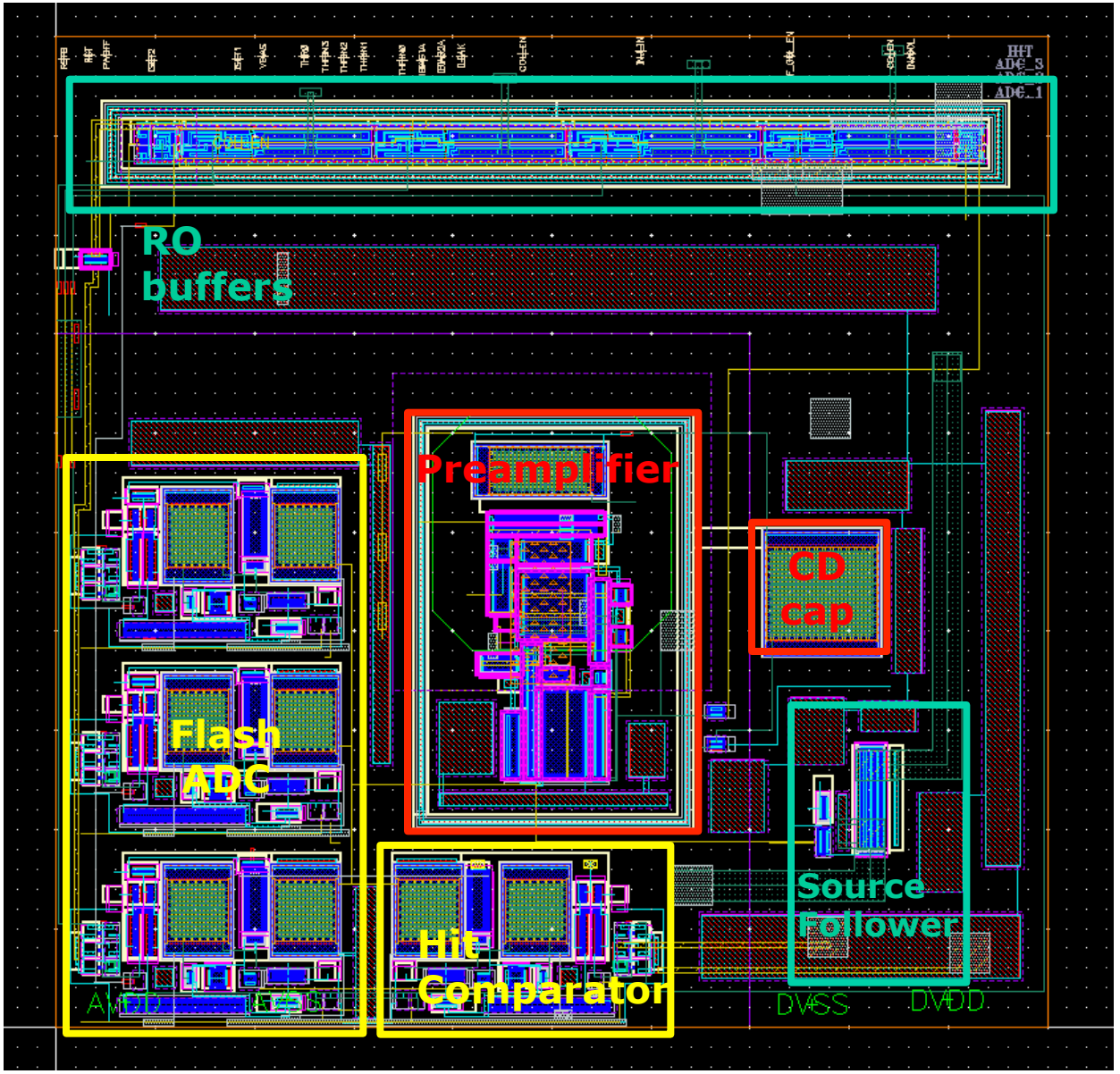
Chip layout

Chip developed by:
Davide Braga,
David Christian,
Grzegorz Deptuch,
Farah Fahim,
Luigi Gaioni,
Benedetta Nodari,
Lodovico Ratti,
Valerio Re,
Thomas Zimmermann

Design by:
Davide Braga,
Luigi Gaioni,
Benedetta Nodari

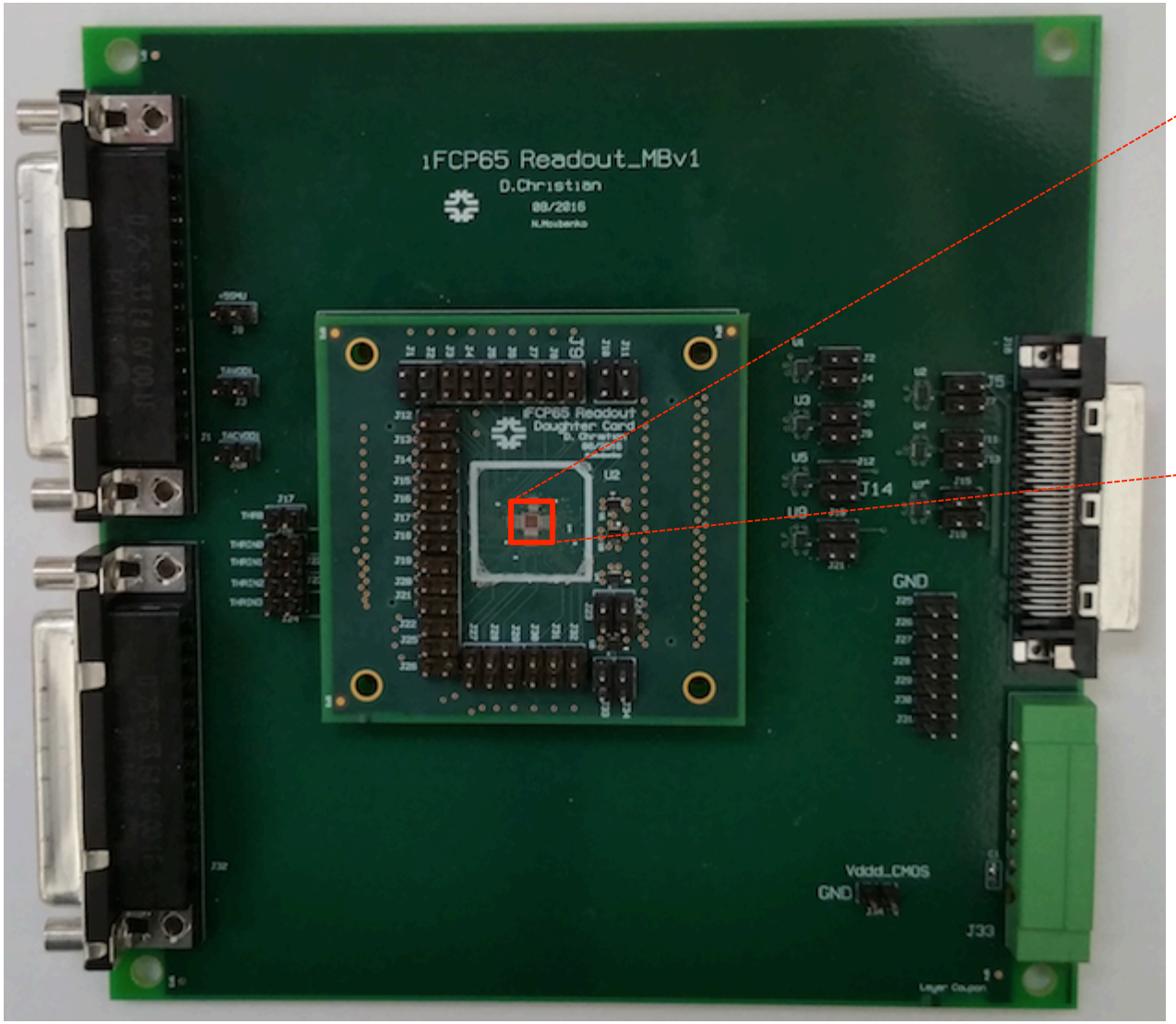


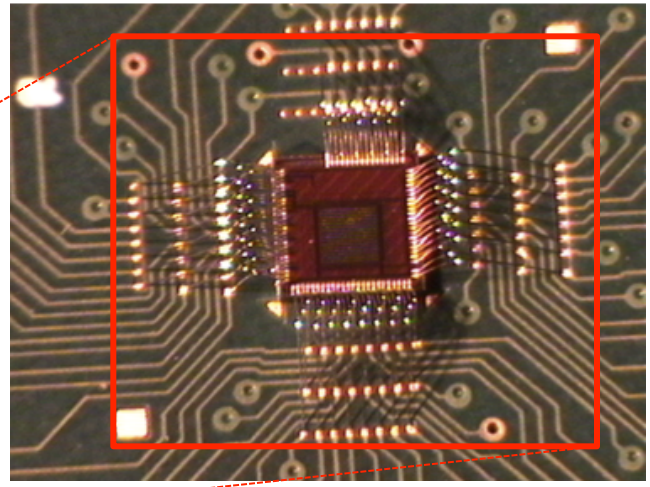
Front-end layout



- Front-end laid out in a 35um x 35um area
- RO buffers and source follower integrated in the top and right side of the pixel
- All the devices in the global P-substrate
- Nwell guard ring surrounding the preamplifier
- 35 fF detector emulating capacitance

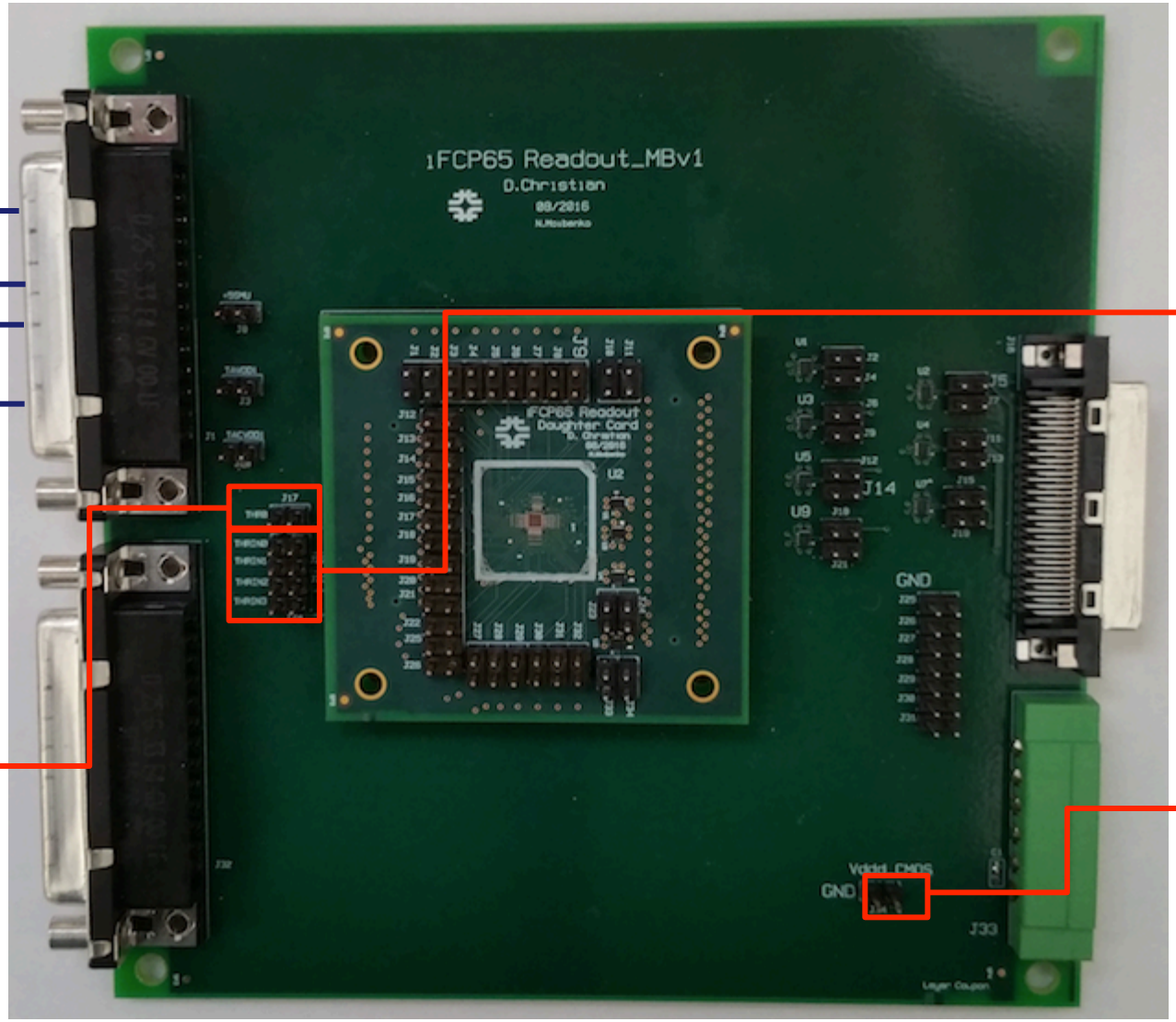
Test setup





- Chip on a small daughter board mounted on a test PCB, with connectors for power, bias, slow control (chip configuration), input and output (both digital and analog) signals

Power and reference voltages



+5 V (output buffer bias)

GND

+1.2 V (analog chip power)

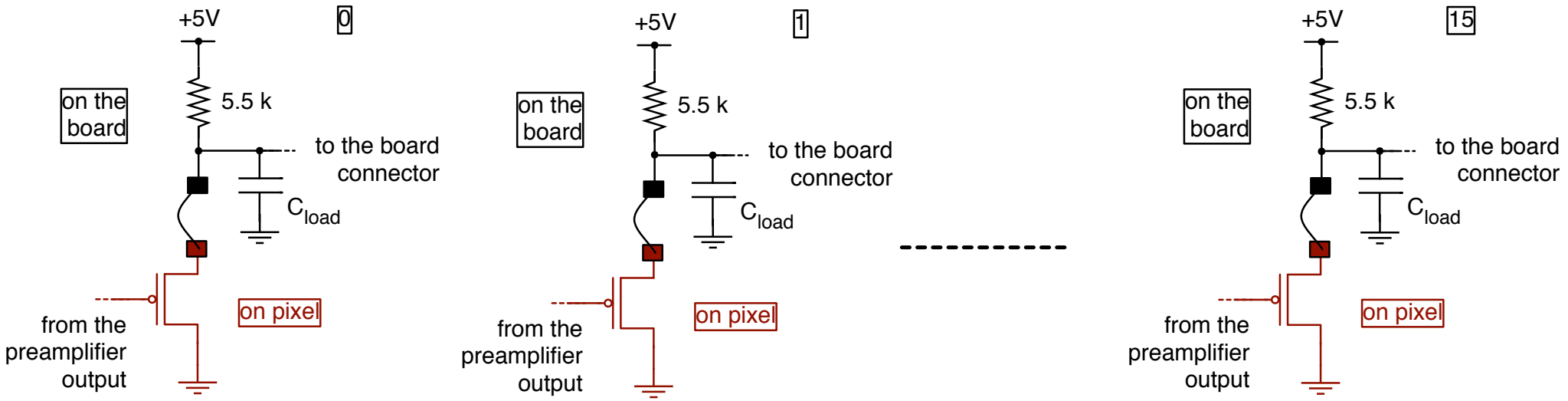
+1.2 V (digital chip power)

reference voltage for the 4 comparators (GND)

4 separate threshold voltages for the 4 comparators

+2.5V/3V (level shifters, 1.2V←→2.5V/3V)

Output buffers



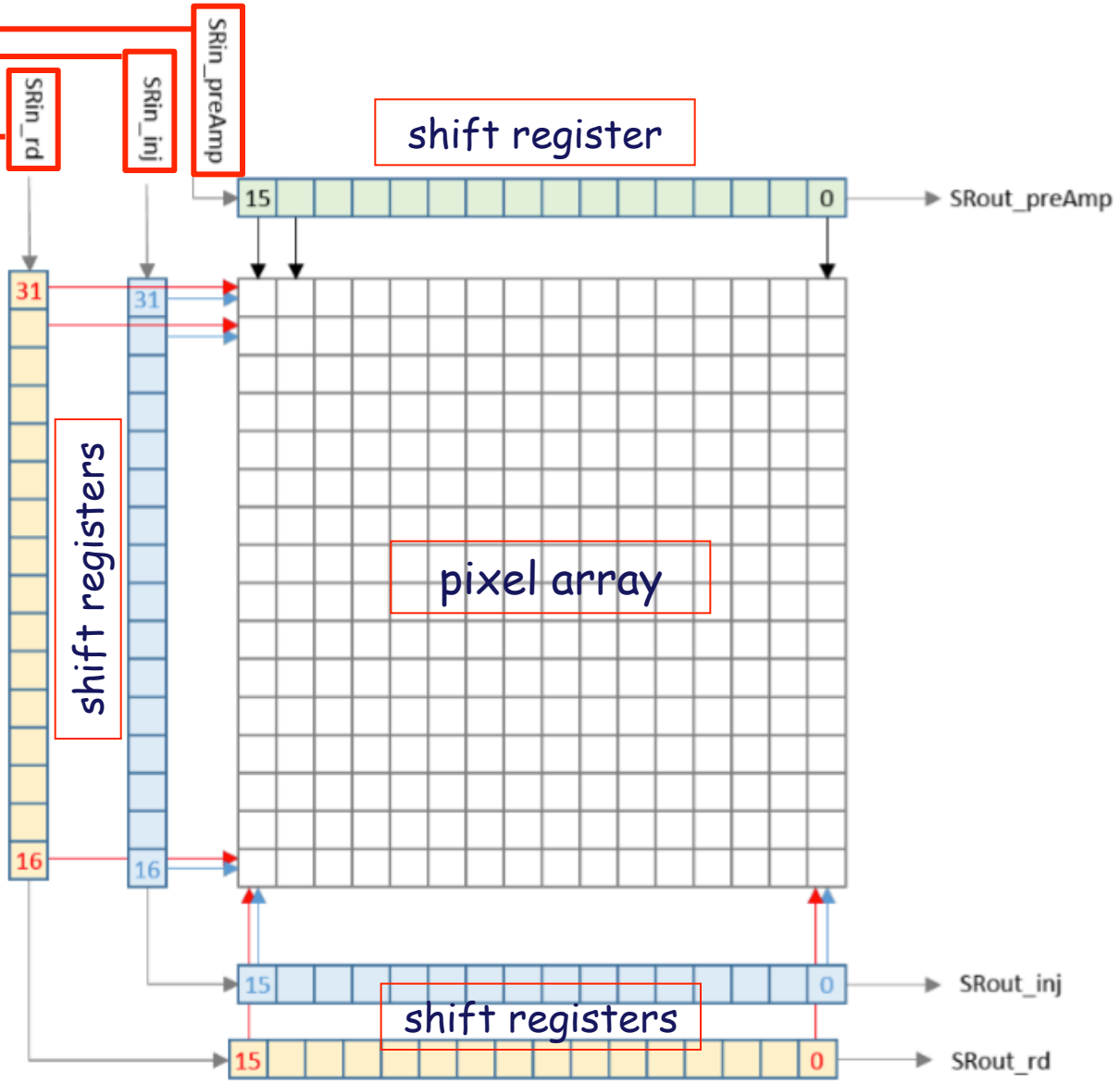
- 16 channels can be selected at a time – the outputs of the relevant preamplifiers are available from test points on the daughter board (see next slides)
- Voltage buffers (PMOS source followers) available in each pixel to drive large loads (i.e., cables to the oscilloscope)
- +5V source used to bias the buffers
- Note that the output cap, on the rising edge of the signal, is charged through the 5.5k bias resistor – e.g., if C_{load}=1 pF, τ=5 ns ➔ bandwidth limitation (low pass filtering) for the signal coming from the preamplifier ➔ low capacitance probe needed

Chip configuration

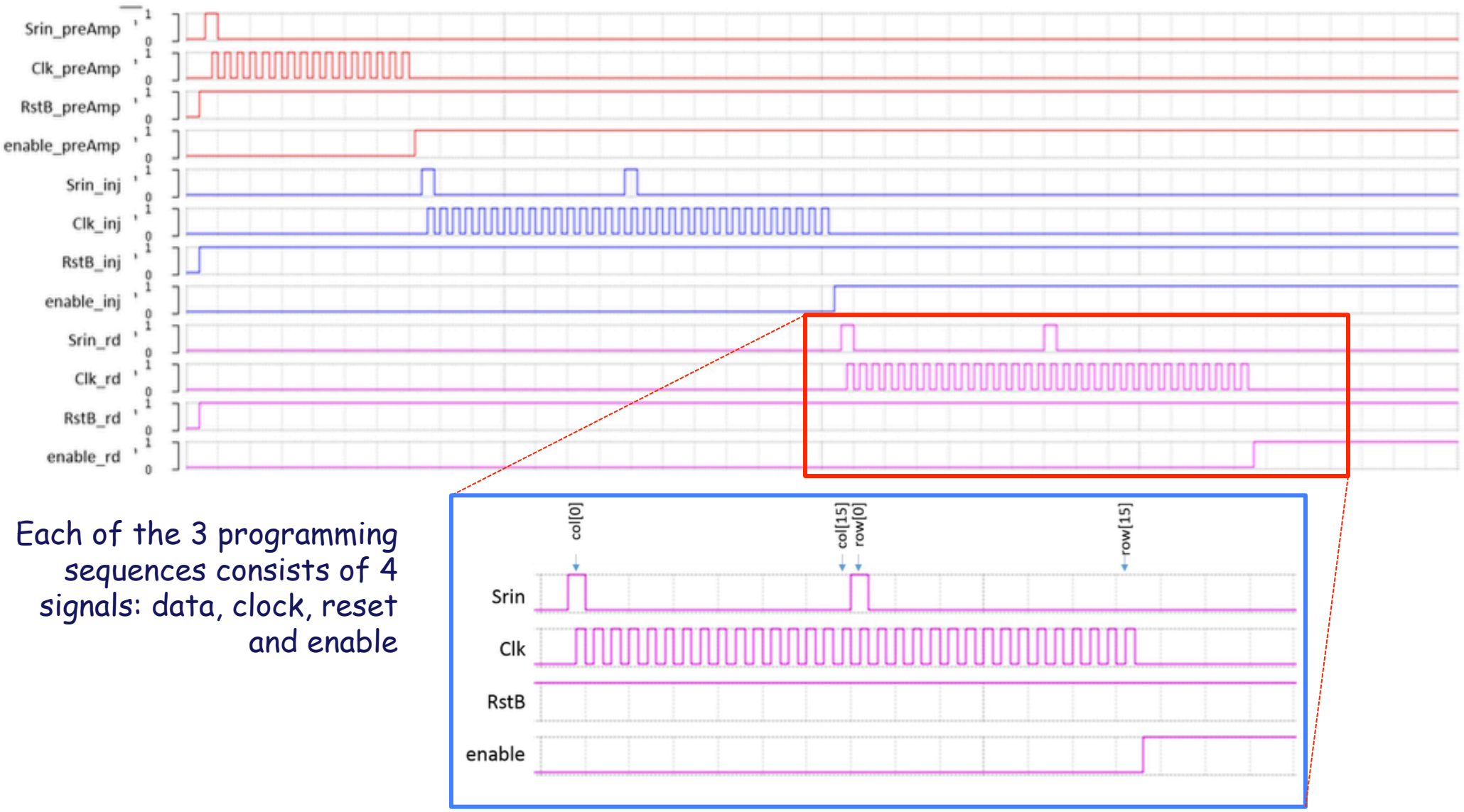
16 bit word for column selection – analog output signal from the 16 pixels is made available

32 bit word (16 bit raw address, 16 bit column address) to select one pixel to test through charge injection

32 bit word (16 bit raw address, 16 bit column address) to select one pixel to readout - digital output (1 hit comparator and 3 ADC comparators)

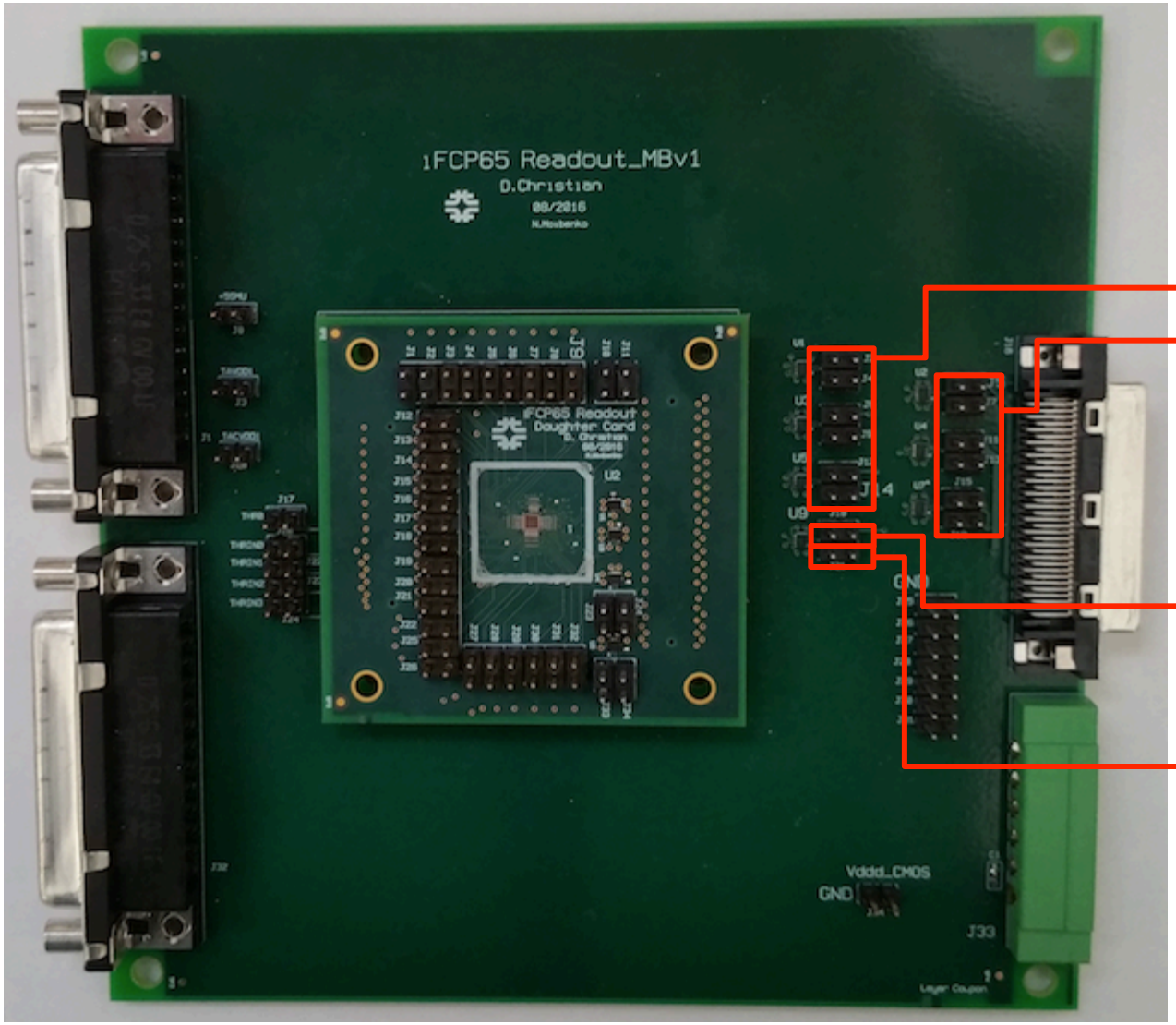


Chip configuration: sample signals



Each of the 3 programming sequences consists of 4 signals: data, clock, reset and enable

Chip configuration

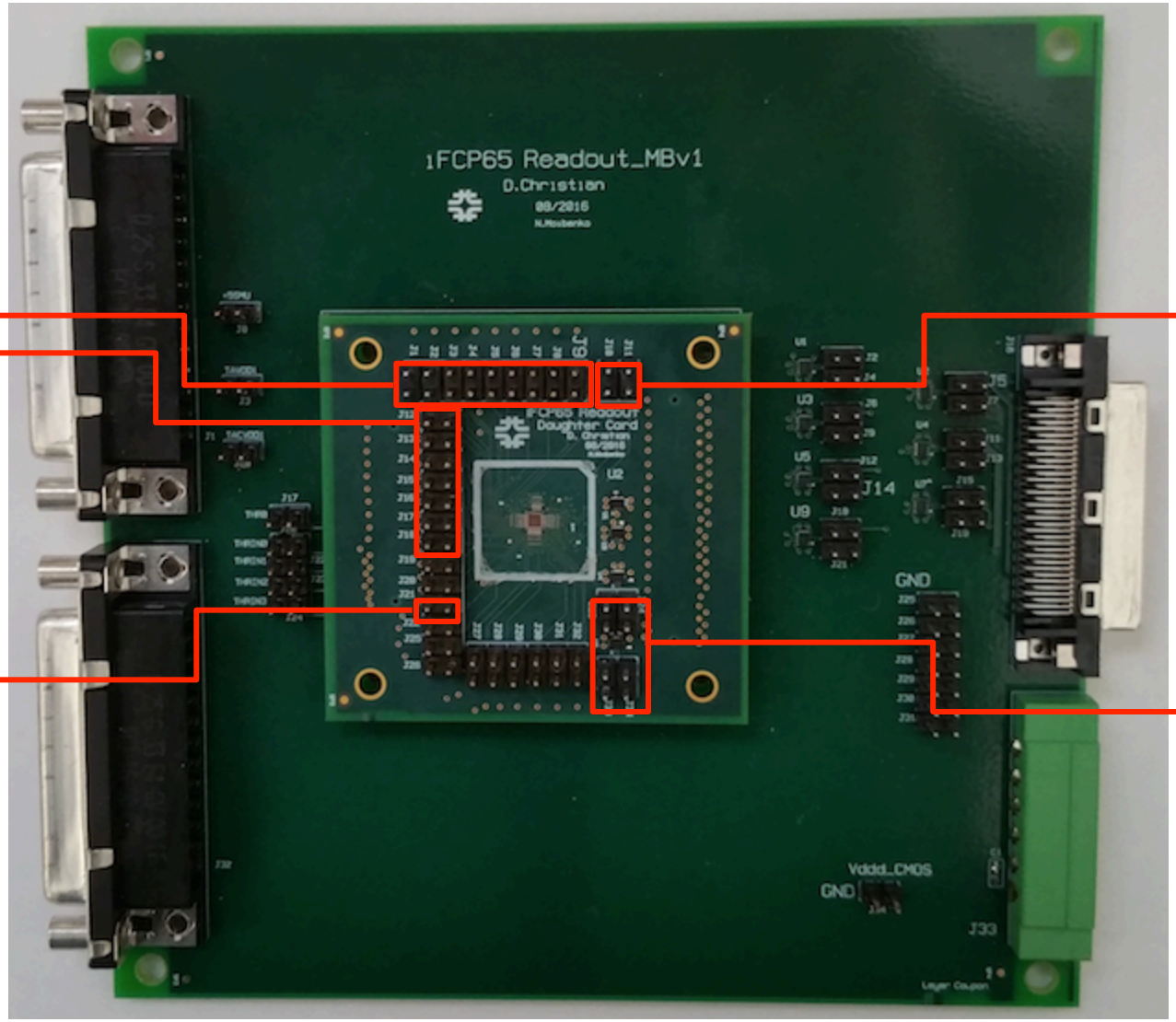


12 signals for column and pixel selection (analog output, injection, digital output)

detector emulating cap selection (0 when low, 35 fF when high)

power off – when high, ADC is off in all the pixels

Inputs and outputs



analog output (16 test points, one for each pixel in the selected column)

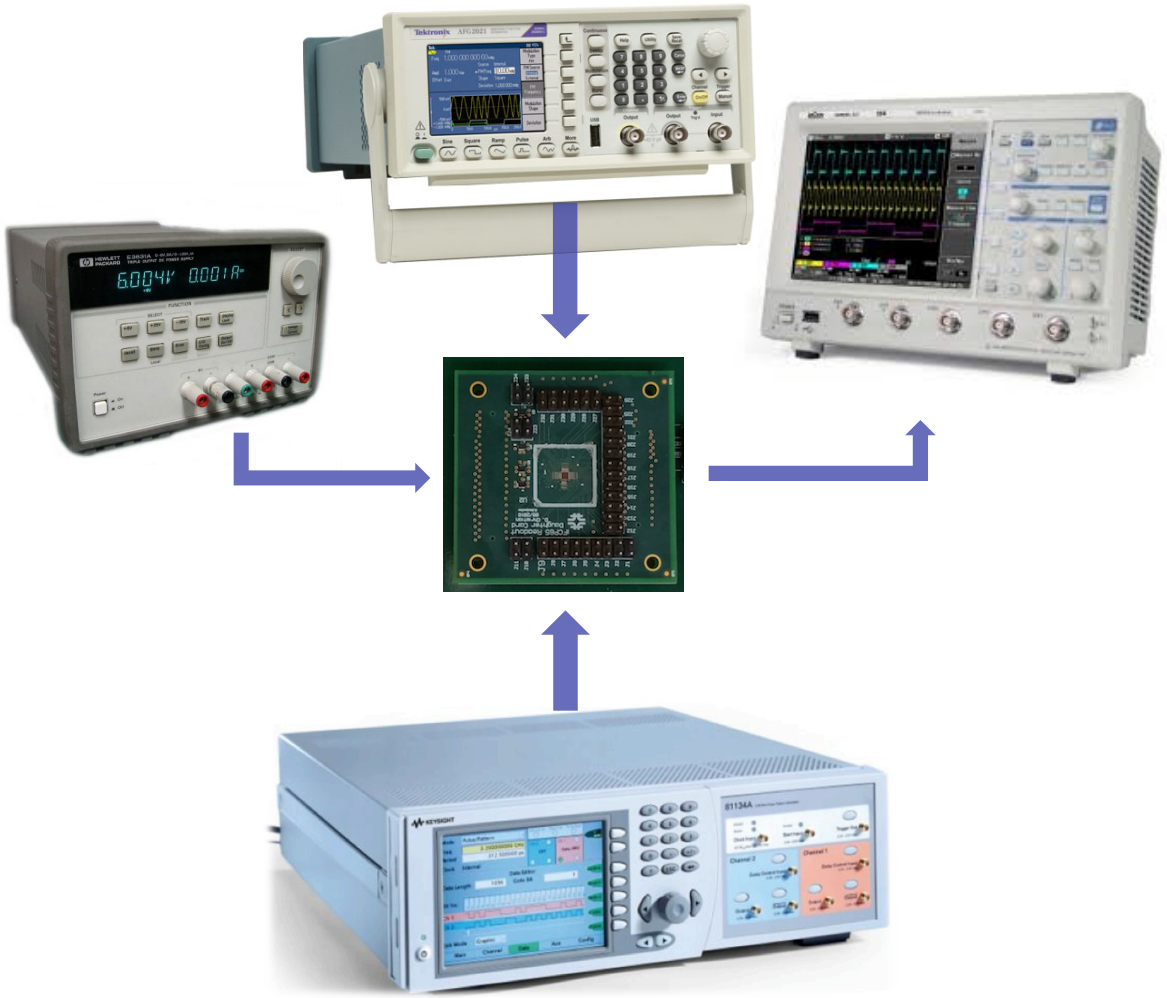
charge injection

clock and complementary clock (for discriminator operation)

comparator outputs (hit and ADC comparators)

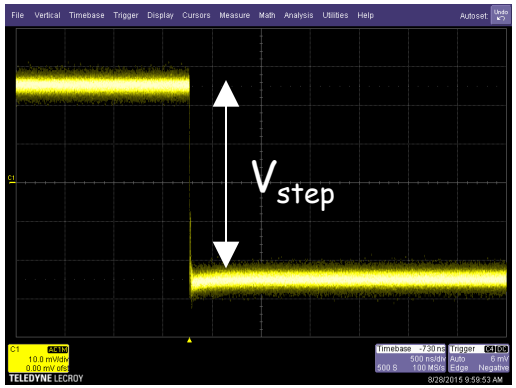
Instrumentation and prerequisites

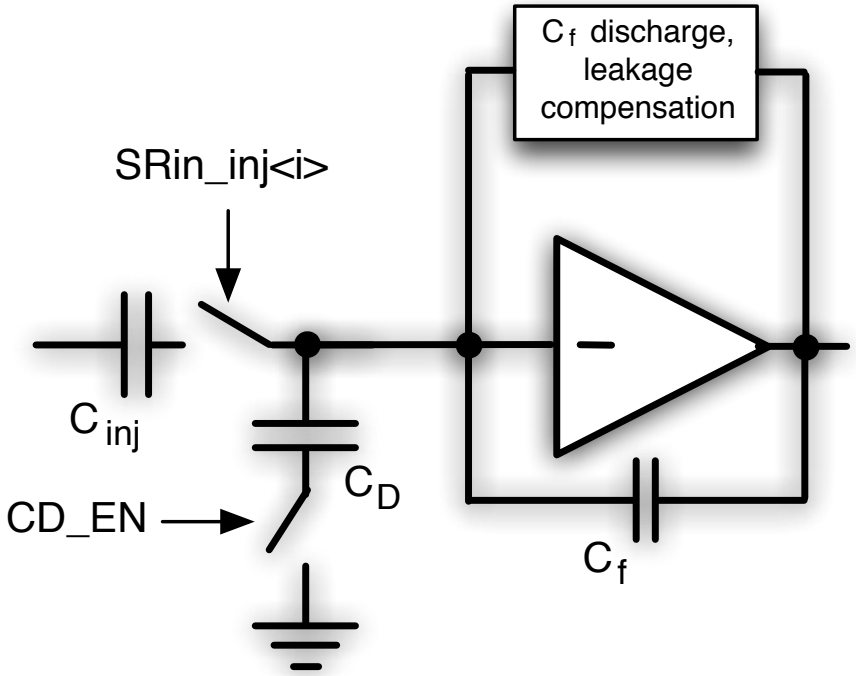
- Simple bench top instrumentation is required for measuring gain, ENC and response of the charge preamplifier and studying the behavior of the hit discriminator: power supply, digital scope, function generator, pattern generator
- No previous experience in pixel front-end characterization is required
- Basic knowledge on electronic circuit operation and standard electronic instrumentation can help

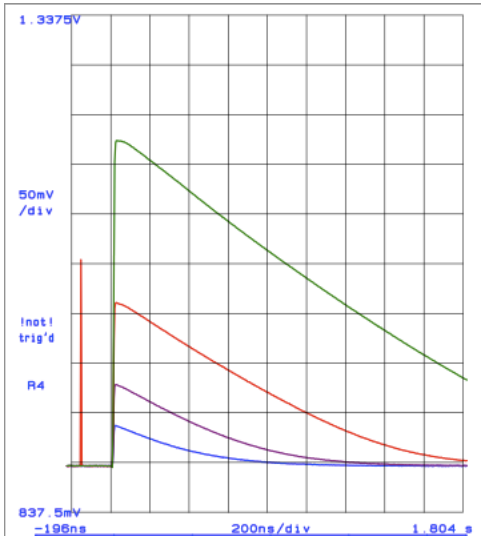


Signal at the preamplifier output

- The expected signal at a charge preamplifier input is a current pulse – it can be obtained by differentiating a voltage step signal through the injection capacitance



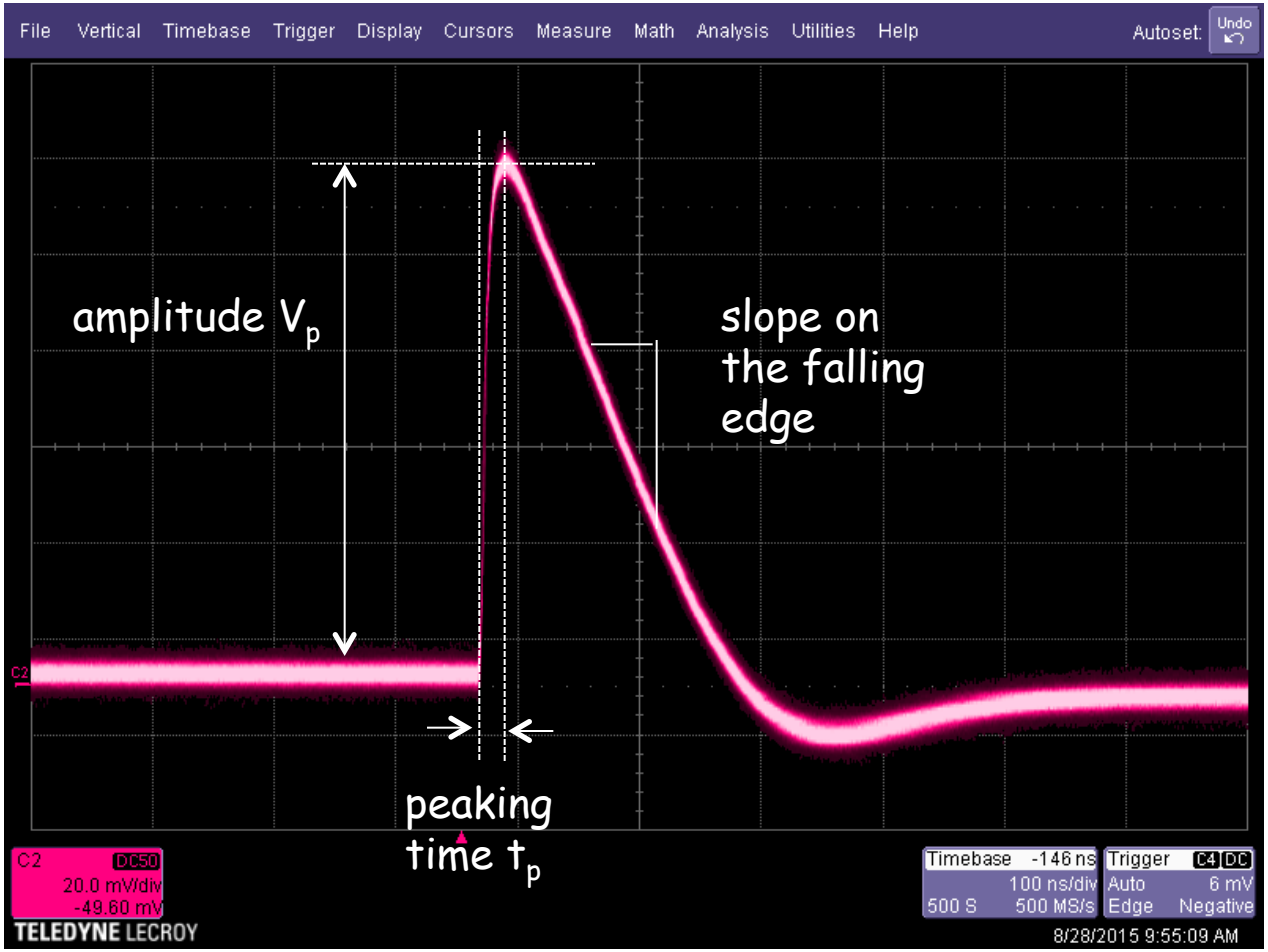




- The actual input variable is the charge $Q=C_{inj}V_{step}$

Characterization of the preamplifier response

- Main signal parameters:
  - amplitude
  - peaking time (also as a function of the detector capacitance)
  - slope on the falling edge



Peaking time variation with C_D

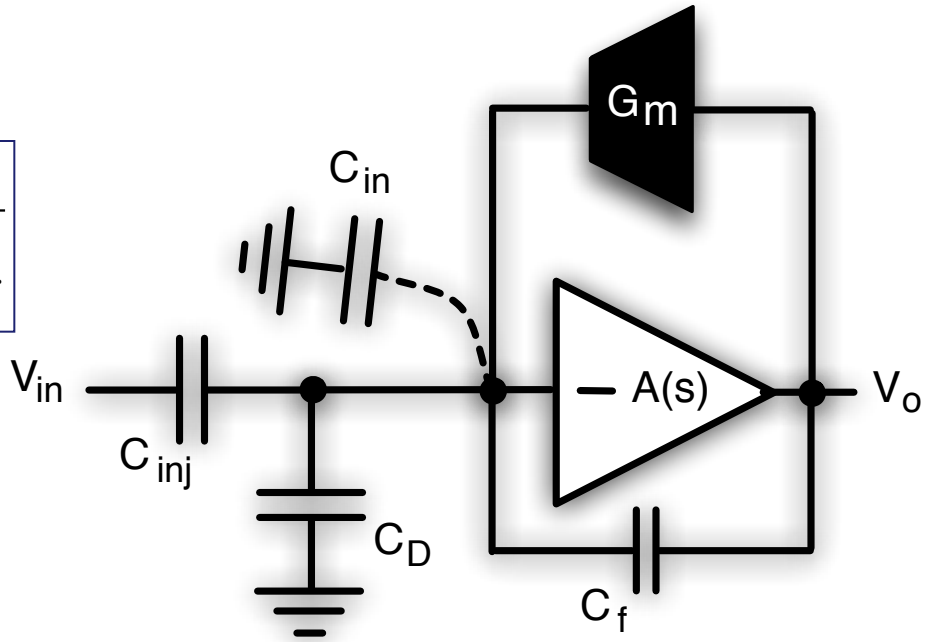
- The peaking time is found to increase with C_D: to understand why assume a single pole approximation for the gain of the forward stage

$$A(s)=\frac{A_0}{1+s\tau}$$

- The closed loop gain is

$$\frac{V_o}{V_{in}} \approx -\frac{2sC_{inj}}{G_m} \frac{1}{2s^2\tau C_T / A_0 G_m + 2s(C_T + A_0 C_f)/A_0 G_m + 1}$$

$C_T = C_D + C_{in} + C_f + C_{inj}$



- In the high frequency regime, governing the response speed of the preamplifier

$$\frac{V_o}{V_{in}} \approx -\frac{C_{inj}}{C_f} \frac{1}{s\tau C_T / A_0 C_f + 1}$$

corresponding to an exponential response (of the 1-exp(-t/τ_F) kind) with time constant

$$\tau_F \approx \tau \frac{C_D + C_{inj} + C_f + C_{in}}{A_0 C_f}$$

Charge sensitivity

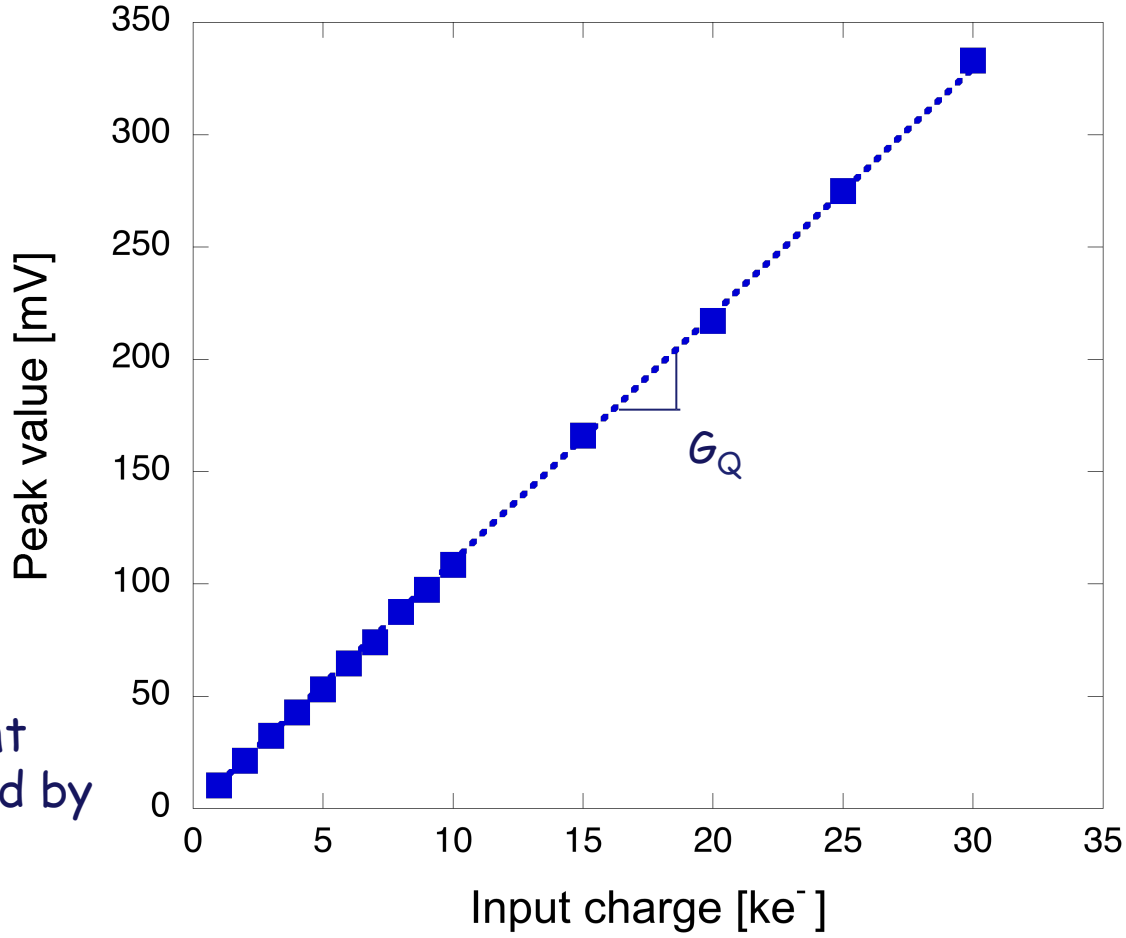
- Is defined as

$$G_Q = \frac{dV_p}{dQ}$$

- As long as the circuit is operated in the linear region

$$G_Q = \frac{V_p}{Q} \propto C_f^{-1}$$

- To avoid the effects of local, slight non-linearities, G_Q can be measured by
  - measuring the amplitude for different values of the input charge
  - linearly interpolating the data points in the amplitude vs charge plot ➔ G_Q is the slope of the interpolating straight line



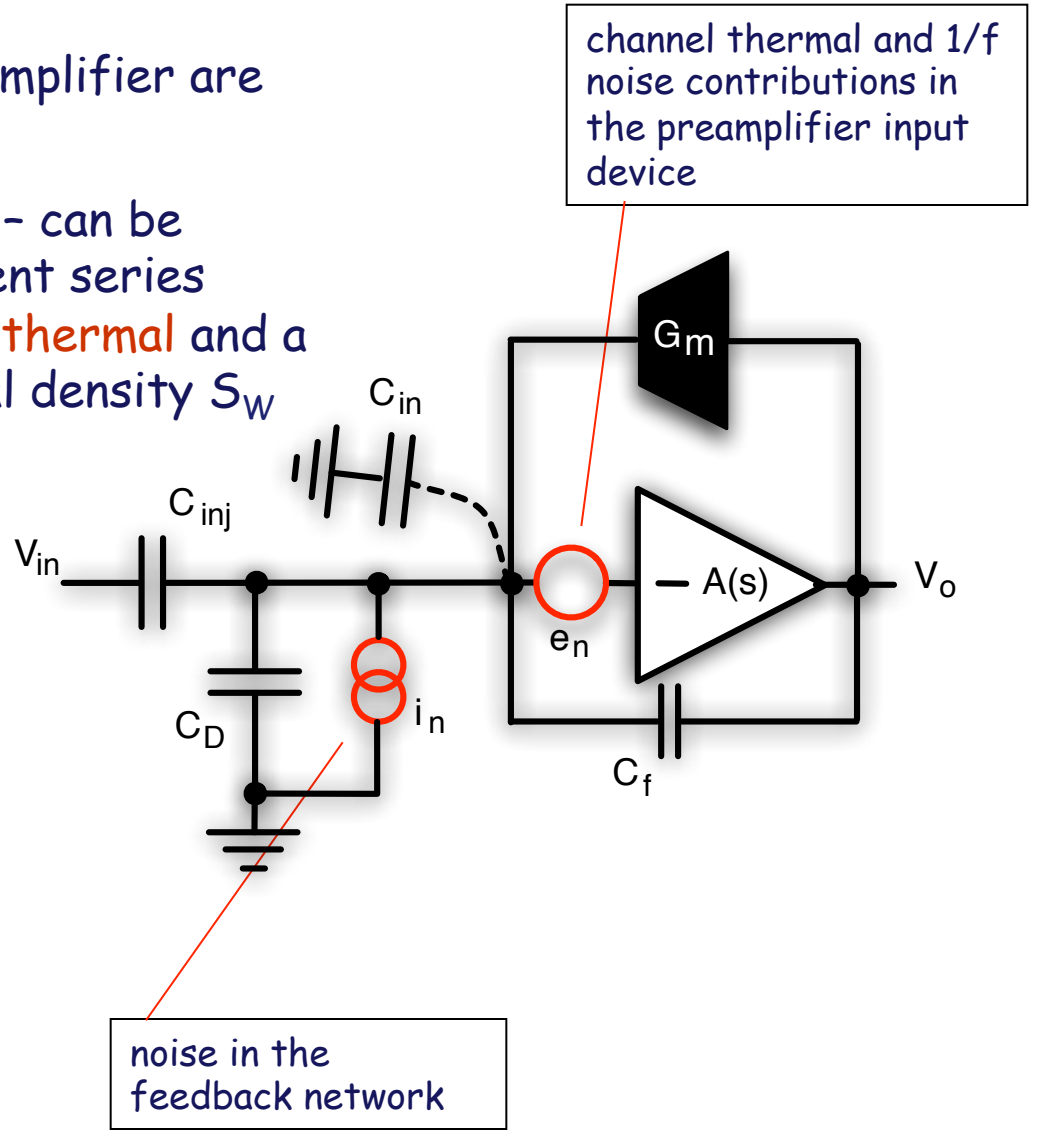
Noise and equivalent noise charge (ENC)

- The main noise sources in the preamplifier are located
  - in the preamplifier input device – can be represented through an equivalent series source (e_n) and includes a white thermal and a flicker term with power spectral density S_W and S_f respectively

$$\frac{\overline{de_n^2}}{df} = S_W + \frac{S_f}{f}$$

  - in the feedback network – can be represented through an equivalent parallel source (i_n), mostly with a white spectrum with power spectral density S_P

$$\frac{\overline{di_n^2}}{df} = S_P$$



Noise and equivalent noise charge (ENC)

- Noise in the preamplifier is responsible for some degree of inaccuracy in the measurement of the signal amplitude at the circuit output
- Noise at the channel output can be measured as the standard deviation of the signal when no stimulus is applied to the input
- One can actually sample the voltage at the channel output and compute the standard deviation σ_n as

$$\sigma_n = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2 - \left(\frac{1}{N}\sum_{i=1}^{N} x_i\right)^2}$$

x_i=i-th sample

N=# of samples

which is easily done by using the statistical functions available in virtually all digital storage scopes

Noise and equivalent noise charge (ENC)

- Equivalent noise charge is defined as the charge to be injected at the input to have an output signal with an amplitude V_P equal to the noise σ_n, or the input charge needed to have a unit signal-to-noise-ratio at the output

$$\frac{G_Q \cdot ENC}{\sigma_n} = 1 \Rightarrow ENC = \frac{\sigma_n}{G_Q}$$

- So, to measure the ENC you need measure
  - the noise at the preamplifier output
  - the charge sensitivity

- The ENC is a charge and is measured in Coulomb, but is seldom expressed in electrons

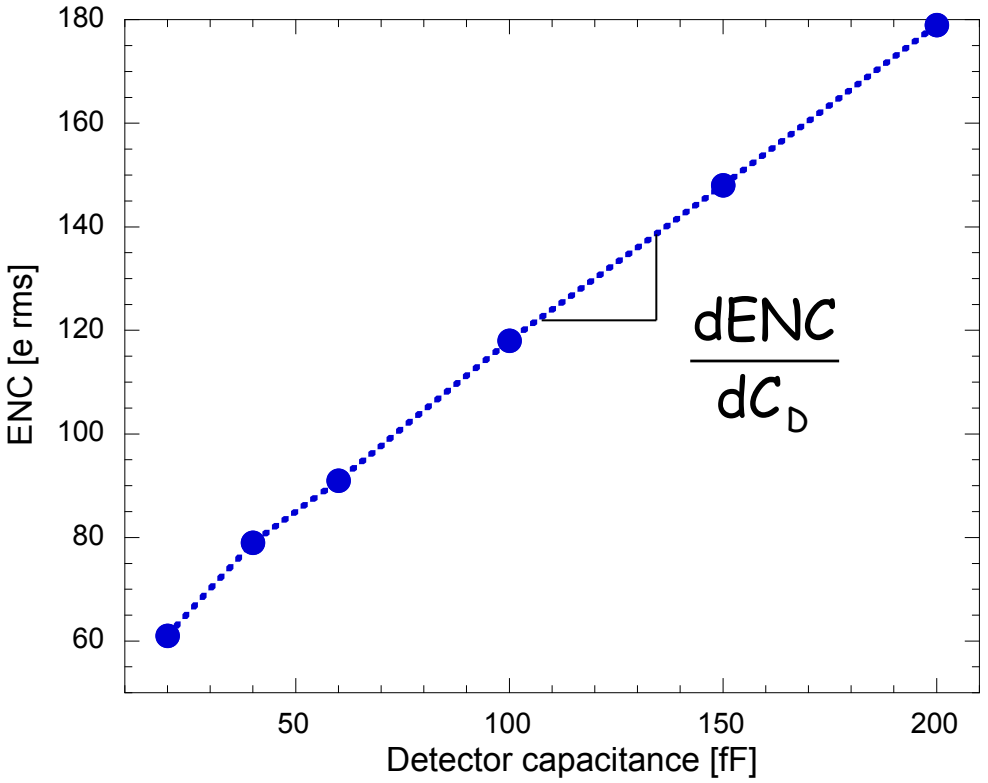
$$ENC[\text{in electrons}] = \frac{ENC[\text{Coulomb}]}{1.602 \cdot 10^{-19}\ C}$$

ENC and detector capacitance

- A quite general expression for the ENC is the following, accounting for the different noise contribution

$$ENC^2 = C_T^2 A_1 S_W \frac{1}{\tau} + C_T^2 A_2 S_f + A_3 S_p \tau$$

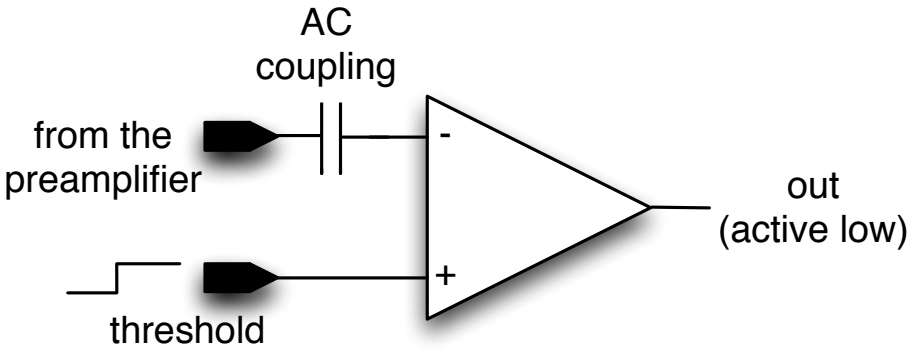
$C_T = C_D + C_{in} + C_f + C_{inj}$
A_1, A_2, A_3=shaping coefficient
τ=shaping time (has some relationship with t_p)



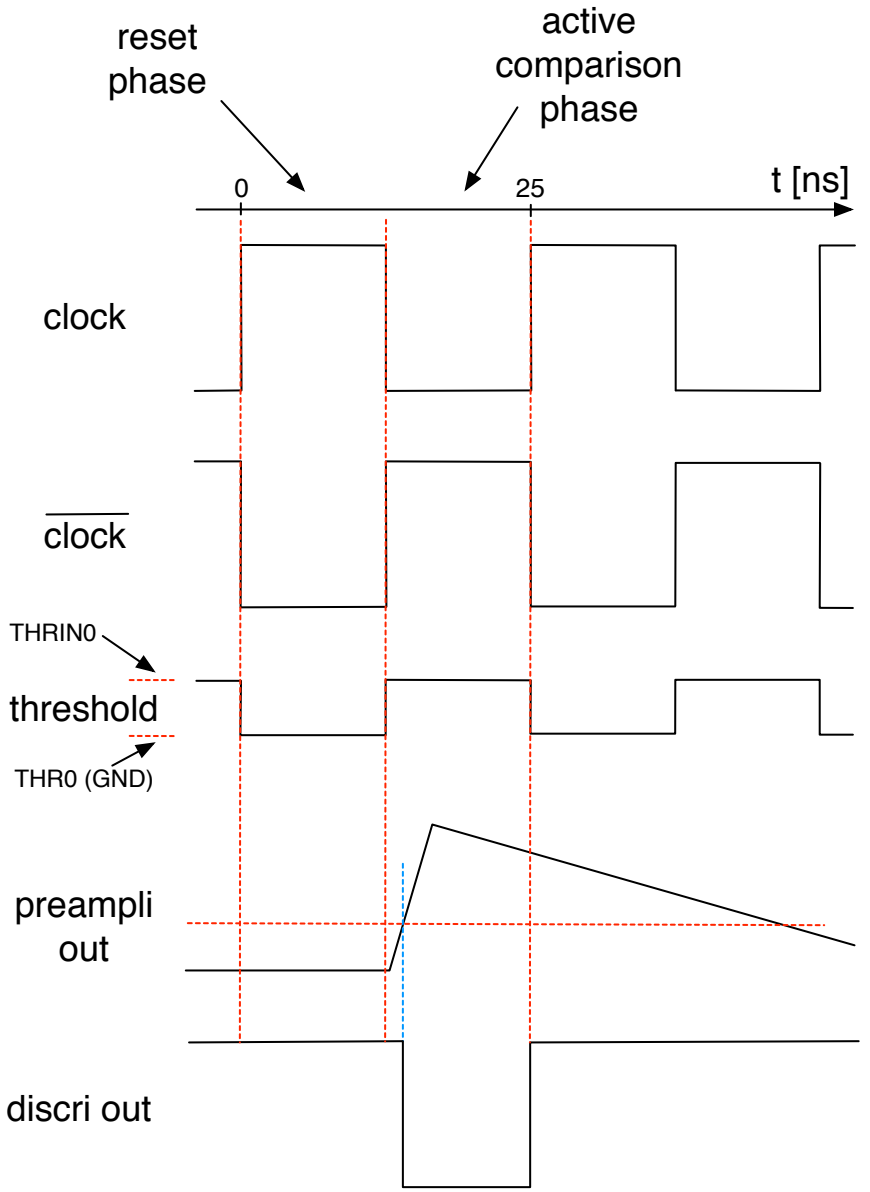
- The effect of the series noise source on the overall noise performance gets more pronounced as C_T (the capacitance shunting the circuit input terminal) increases

- The slope of the ENC vs C_D is a figure of merit telling us how the noise performance of the circuit degrades as the detector capacitance increases

Discriminator operation

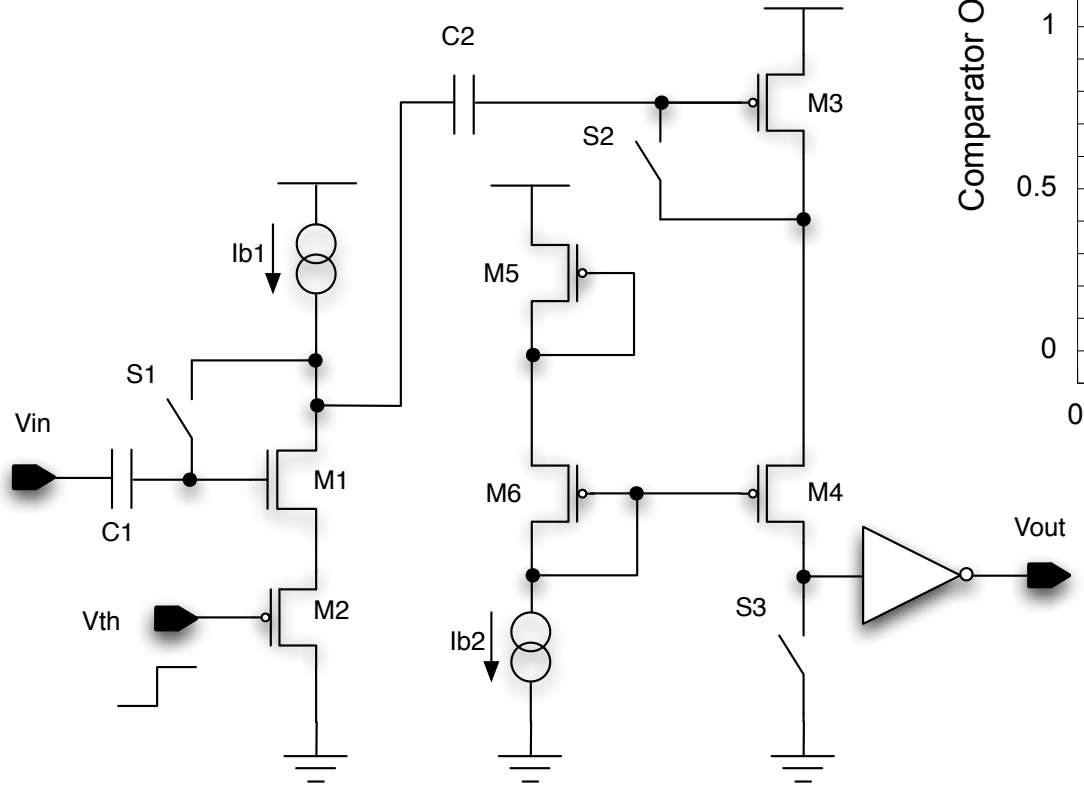


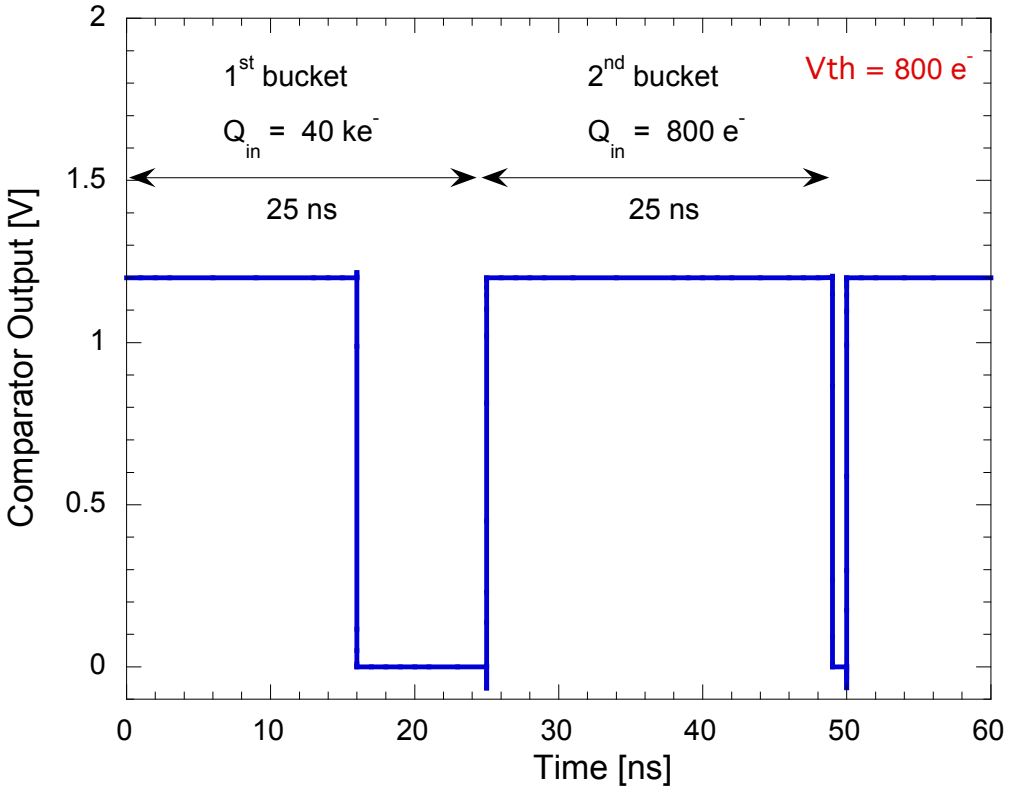
- Operation based on a reset and an active comparison phase
  - reset phase: comparator out (active low) is set to 1
  - comparison phase: preamplifier out is compared with a threshold
- AC coupling between preamplifier and discriminator → only positive changes in the preamplifier output signals are effective in triggering the discriminator
- Reset every 25 ns ensures zero dead time operation (25 ns is the bunch crossing period at the HL-LHC ➔ potential detection of an event every 25 ns)



Discriminator architecture

- 1 uA current consumption
- Threshold step is generated in the pixel





- The comparator should be capable of detecting a signal just above threshold after detecting a very large signal in the previous time slot