Lab session on pixel front-end characterization

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Focus of the lab

Pixel front-end ASICs are located at the very beginning of the signal processing chain in pixel based detectors used in many fundamental and applied research fields.

Experimental characterization of front-end circuits in advanced microelectronic technologies is an integral part of the implementation of modern radiation detection systems.

The focus of the lab will be the characterization of a front-end channel for pixel detectors in a 65 nm CMOS technology.

The circuit under test was developed for the upgrade of the innermost layer of the CMS pixel detector - to be deployed at the future High Luminosity Large Hadron Collider (HL-LHC).
In the phase 2 upgrade of the ATLAS and CMS experiments at the LHC, the inner layers of the pixel trackers will have to face some serious challenges:

- very high hit rates: $1 - 2 \text{ GHz/cm}^2$ → need of intelligent pixel level data processing
- very high radiation levels: 1 Grad total ionizing dose, $10^{16} \text{ neutrons/cm}^2$ fluence
- very high trigger rates: 1 MHz
- small pixel cells: $50 \times 50 \text{ um}^2$ (or $25 \times 100 \text{ um}^2$) → improve resolution and reduce occupancy
- small power dissipation: $\sim 10 \text{ uW per cell}$ (including analog and digital sections)

Optimum front-end design requires a trade-off between noise, area, speed, power dissipation, amount of in-pixel functions.

The **65 nm CMOS process** in its low power (LP) flavor is optimized for a reduced leakage and a small power consumption (at the price of a lower speed).
Readout channel implementing a zero dead-time design - hit detection takes no more than 25 ns

- Leakage current compensation up to 10 nA
- Hit comparator based on “praying mantis” architecture - 12.5 ns reset phase + 12.5 ns comparison phase
- 2-bit flash ADC (3 discriminators, same as the hit comparator) for amplitude measurements
Chip layout

Chip developed by:
Davide Braga,
David Christian,
Grzegorz Deptuch,
Farah Fahim,
Luigi Gaioni,
Benedetta Nodari,
Lodovico Ratti,
Valerio Re,
Thomas Zimmermann

Design by:
Davide Braga,
Luigi Gaioni,
Benedetta Nodari
Test setup

Chip on a small daughter board mounted on a test PCB, with connectors for power, bias, slow control (chip configuration), input and output (both digital and analog) signals.
Instrumentation and prerequisites

- Simple bench top instrumentation is required for measuring gain, ENC and response of the charge preamplifier and studying the behavior of the hit discriminator: power supply, digital scope, function generator, pattern generator.

- No previous experience in pixel front-end characterization is required.

- Basic knowledge on electronic circuit operation and standard electronic instrumentation can help.