Computing Labs

Multi-/Many-Core Programming with Intel Xeon Phi Coprocessors

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“JÚLIO DE MESQUITA FILHO”
Intel Modern Code Community

UNESP CSC is an official Intel Modern Code Partner for Latin America


The São Paulo State University – UNESP (Univ. Estadual Paulista), part of the state of São Paulo public higher education system, is one of the largest universities in Brazil, and its Center for Scientific Computing (CSC) operates two large Linux-based clusters to support the university research community. As high-performance computing moves toward the exascale era, many current scientific applications are unable to exploit modern manycore computing environment. To take this challenge, UNESP CSC and Intel established a new partnership focused on code modernization and dissemination of improvements and innovations in parallel processing.
Lab Sessions

• Hands-on activities split into 2 ~ 3 hour sessions
• Learner proceeds from one topic to the next at his/her own speed

Lab Session 1

• Starts with a short demo on how to access the **remote systems**
• Continues with a **high-performance test-drive**, where the participants are guided to extract **the maximum performance of the coprocessor**
• Finishes with the **benchmarking** of a simple scientific application (N-body simulation)

Lab Session 2

• Starts with an overview of task **parallelism** with **OpenMP** and **Cilk Plus**
• Continues with an overview of process **parallelism** using **MPI**
• Concludes with a step-by-step **optimization** of a real-word code example (diffusion simulation algorithm)
Lab Session 1

1. Introduction to the Intel Xeon Phi Coprocessor
   - Overview of the hardware architecture
   - Overview of the system software and programming models

2. Compiling and running simple applications

3. High-performance Test-Drive

4. Running a basic N-body simulation
Lab Session 2

1. Task Parallelism with OpenMP and Cilk Plus
   • Overview of OpenMP
   • Overview of Cilk Plus
   • Overview of Intel Advisor

2. Process Parallelism: MPI programming models

3. Using Intel Math Kernel Library (MKL)

4. Optimizing a real-world code example
Intel / UNESP servers for the labs

• Host Server 1 [Xeon + Xeon Phi (KNC)]
  • 2x Intel(R) Xeon(R) CPU E5-2699 v3 @ 2.30GHz, 18 cores
  • 128 GB DDR4 memory, 2x 1 TB (7200 rpm) disks
  • Intel 750 Series NVMe PCIe SSD card (1.2 TB)
  • 2x 1Gb Ethernet ports
  • Ethernet 40 Gb / Infiniband 56 Gb/s FDR card
  • 5x Intel Xeon Phi KNC 5110P @ 1.1 GHz, 8 GB GDDR5, 60 cores

• Host Server 2 [Xeon Phi (KNL)]
  • 1x Intel(R) Xeon Phi(TM) CPU 7250 @ 1.40GHz
  • 192 GB memory, 2 TB (7200 rpm) disk
  • Ethernet 2x Gigabit
Intel Xeon Phi servers (KNC)

- Intel Xeon Phi
  - 5110P
  - 7120P
## Intel Xeon Phi (KNC) versions

<table>
<thead>
<tr>
<th>Product Number</th>
<th>Form Factor &amp; Thermal Solution</th>
<th>Board TDP (Watts)</th>
<th>Number of Cores</th>
<th>Frequency (GHz)</th>
<th>Peak Double-Precision Performance (GFLOP)</th>
<th>Peak Memory Bandwidth (GB/s)</th>
<th>Memory Capacity (GB)</th>
<th>Intel® Turbo Boost Technology</th>
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Intel Xeon Phi KNL workstation

- Internal Fan
- Intel® Xeon® Phi x200 up to 260W
- 6 DIMM Slots DDR4
- 2 PCI-E 3.0 x16 Slots
- PCI-E 3.0 x4 Slot
- 750W Multi-output Power Supply
- 3x 3.5” tool-less drive bays
- 4x 2.5” tool-less drive bays
- 3x 3.5” tool-less drive bays
- 10 SATA3 Ports
- Liquid cooling system

[Image of Intel Xeon Phi KNL workstation with labels]
Intel Xeon PHI KNL versions

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<tr>
<th></th>
<th>Cores</th>
<th>Ghz</th>
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<th>Fabric</th>
<th>DDR4</th>
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Learn more: [www.intel.com/xeonphi](http://www.intel.com/xeonphi)
Thank you!

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