4th Summer School on INtelligent signal processing for FrontIEr Research and Industry

Computing Labs

Multi-/Many-Core Programming with Intel Xeon Phi Coprocessors

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UNIVERSIDADE ESTADUAL PAULISTA
"JÚLIO DE MESQUITA FILHO"

Intel Modern Code Community

UNESP CSC is an official Intel Modern Code Partner for Latin America
https://software.intel.com/en-us/modern-code/live-workshops

Núcleo de Computação Científica - UNESP

The São Paulo State University – UNESP (Univ. Estadual Paulista), part of the state of São Paulo public higher education system, is one of the largest universities in Brazil, and **its Center for Scientific Computing (CSC) operates two large Linux-based clusters to support the university research community.** As high-performance computing moves toward the exascale era, many current scientific applications are unable to **exploit modern manycore computing environment**. To takle this challenge, **UNESP CSC and Intel** established a new **partnership focused on code modernization and dissemination of improvements and innovations in parallel processing.**

Lab Sessions

- Hands-on activities split into 2 ~ 3 hour sessions
- Learner proceeds from one topic to the next at his/her own speed

Lab Session 1

- Starts with a short demo on how to **access** the **remote systems**
- Continues with a **high-performance test-drive**, where the participants are guided to extract **the maximum performance of the coprocessor**
- Finishes with the **benchmarking** of a simple scientific application (N-body simulation)

Lab Session 2

- Starts with an overview of task **parallelism** with **OpenMP** and **Cilk Plus**
- Continues with an overview of process **parallelism** using **MPI**
- Concludes with a step-by-step **optimization** of a real-word code example (diffusion simulation algorithm)

Lab Session 1

1. Introduction to the Intel Xeon Phi Coprocessor
- Overview of the hardware architecture
- Overview of the system software and programming models

2. Compiling and running simple applications

3. High-performance Test-Drive

4. Running a basic N-body simulation

Lab Session 2

1. Task Parallelism with OpenMP and Cilk Plus
- Overview of OpenMP
- Overview of Cilk Plus
- Overview of Intel Advisor

2. Process Parallelism: MPI programming models

3. Using Intel Math Kernel Library (MKL)

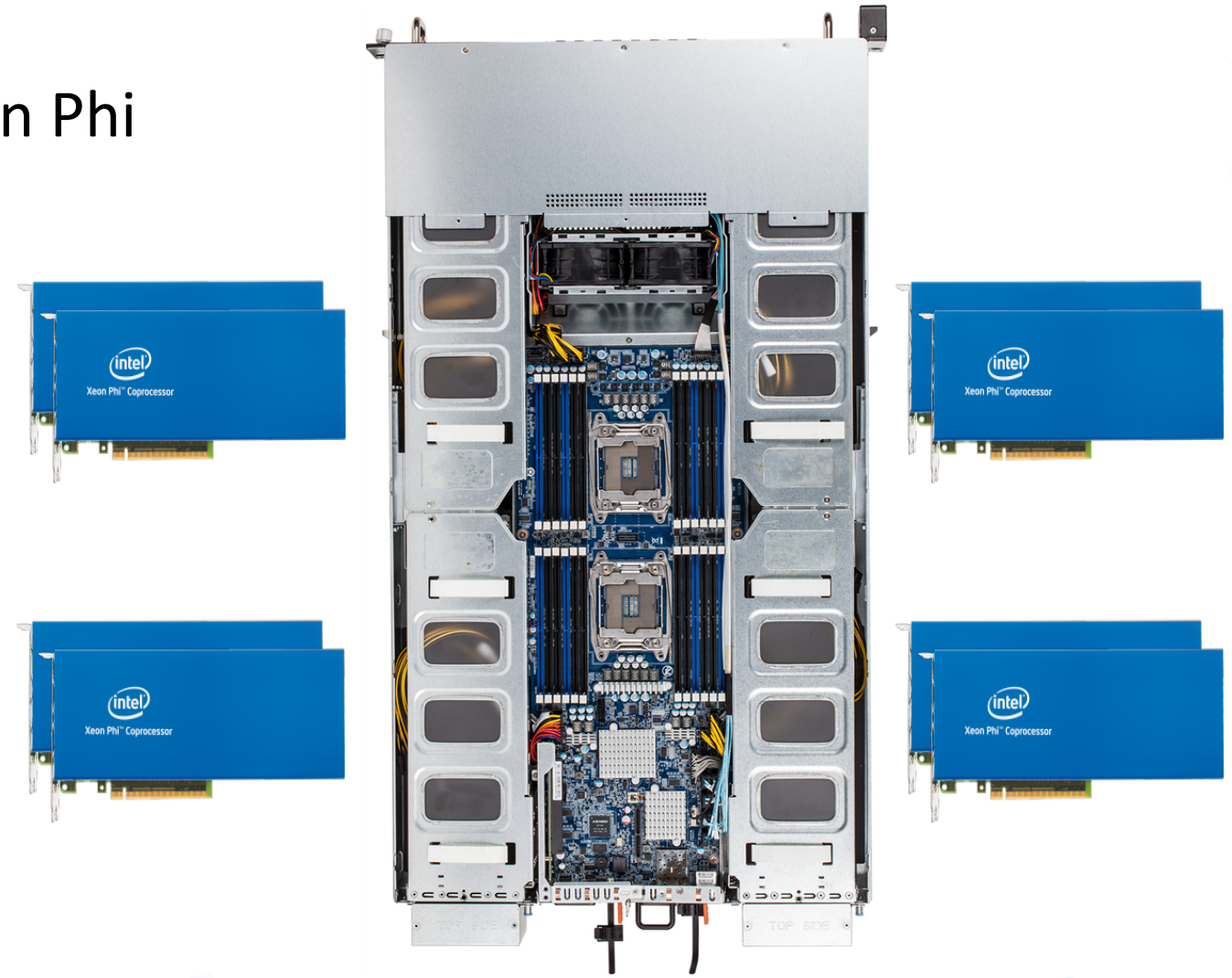
4. Optimizing a real-world code example

Intel / UNESP servers for the labs

- Host Server 1 [Xeon + Xeon Phi (KNC)]
  - 2x Intel(R) Xeon(R) CPU E5-2699 v3 @ 2.30GHz, 18 cores
  - 128 GB DDR4 memory, 2x 1 TB (7200 rpm) disks
  - Intel 750 Series NVMe PCIe SSD card (1.2 TB)
  - 2x 1Gb Ethernet ports
  - Ethernet 40 Gb / Infiniband 56 Gb/s FDR card
  - 5x Intel Xeon Phi KNC 5110P @ 1.1 GHz, 8 GB GDDR5, 60 cores
- Host Server 2 [Xeon Phi (KNL)]
  - 1x Intel(R) Xeon Phi(TM) CPU 7250 @ 1.40GHz
  - 192 GB memory, 2 TB (7200 rpm) disk
  - Ethernet 2x Gigabit

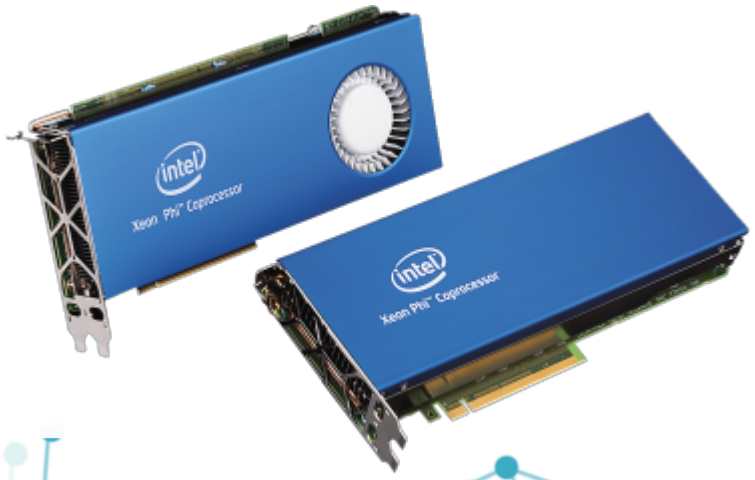
Intel Xeon Phi servers (KNC)

- Intel Xeon Phi
  - 5110P
  - 7120P

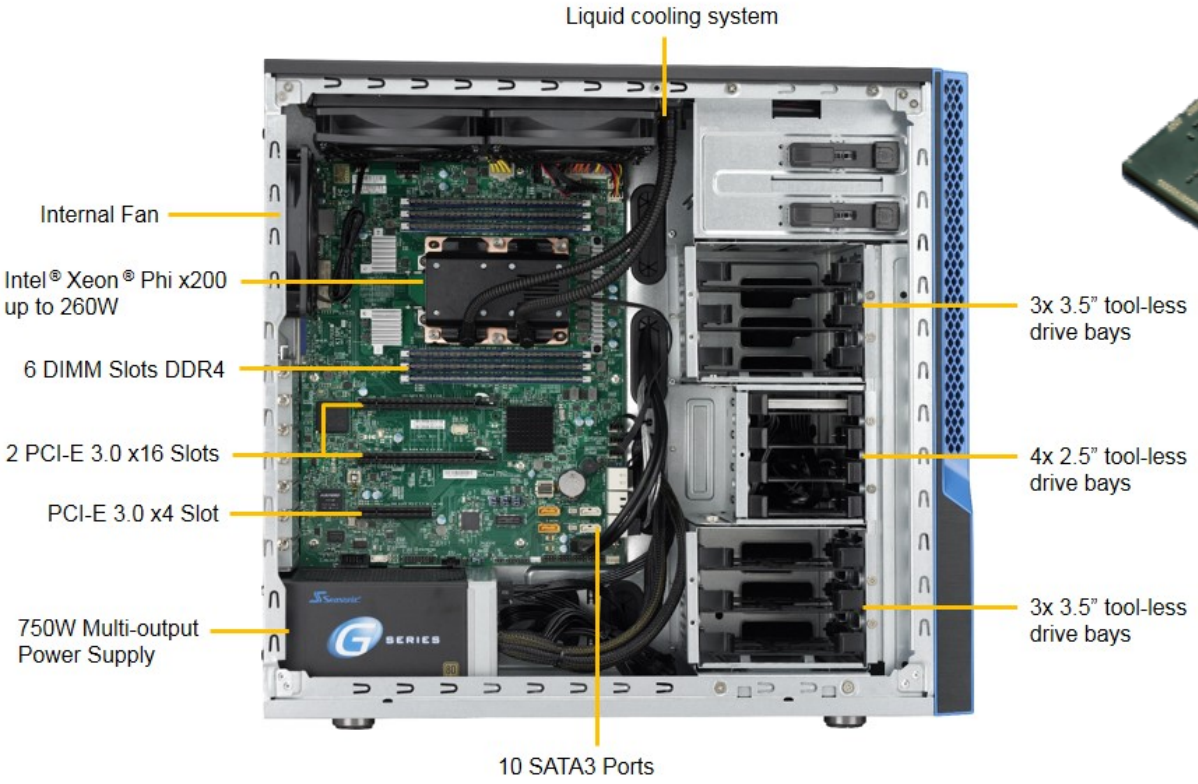


Intel Xeon Phi (KNC) versions

PRODUCT NUMBER	FORM FACTOR &, THERMAL SOLUTION[4]	BOARD TDP (WATTS)	NUMBER OF CORES	FREQUENCY (GHz)	PEAK DOUBLE PRECISION PERFORMANCE (GFLOP)	PEAK MEMORY BANDWIDTH (GB/s)	MEMORY CAPACITY (GB)	INTEL® TURBO BOOST TECHNOLOGY
3120P	PCIe, Passive	300	57	1.1	1003	240	6	N/A
3120A	PCIe, Active	300	57	1.1	1003	240	6	N/A
5110P	PCIe, Passive	225	60	1.053	1011	320	8	N/A
5120D	Dense form factor, None	245	60	1.053	1011	352	8	N/A
7110P	PCIe, Passive	300	61	1.238	1208	352	16	Peak turbo frequency: 1.33 GHz
7120X	PCIe, None	300	61	1.238	1208	352	16	



Intel Xeon Phi KNL workstation



Intel Xeon PHI KNL versions

			INTEGRATED			
	Cores	Ghz[3]	Memory	Fabric*	DDR4	Power
7290* Best Performance/Node	72	1.5	16GB 7.2 GT/s	Yes	384GB 2400 MHz	245W +15W fabric
7250 Best Performance/Watt	68	1.4	16GB 7.2 GT/s	Yes	384GB 2400 MHz	215W +15W fabric
7230 Best Memory Bandwidth/Core	64	1.3	16GB 7.2 GT/s	Yes	384GB 2400 MHz	215W +15W fabric
7210 Best Value	64	1.3	16GB 6.4 GT/s	Yes	384GB 2133 MHz	215W +15W fabric

Learn more: www.intel.com/xeonphi

Thank you!

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