A SEED FILTER + LINEAR REGRESSION FITTER FOR THE TIME MULTIPLEXED TRACK TRIGGER

The Time Multiplexed Track Trigger

The Time Multiplexed Track Trigger (TMTT) is one of the main proposal for the architecture of the future L1 Track Trigger system for the Phase II upgrade of the Compact Muon Solenoid (CMS) experiment. Goal of the Track Trigger is to find track candidates from a series of hits (stubs) in the outer tracker detector.

In the TMTT approach the L1 Track Finding task is achieved by means of FPGA circuits. To handle with the high bandwidth coming out from the tracker detector, this has been divided in 8 segments (octants) along the azimuthal angle Φ. Data from each octant are analysed by a single L1 Track Finder Processor (TFP), where the L1 Track Finding algorithm has been implemented. The algorithm has been divided in several blocks, each of them running on a separate FPGA for the purpose of the hardware demonstrator. Tracker data are first organised and converted in the Geometric Processor (GP), then candidate tracks in the RØ are found using the Hough Transform (HT) technique. Downstream HT candidates are filtered and fitted in the Track Fitter processor (TF). Finally a duplicate removal (DR) step get rid of the surviving duplicate tracks.

The Seed Filter Algorithm

The Seed Filter identifies and eliminates stubs assigned to tracks by the HT that lie tens of centimetres from the track in the RØ plane.

1. Collects pairs of stubs, which belong to different PS layers (blue)
2. Computes lines passing through those stubs (seeds)
3. Discards seeds that would correspond to tracks out of the beam-spot and sector definition
4. Extrapolates surviving seeds to other tracker layers, keeping only one stub per layer
5. Only tracks that still contain enough stubs in different layers are kept

The Linear Regression Fitter

Tracks with sufficient pT should draw a straight line on both RØ and RΖ planes. The Linear Regression Fitter fits the helix parameters using independent straight line fit in the two planes with Linear Regression technique.

1. Calculates the helix parameters on the RØ plane
2. Remove from the track the stubs with the largest residual, keeping at least two stubs in the PS layers
3. Calculates again the helix parameters, also in the RΖ plane, using only stubs in the PS layers
4. Computes the y2 and rejects tracks with a y2 larger than a predefined cut

\[
\begin{align*}
\chi^2 & = \sum_i \left( \frac{(y_i - \hat{y}_i)^2}{\sigma_i^2} \right) \\
q/p & = \frac{\text{ reconstructed charge/pitch } \phi}{\text{ pitch } \phi} \\
\text{RØ} & = \frac{R^n - R^s}{R^m - R^e} \\
\text{RΖ} & = \frac{Z^n - Z^s}{Z^m - Z^e}
\end{align*}
\]

Firmware Implementation

The algorithm has been implemented in a Virtex 7 FPGA, mounted on a pTCA MP7 board. Stubs from each HT output channel are stored in a separate FIFO (Track Locator). The Control Unit (CU) reads out stubs, belonging to the same track candidate, from the Track Locators and send them to the first available Seed Filter + Linear Regression (SF+LR) module. Stubs from the next candidate are sent to the next free module and so on. Each CU handles 5 Track Locator and 4 SF+LR block.

The filter algorithm is implemented in the SF block, which processes a HT candidate at the time. If the candidate passes the filter, the surviving stubs are sent to the downstream LR module, where eventually a pipelined chain computes the fit parameters.

<table>
<thead>
<tr>
<th>Module (hit)</th>
<th>Track Locator 9-5</th>
<th>Track Locator 6-11</th>
<th>Track Locator 12-17</th>
<th>Track Locator 16-23</th>
<th>Track Locator 24-29</th>
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<tr>
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Latency ~635 ns @ 240 MHz

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