Verilog modeling of a Region-Of-Interest (ROI) Fast L1 pixel Track Trigger strategy for LHC

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Abstract

In the framework of the Level-1 pixel based track trigger for CMS studies, a novel and intelligent digital architecture has been proposed, in order to focus the efforts of the front-end on the implementations of three main features: a novel data sparsification method, a clusterisation scheme at the hardware level itself and especially fast Region-Of-Interest (ROI) trigger capability. The ongoing work focuses on the Verilog simulation of a ROI fast L1 trigger strategy, similar to the one of FEI4-b for ATLAS experiment.

Introduction on L1 pixel based track trigger for CMS study

A series of feasibility studies have been conducted in order to investigate the performances and motivations for a Level-1 trigger based on pixel information (so-called L1 pixel trigger) [1], in the framework of the High Luminosity LHC. Such a type of L1 trigger can provide the ability to efficiently select leptons and to achieve a high rejection factor in high-rate collision environment. Pixel tracking information also provides precise primary vertex determination especially along the beam axis (for the tagging of b-quarks i.e. the secondary vertex determination). The physics motivations cover several physics cases: electroweak standard physics, new physics phenomena with leptons and other interesting cases.

The L1 pixel trigger is a seeded trigger unlike the L1 outer track trigger. It is based on the pull strategy which defines the ROI where to look in the pixel device. Two cases are considered:
• Use L1 track trigger from outer tracker: L1 track the seed;
• Use L1 tower from e-magnetic calorimeter trigger as seed.

The main technical challenges for the Phase-2 Pixel Read-Out-Chip (ROC) associated with a pixel-based L1 trigger are data bandwidth and the L1 trigger latency:
• not exceed 10% of total L1 trigger bandwidth (estimate).
• Total L1 front-end latency of 12.5 µsec.
In order to keep the latency and further reduce bandwidth, the inclusion of a fast ROI trigger is a key point.

Verilog modeling of FEI4-b for testing the Fast ROI Level-1 pixel based track Trigger

The goal is to model a readout architecture which includes a second fast Level-1 trigger in the FEI4b [2] digital design. The inclusion of such a trigger should provide in the overall architecture a fast extraction of the relevant hit-cluster in the ROI, to be sent to the L1 trigger correlator. The main issue is to study how it impacts on the data transmission and upper stage design. The Verilog model of the simplified FEI4b architecture is based on:
• 336x80 pixels organized in regions by 4;
• Exact column token page logic;
• Simplified End-of-Column logic;
• Digital implementation of the Fast ROI L1 trigger based on 2.5 µsec latency;

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References:

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