Title: “Tuning System for Xilinx MGT Transceivers”
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High speed Serializer-Deserializer interfaces (SerDes) are a recurrent solution for communications in FPGAs, representing an alternative to parallel buses running at a lower rate. Although these interfaces save limited input/output resources, high rate communication demands special signal conditioning to overcome noise and interference.

Modern FPGAs such as Xilinx Virtex 7 offer SerDes modules called Multi-Giga Transceivers (MGTs). They incorporate the hardware infrastructure required for high speed communication, allowing the user to calibrate the signal conditioning parameters for optimal results in different applications using the Xilinx Vivado Design Suite.

The calibration for MGTs communicating between different FPGAs should be performed manually, which is a painful process given the numerous parameter combinations. In order to overcome this difficulty, we have developed a tuning system in Python, aiming to automate the tuning process of Xilinx MGT transceivers.