IPbus applied to the CMS Level1 Tracking Trigger Upgrade

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CMS L1 Tracking Trigger Proposal

Planned to start in 2025, the High Luminosity operation of the LHC will enhance the search of new elementary particles and the study of the Higgs boson. The LHC Phase II upgrade will increase the amount of proton-proton collisions inside the Compact Muon Solenoid (CMS), and consequently, a suitable Level 1 Tracking Trigger (L1TT) hardware is needed to process and filter the large amount of data produced by the detector.

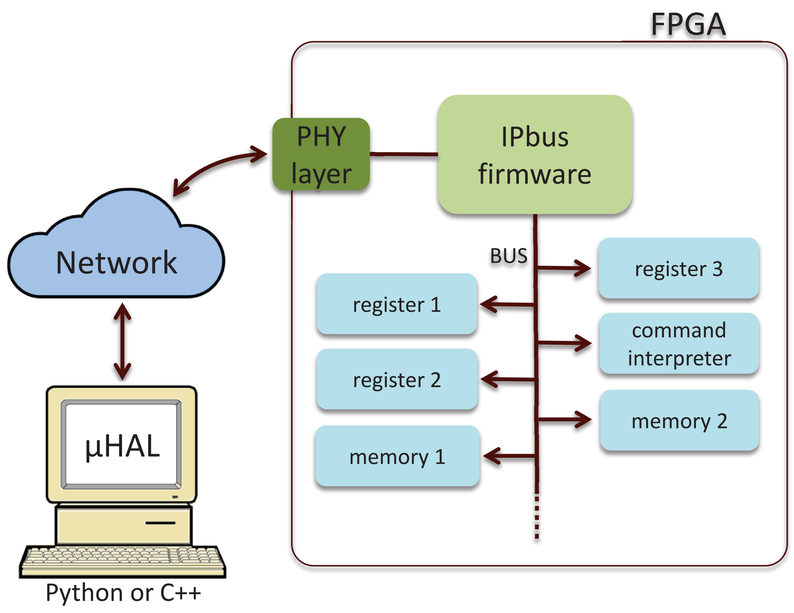
The Fermilab proposal to the L1TT is based on Associative Memories integrated by FPGAs (AM+FPGA) and employs the Pulsar IIb FPGA board as base hardware. One of the Sao Paulo Research and Analysis Center (SPRACE) tasks is to enable the use of IPbus to access and control hardware programmed inside FPGAs in this project, mainly for the testing and prototyping stages, as well as for the demonstration of the system.

The IPbus suite

The IPbus protocol[1] allows any hardware implemented in FPGA to be accessed by a PC over UDP/IP. IPbus suite covers both sides of communication: firmware and PC.

IPbus firmware - It is a VHDL code that offers a generic interface bus flexible enough to be used according to the project requirements. This code implements a UDP server and translates its messages, providing data transactions to user-defined modules attached to that bus.

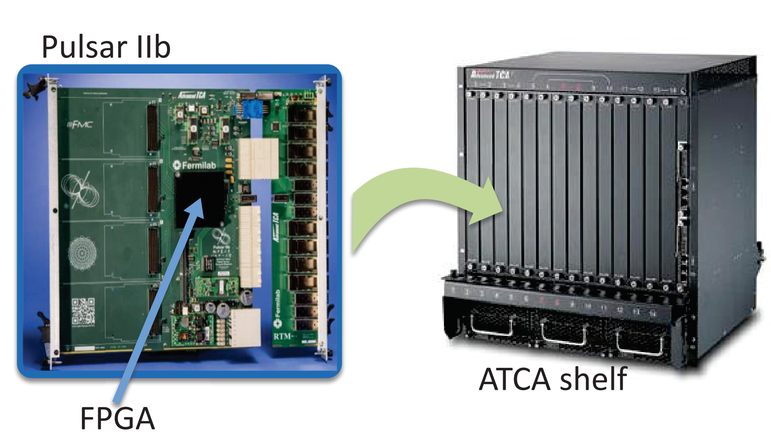
µHAL library - The Hardware Access Library provides a Python/C++ API to control the interface bus implemented in the FPGA. It allows the programmer to perform read and write operations in the hardware through a PC via standard network links.



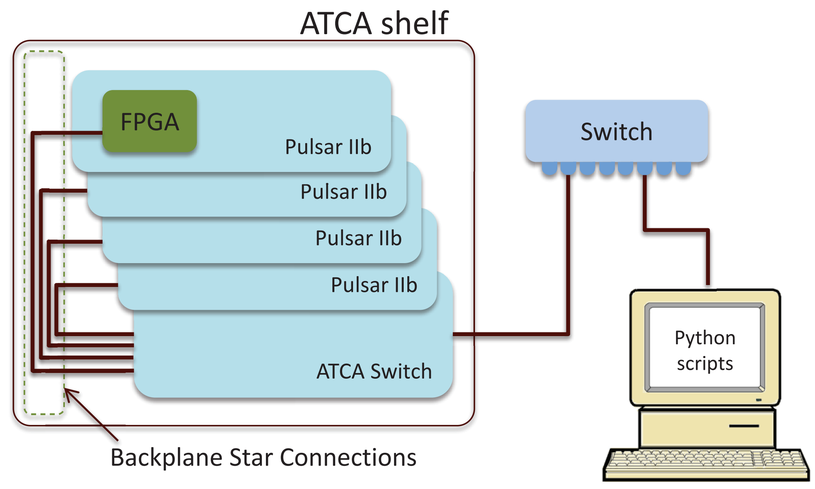
This interface bus reads and writes 32-bit words, and uses a 32-bit addresses to multiplex data origin or destination. Therefore the mapping covers from simple registers to block memories. In addition to that, combinations of address and data could even be mapped as commands to the user-defined modules.

IPbus applied to Pulsar II b

Pulsar IIb[2] is a general purpose FPGA-base carrier board for ATCA platforms. It was developed by Fermilab using a Virtex7 Xilinx FPGA equipped with 80 high speed-transceivers, each of them capable to operate above 10Gb/s in full-duplex mode.

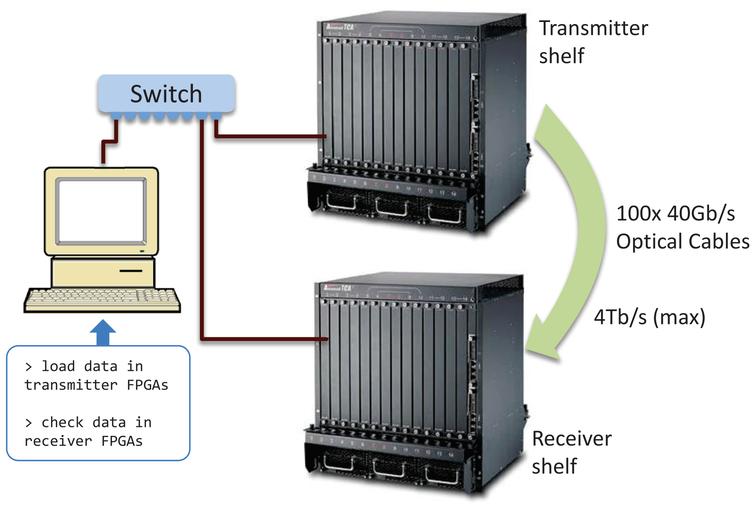


The L1TT Fermilab proposal and its development tests are totally based on Pulsar IIb, using a large number of them. In addition, the final system will stay in difficult access sites. IPbus solves both issues since it uses regular network. The access to each Pulsar IIb board is done through the ATCA Switch in star connection.



IPbus Application

Due to the large amount of data that will be sent by CMS detector to the L1TT under development, several Pulsar IIb boards should receive data through their optical links. To test this scheme, two shelves filled with 10 Pulsar IIb each are used to compose a transmitter/receiver pair. IPbus is used to control the test.



Acknowledgements

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References

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