SciFi Detector Evaluation

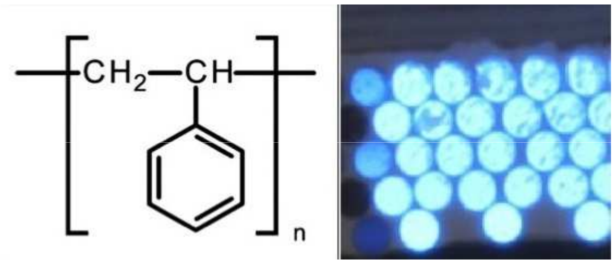
Research and experiment assembly for the SciFi & SiPM technology

André Massafferri, Christian Vincenzi, Valdir Salustino
Brazilian Center for Research in Physics – CBPF – christianvn@cbpf.br

Abstract: The LHCb SciFi upgrade relies on a new technology for particle detection, which consists from the attachment of small diameter scintillating fibers with SiPM photodetectors. Apart from the LHCb, this technology is of interest for other particle detection experiments and applications like medical imaging. The goal of the CBPF project is the development and characterization of a small X/Y 256 channel detector with a sensible area of 3x3 cm² made of thin scintillating fibers and SiPM.

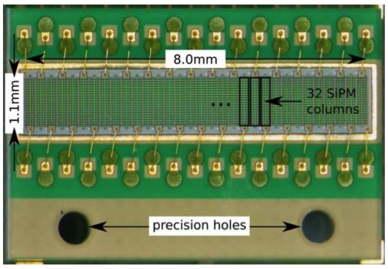
Scintillating Fibers & SiPM

Polystyrene Fibers can now be manufactured with a diameter of 250 µm. The LHCb succeeded in fitting the fibers together and laying them straight and aligned, providing an estimated resolution of 70 µm. In addition, they were able to provide good quality control of the diameter, otherwise the fibers would mechanically misfit creating problems with signal resolution.



Picture 1: Left - Polystyrene molecule; Right - 250um fibers.

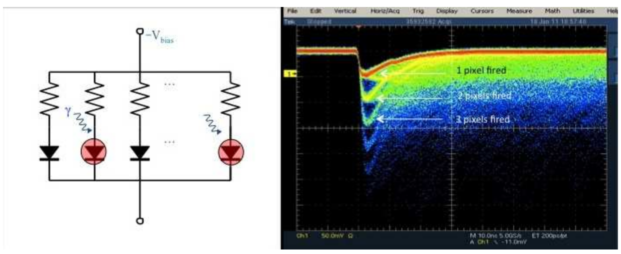
The output light from the fibers are readout by the SiPM. The SiPM are solid-state devices composed by an avalanche photodiode(APD) array operating in Geiger-Mode with high voltage on common silicon substrate. The SiPM temperature must be low and stable in order to reduce noise and gain variation.



Picture 2: SiPM Photodetector

Picture 3: SciFI Matrix

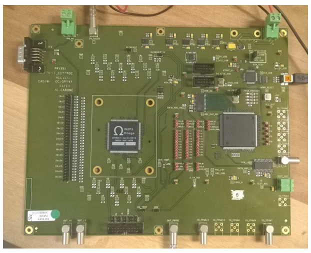
When a pixel is hit, it delivers an output charge which is summed with other channel pixels. By these properties, it works as photocounter. The pixel sensitivity is sufficient to detect a single photon. This project uses two SiPMs, 128 channels each. Each channel has 96 pixels. The resolution of 70 um is achieved by analyzing adjacent channel levels, allowing the determination of baricenter of the hit cluster.



Picture 4: SiPM Pixels and Pixel firing on scope

CITIROC Evaluation Board

The FEE will use a CITIROC ASIC designed by IN2P3 which features individual channel charge measurement and triggering. Meanwhile we are using the 32 channel Evaluation Board housing one ASIC and an FPGA, controled by labview software.

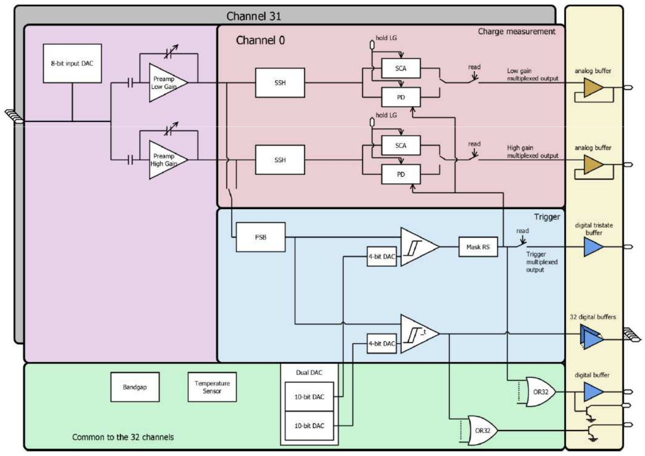


Picture 5: CITIROC Evaluation Board

The FPGA configures the CITIROC chip by Slow Control on a train of 1144 bits. It also receives information from the ASIC, sends pulse commands and reference frequencies. The LabView user interface communicates with the FPGA allowing easy ASIC configuration, ADC measure and periferical tests.

CITIROC Signal Processing & Control

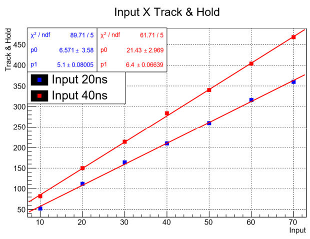
The analogue core features 32 channels embedding an input DAC for SiPM high voltage adjustment on 4.5V to tune the sensor gain channel by channel. Two voltage sensitive preamplifiers allow the requested dynamic range from 160 fC to 320 pC and are followed by a trigger line made of a fast shaper and two discriminators. The charge measurement is provided by two variable slow shapers and two Track and Hold blocks. (CITIROC Datasheet. Retrieved from omega.in2p3.fr)



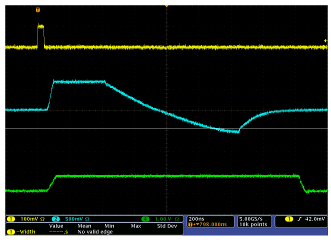
Picture 6: Signal processing Block Diagram - Per Channel

Tests on Evaluation Board

The lab is yet to connect the SiPM on the evaluation board, for it's special connector is incompatible with the evaluation board pin header. Therefore, arbitrary waveforms were injected on the evaluation board for proper understanding of it. The test input used was: Square wave; 20ns or 40ns; 50mV to 100mV; 100kHz. The plotted results include Slow Shaper Output and charge measurement by Track & Hold. The board has two 12-bit ADCs on the charge output, whose values could be evaluated on LabView regarding signal/noise ratio.



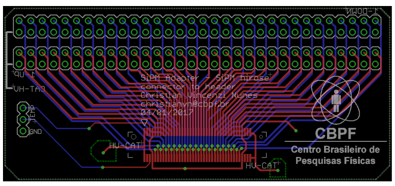
Picture 7: T&H values



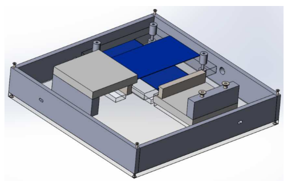
Picture 8: High Gain Shaper and T&H

Next Steps

- Adapter: SiPM to Evaluation Board
- Case for mechanical protection, Peltier cooling and light injection.
- Acquire strontium source for tests.
- Project and build 256 channel FEE. Two boards, each one with 1 FPGA controlling 4 CITIROCs, with a newly programmed firmware.



Picture 9: SiPM Adapter



Picture 10: Detector Case

CNPq Conselho Nacional de Desenvolvimento Científico e Tecnológico

LHCb