

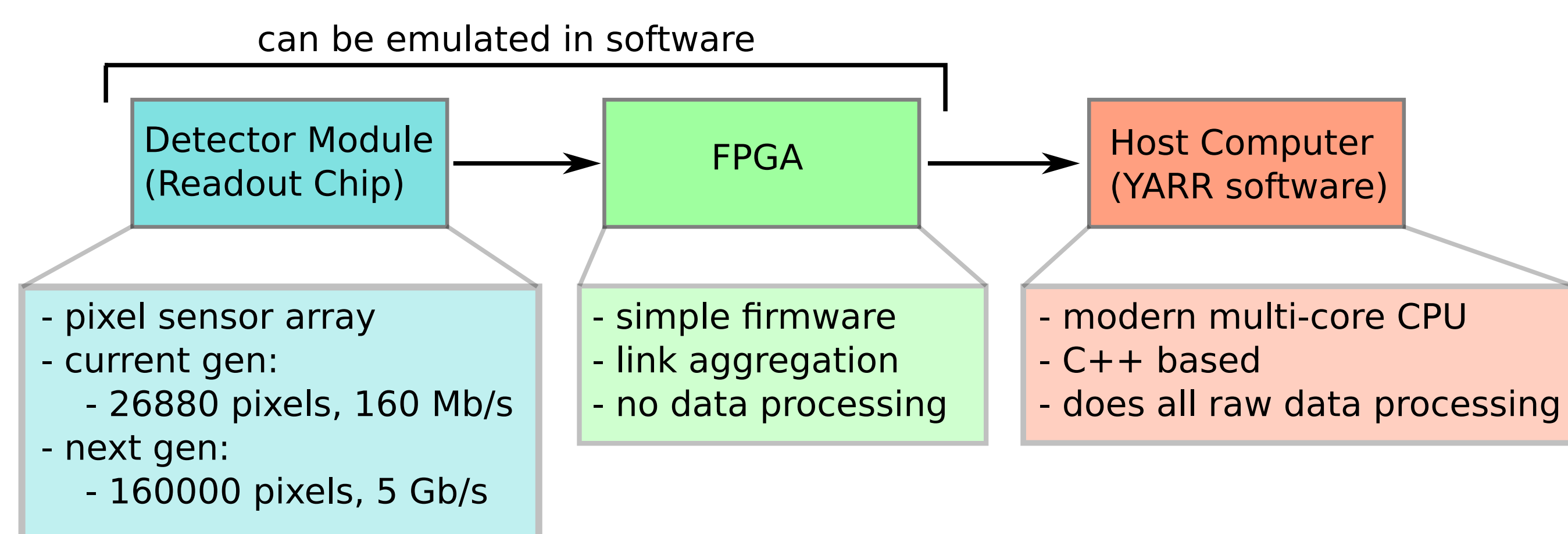
# Software Emulators for the YARR DAQ System

## Introduction

The Yet Another Rapid Readout (YARR) software aims to provide a simple, modular, and high performance data acquisition (DAQ) system for next generation pixel readout chips to be deployed in the High Luminosity LHC (HL-LHC) ATLAS Inner Tracker Detector (ITk). YARR can interface with current generation pixel readout chips, such as FE-I4, and is being upgraded to interface with the RD53A demonstrator chip for ITk. It can also interface with software emulators of readout chips, greatly simplifying the DAQ development and allowing development of DAQ for future readout chips, such as RD53A. These emulators also allow the implementation of continuous integration for YARR, improving the maintainability and quality of the software.

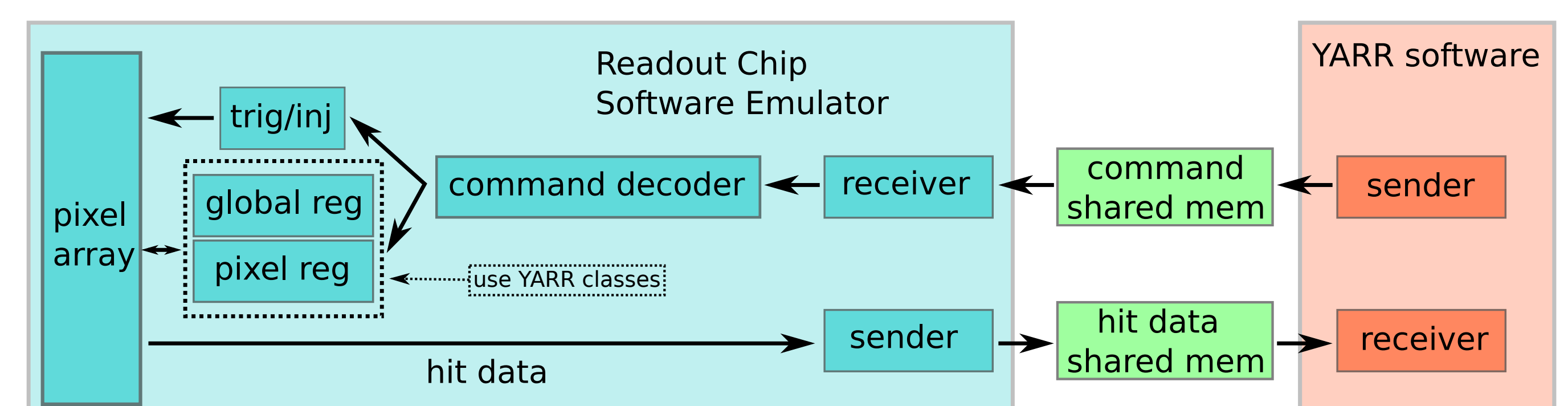
## YARR In a Nutshell

- YARR software interfaces with readout chips via a PCIe FPGA board
- the FPGA firmware is simple and multiplexes links
- core design philosophy is to delegate all data processing to the host
- a recent major addition to YARR is the ability to interface with emulators



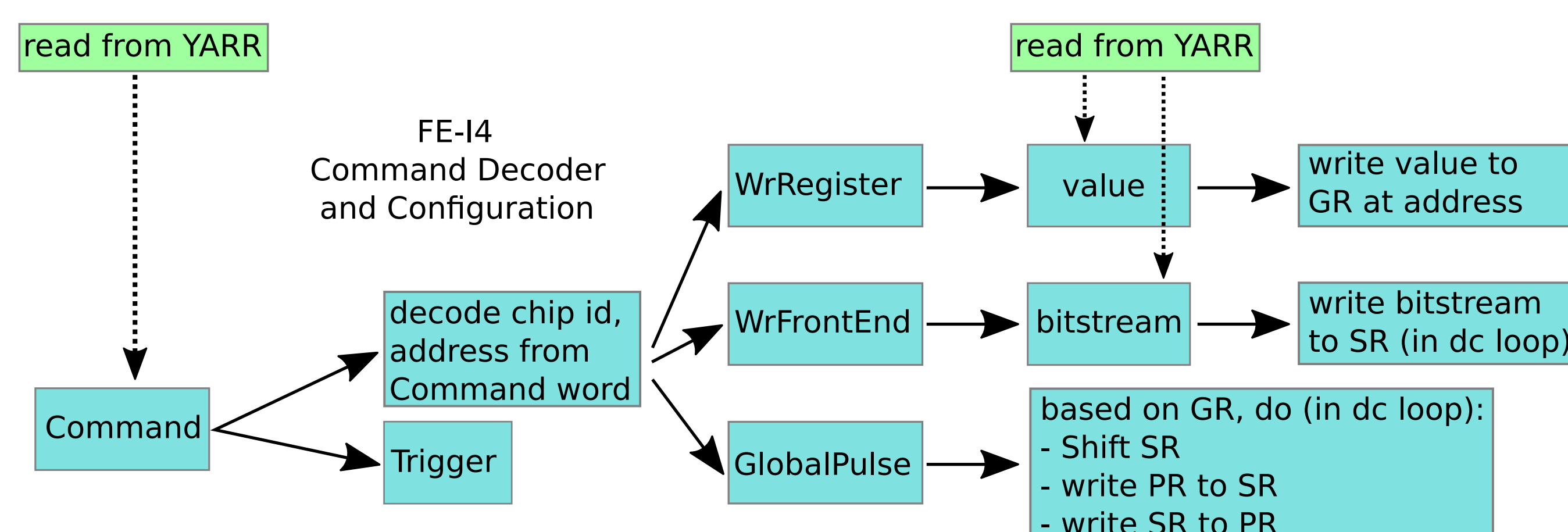
## Emulator Design

- emulator receives commands from YARR and decodes them
- non-trigger commands configure Global/Pixel Registers (GR, PR)
- trigger commands cause the emulator to loop over a virtual pixel array
- emulator models pixel hits and sends hit data back to YARR
- 2 emulators currently: FE-I4 (done) and RD53A (in development)



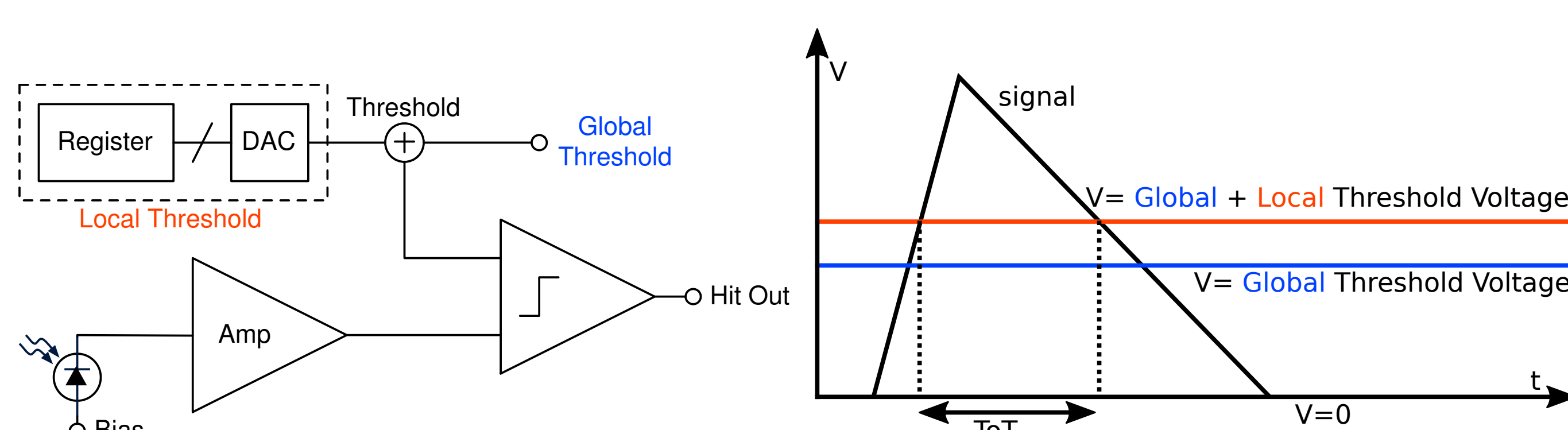
## FE-I4 Register Configuration

- Global Registers contain chip-level settings, e.g. global threshold voltage
- Pixel Registers contain pixel-level settings, e.g. local threshold voltage
- to configure registers, must send specific commands to the chip/emulator



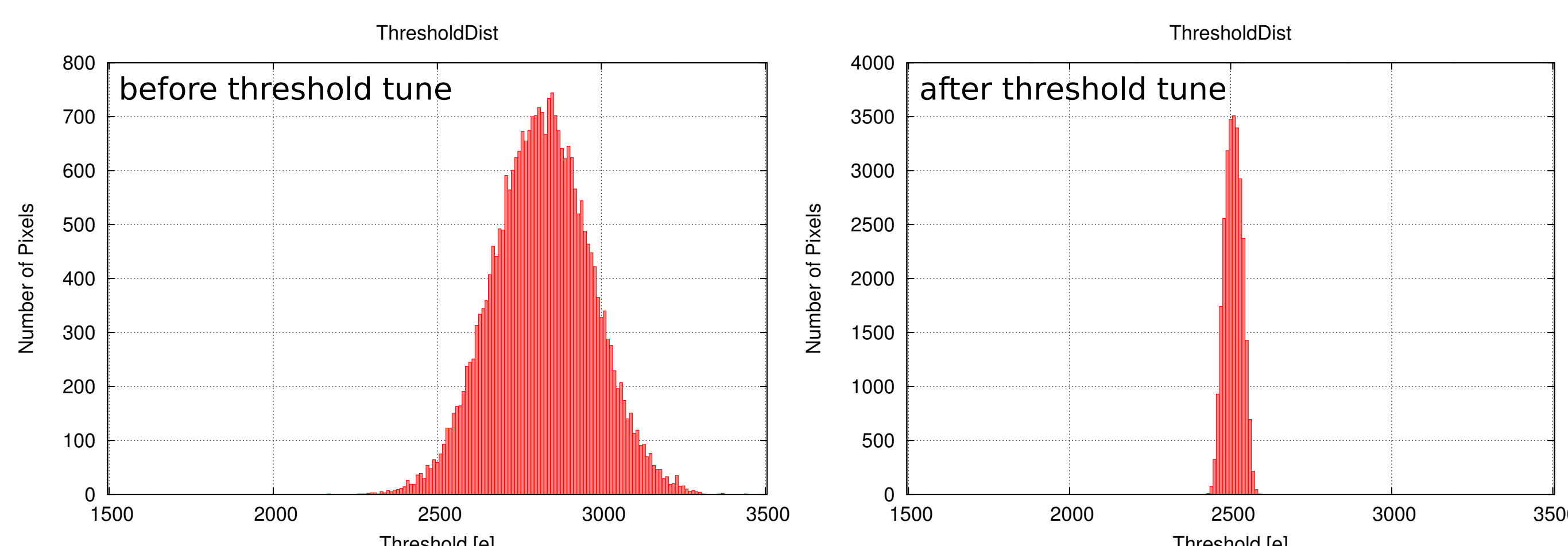
## FE-I4 Hit Modelling

- hits are registered if signal is above a threshold voltage
- the threshold voltage is determined by global and local threshold values
- emulator models threshold behavior/noise with per-pixel Gaussian smearing
- the Time over Threshold (ToT) is the main hit information calculated



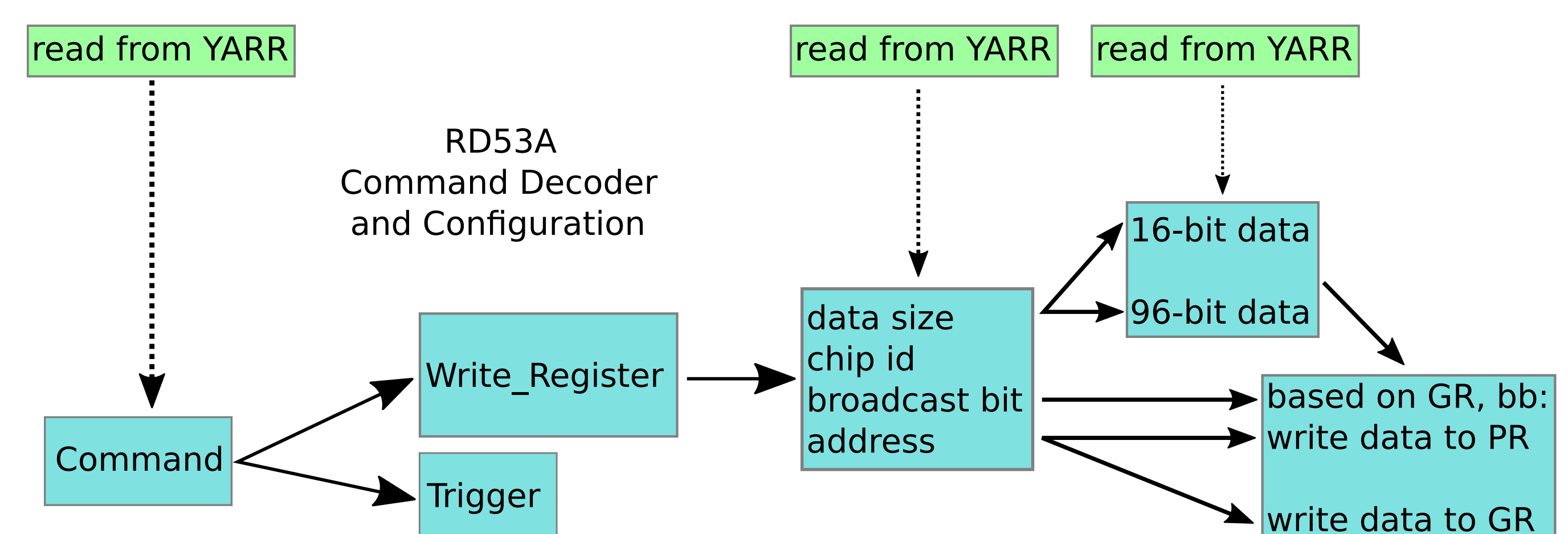
## FE-I4 Scans and Calibrations

- FE-I4 emulator behaves like real FE-I4 chips
- can run all scans and calibrations, e.g. threshold calibration shown below

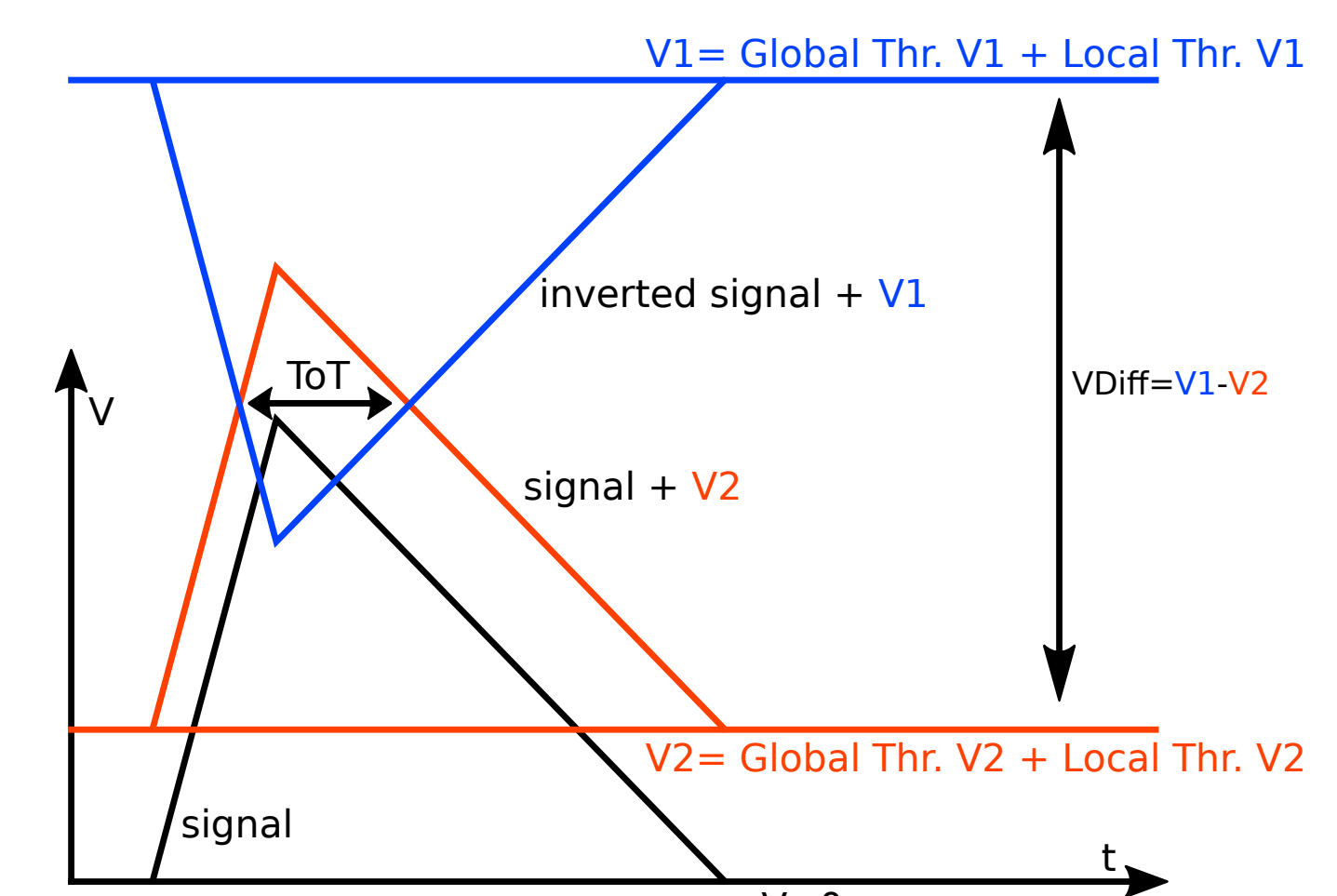


## RD53A Software Emulator

- RD53A software emulator under development
- emulator development in parallel with YARR RD53A DAQ development
- new command decoder, chip configuration, and hit modelling

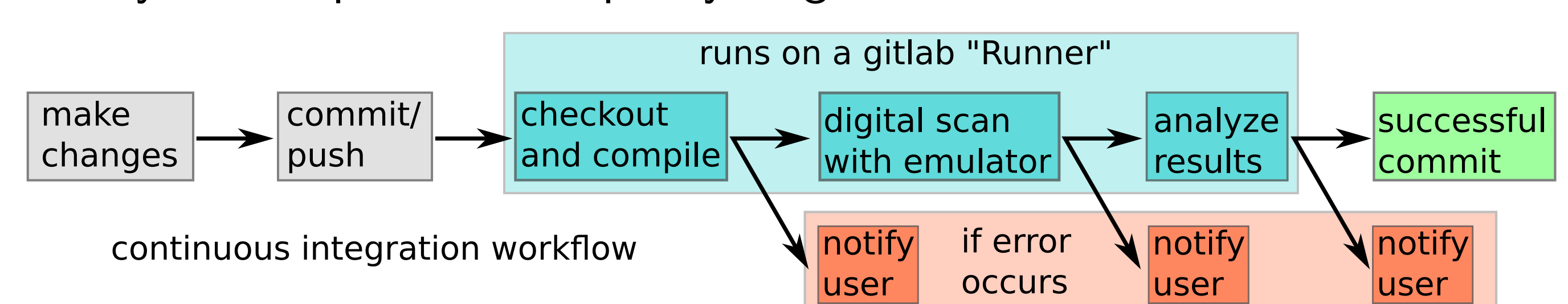


- RD53A contains 3 types of analog front end, requiring 3 different hit models to be implemented
- hit modelling for 1 of the analog front end types shown to the right
- here, ToT is calculated by comparing an offset signal with an inverted and offset signal



## Continuous Integration

- software emulators allow for easy continuous integration implementation
- after every commit, a server called a "Runner" checks out the YARR repo
- Runner compiles YARR, runs a digital scan with an emulator, checks results
- if the Runner fails, user is notified that their code broke something
- this system helps maintain quality, bug-free code



## References and Further Info

- refs: [cern.ch/go/D8gF](https://cern.ch/go/D8gF) [cern.ch/go/D6TW](https://cern.ch/go/D6TW) [cern.ch/go/F9BL](https://cern.ch/go/F9BL)
- for YARR software on GitLab, scan the QR code to the right:
- my email: [alokin@uw.edu](mailto:alokin@uw.edu)

