Contribution ID: **144** Type: **Poster**

Upgrade of the YARR DAQ system for the ATLAS Phase-II Pixel detector readout chip

Tuesday 22 August 2017 16:25 (20 minutes)

The Yet Another Rapid Readout (YARR) system is a DAQ system designed for the readout of the current generation ATLAS Pixel FE-I4 chip, which has a readout bandwidth of 160 Mb/s, and the latest readout chip currently under design by the RD53 collaboration which has a much higher bandwidth up to 5 Gb/s and is part of the development of new Pixel detector technology to be implemented in High-Luminosity Large Hadron Collider experiments.
YARR utilises a commercial-off-the-shelf PCIe FPGA card as a reconfigurable I/O interface, which acts as a simple gateway to pipe all data from Pixel modules via the high speed PCIe connection into the host system' s memory.
All data processing is done on a software level in the host CPU(s), utilising a data-driven, multi-threaded, parallel processing paradigm.
This processing is designed to support a scalable, modular distribution to multiple CPUs with an asynchronous, message-oriented system control.
It is also designed to allow for a flexible configuration, enabling the system to adapt to various hardware boards and use-case scenarios.
As such, the software is designed to cover a large range of operational environments, from prototyping in the laboratory, to full scale implementation in the experiment -
this is one of the core design goals, as it conserves manpower and builds a larger user-base compared to more specialised systems.
YARR is also able to interface directly with software emulators of front-end chips which frees the software development from the necessity of readout hardware and is
useful for unit and coverage tests.
The overall concept and data flow of YARR will be outlined, as well as a demonstration of the system's DAQ and calibration capabilities and performance results of the PCIe transfer rate.

Primary author: WHALLON, Nikola Lazar (University of Washington (US))

Co-authors: HEIM, Timon (Lawrence Berkeley National Lab. (US)); OIDE, Hideyuki (INFN-Genova); POTAMIANOS, Karolos (Lawrence Berkeley National Lab. (US))

Presenter: WHALLON, Nikola Lazar (University of Washington (US))

Session Classification: Poster Session

Track Classification: Track 1: Computing Technology for Physics Research