LHC Power Converters And their SEE design

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Acknowledgments:

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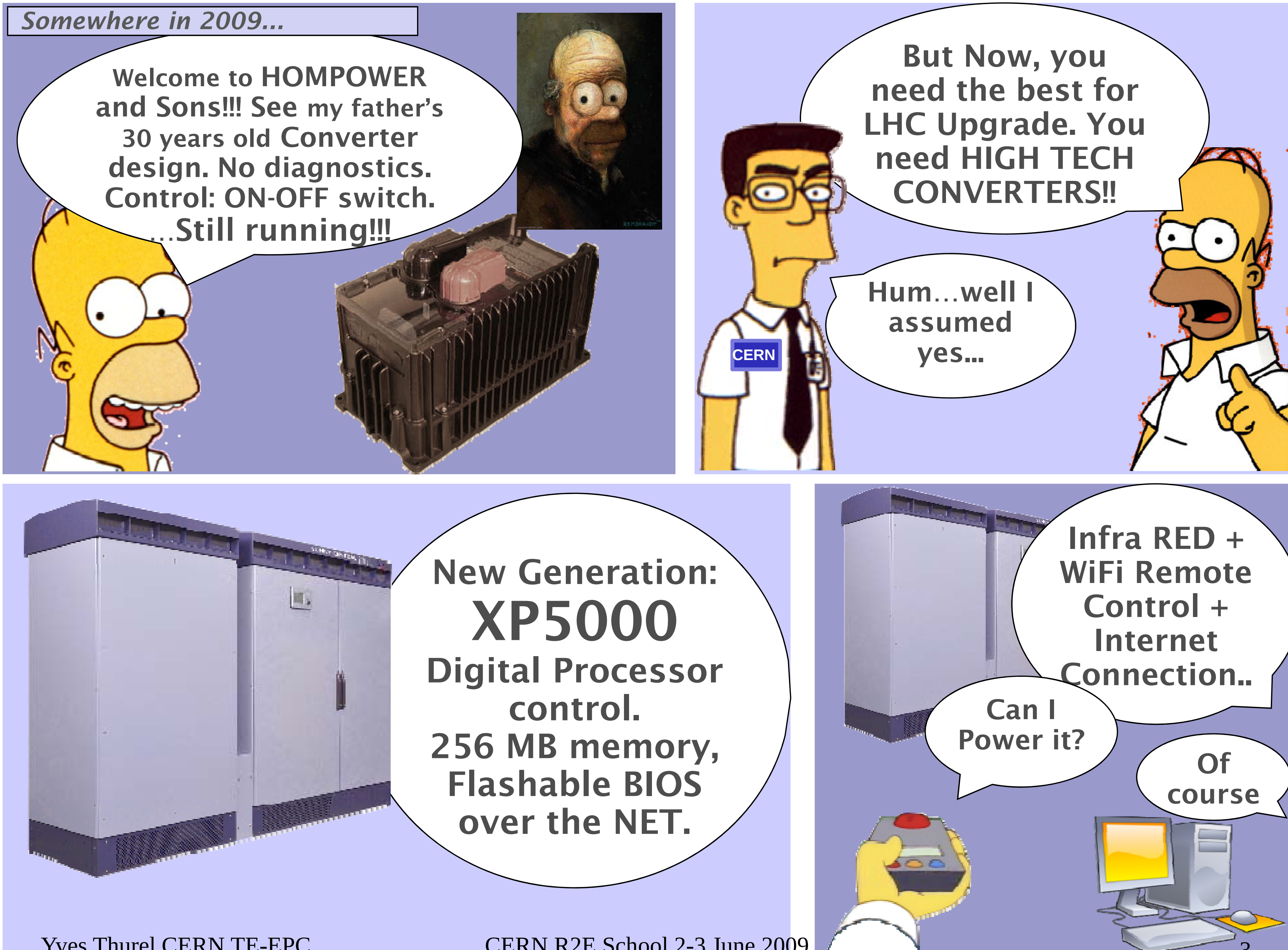
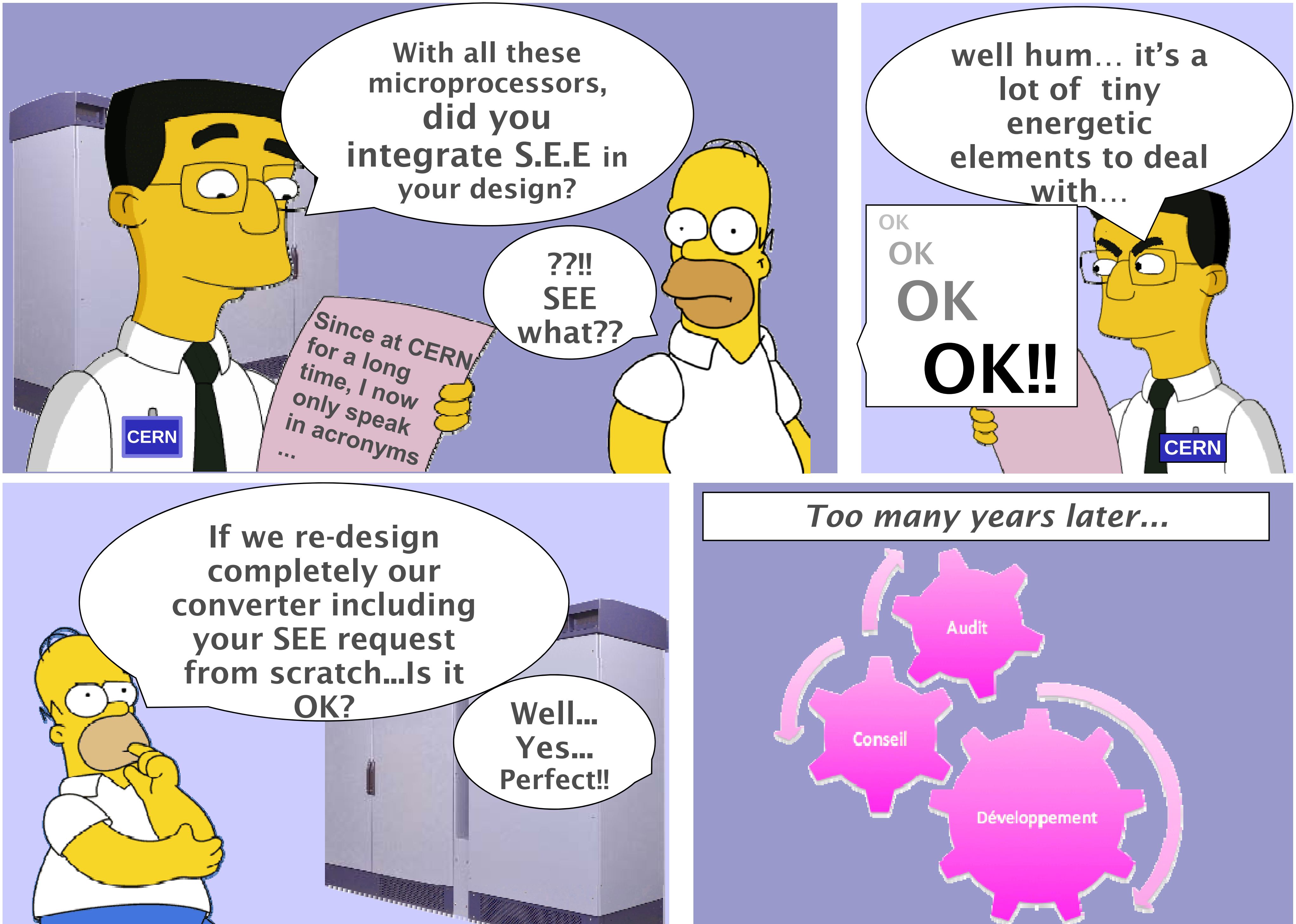
• Frederick Bordry .... [CERN]
Slides from RADECS 2007 presentation :
"The LHC Power Converters and their radiation tolerance"

First, what to expect from a power converter engineer dealing with Single Event Effects design…

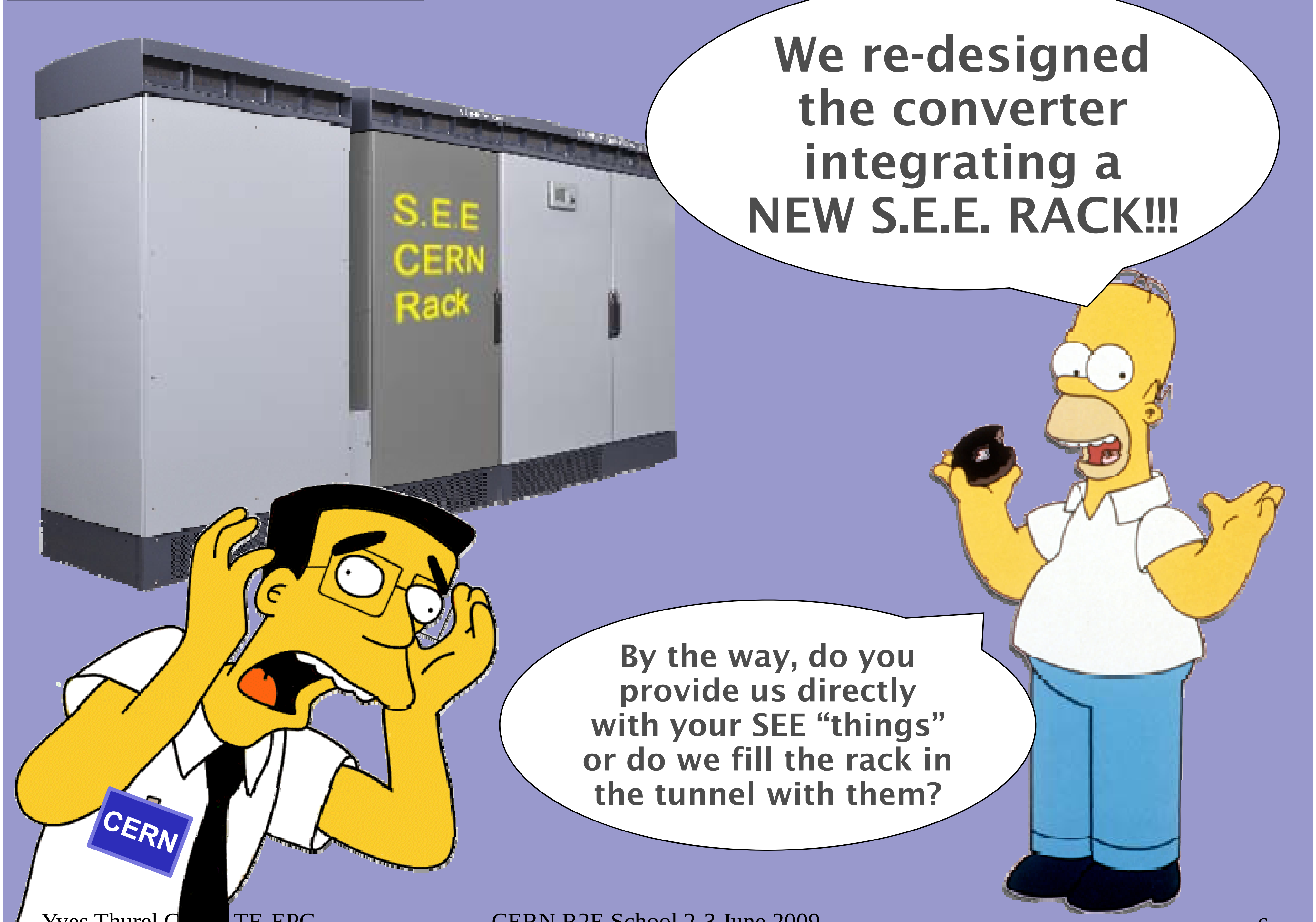
Let's have a look in detail and imagine a CERN Engineer visiting a Power Converter Company for a S.E.E compliant power converter for the LHC Upgrade Program...


Somewhere in 2009…
Welcome to HOMPOWER and Sons!!! See my father's 30 years old Converter design. No diagnostics. Control: ON-OFF switch. …Still running!!!
But Now, you need the best for LHC Upgrade. You need HIGH TECH CONVERTERS!!
CERN
Hum…well I assumed yes…
New Generation: XP5000 Digital Processor control. 256 MB memory, Flashable BIOS over the NET.
Infra RED + WiFi Remote Control + Internet Connection..
Can I Power it?
Of course


It doesn't work!!!
Well?
D'OH!!
OOPS!! Remote batteries dead ?
It doesn't work better through the network...
Well???
CERN
D'OH!
OOPS... Its surely a firewall problem


With all these microprocessors, did you integrate S.E.E in your design?
Since at CERN for a long time, I now only speak in acronyms …
CERN
??!! SEE what??
well hum… it's a lot of tiny energetic elements to deal with…
OK
OK
OK
OK!!
CERN
If we re-design completely our converter including your SEE request from scratch...Is it OK?
Well... Yes... Perfect!!
Too many years later...
Audit
Conseil
Développement

Same place in 2012...



What was SO wrong in the process???

Did you integrate SEE in your design?

Too much simplified description of the problem for a SEE newbie

Did you integrate in your design the high volume of tiny elements we will send to the power converters?

I have to find a place in the power converter to store all the small things they have a lot at CERN

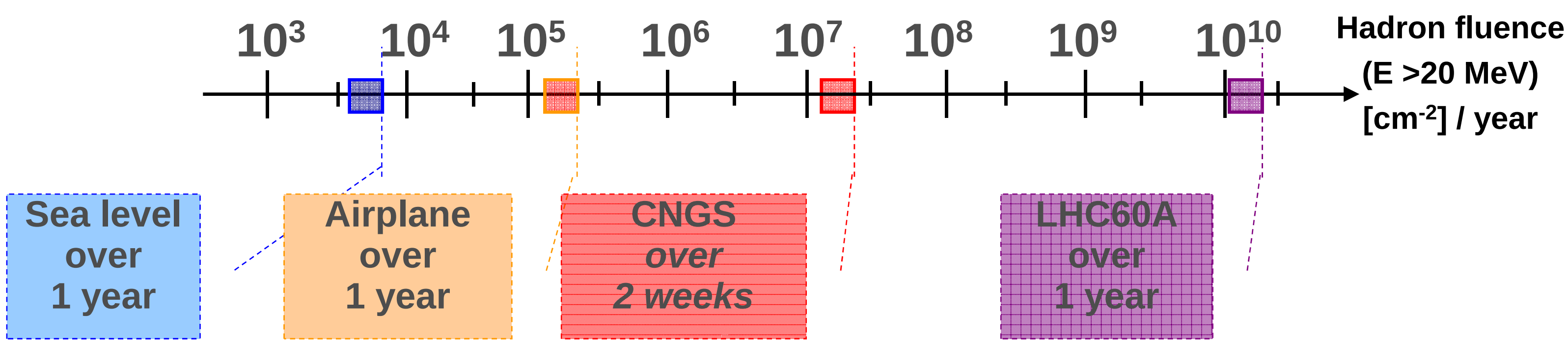
Don't simplify too much the S.E.E problematic. It is not simple and you have to be prepared to invest a lot of time to LEARN, TEACH what IT IS to people not used to. A good comprehension of the mechanism is the crucial 1st step.

Moral and talk construction

- **Power Converters are nowadays integrating a lot of « high performance digital » components: CPU, RAM…**
- **Power Converter Specialists are not familiar at all with S.E.E concepts: WHAT IT IS!!, design key rules**
- **Old Fashioned Power Converters were certainly more robust with respect to S.E.E problems**
- **A « S.E.E. » design is long, costly and not always possible (Test infrastructure)**
- **Even with good intentions, disaster is never far away for a « rad-tolerant » design, especially when using COTS components**

Power Converter Design Regarding Single Event Effect Issues*

**** See context Below***



How does a converter look like

- From some kg up to thousands of kg
- Electrical connections
- A cooling system (water / air)
- Digital Controller with a Control Field bus

LHC13kA-180V
2-Quadrant

8 Units
CERN Design

LHC120A-10V
4-Quadrant

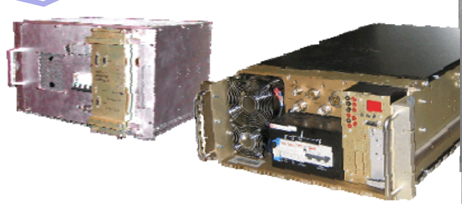
300 Units
CERN Design

LHC4..6kA-08V
1-Quadrant

200 Units
Kempower

LHC60A-08V
4-Quadrant

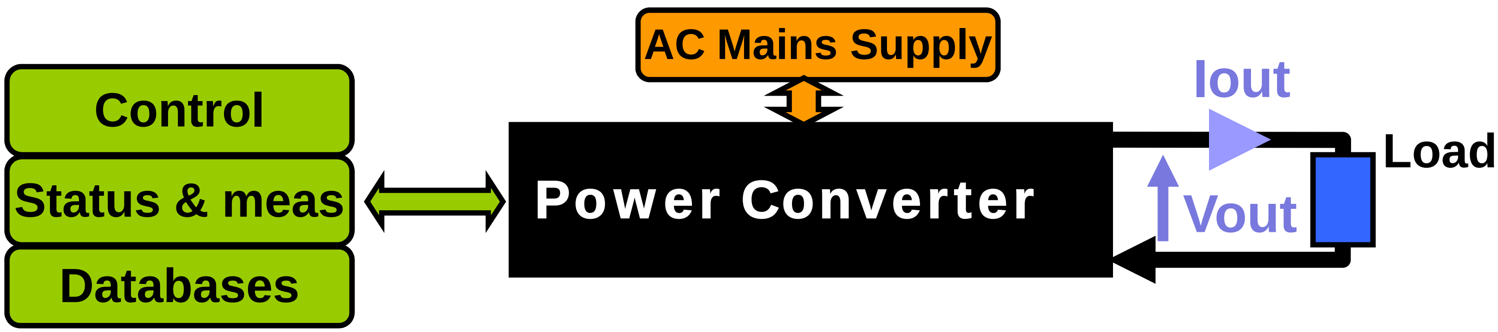
730 Units
CERN Design



The basics

A Modern Converter is a “black box” which:

1. transform AC Mains Power into adequate conditioned power to the load
2. Is controllable over a field bus with advanced diagnostic features
3. Import and export data from and to the controls applications and database



The Good Question in the case of a radiation-hard converter

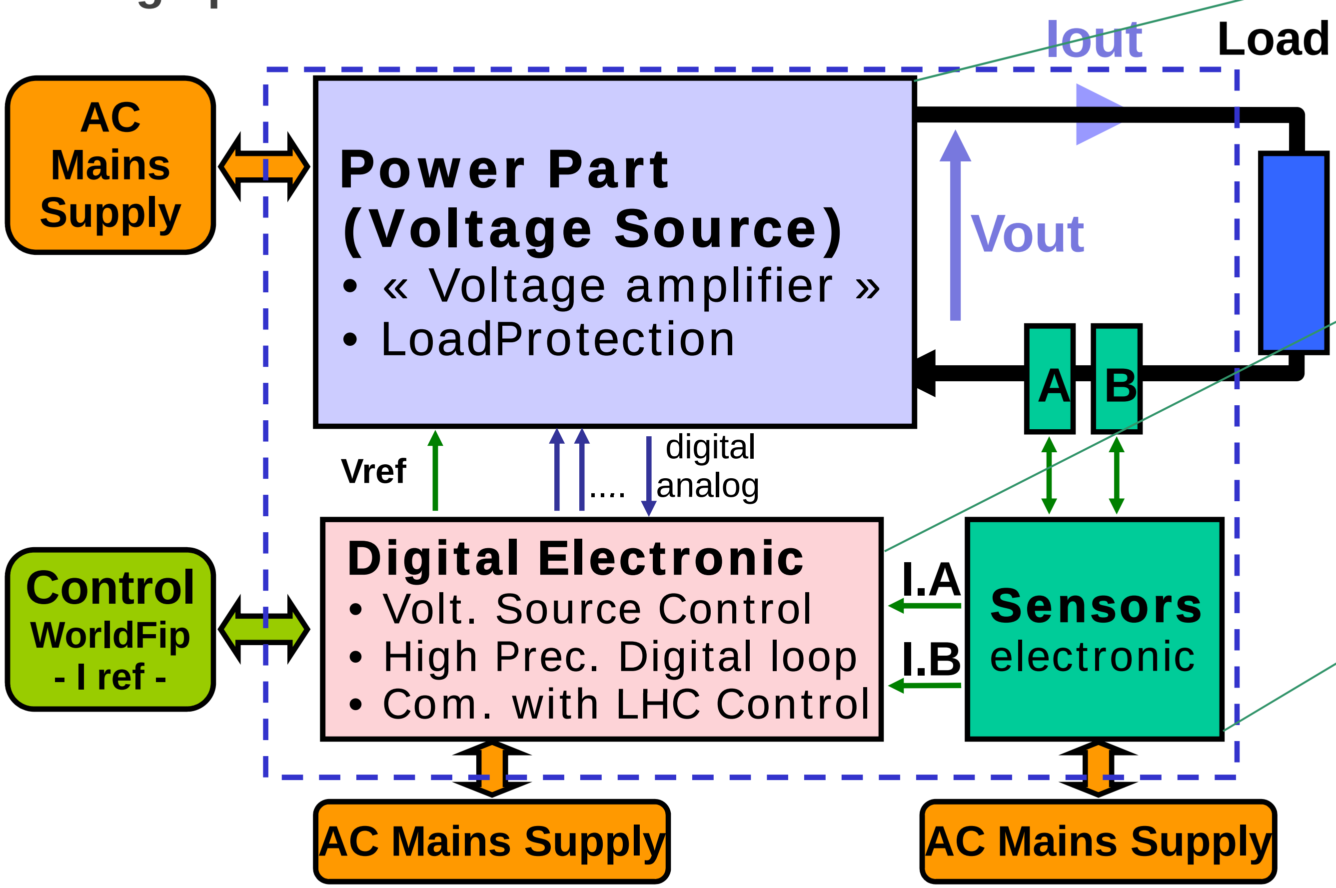
How to manage the following required data processing of the converter

- Remote control of the power converter (using Field Bus)
- Accessing external database
  - Load Parameters for tuning Digital Control loop (database import)
  - Load operational Limits (current voltage)
  - Calibration parameters
- Providing modern Post Mortem Analyze (database export)
- On line status and analog measurements

An adequate Answer (LHC Answer)

Architecture of the LHC power converter was divided in 3 parts:

1. **Power conversion unit**
2. **Digital Control unit**
3. **High precision measurement unit**



This unit does not require any trimming depending on load nature. No access to database required

*This unit **concentrates** all data processing, database request, import & export data, post mortem…*

This unit can be pure analog sensor

Entering the different parts

Power Part (Voltage Source)
- « Volt. amplifier »
- Load Protection

Component types
- ~~CPU~~, CPLD, ~~DSP~~, ~~RAM~~
- Power Transistors & Drivers
- Optocouplers
- DC-DC, AC-DC
- Traditional other circuits

Radiation Impact
- Not highly sensitive components like CPU or RAM
- But High Power = danger / destruc.

Digital Electronic
- Volt. Source Control
- High Prec. Dig. loop
- Communication

Component types
- CPU, CPLD, DSP, RAM, FPGA
- ~~Power Transistors & Drivers~~
- Optocouplers
- DC-DC, AC-DC
- Traditional other circuits

Radiation Impact
- Great care on this Unit since high concentration of sensitive components

Sensors electronic

A

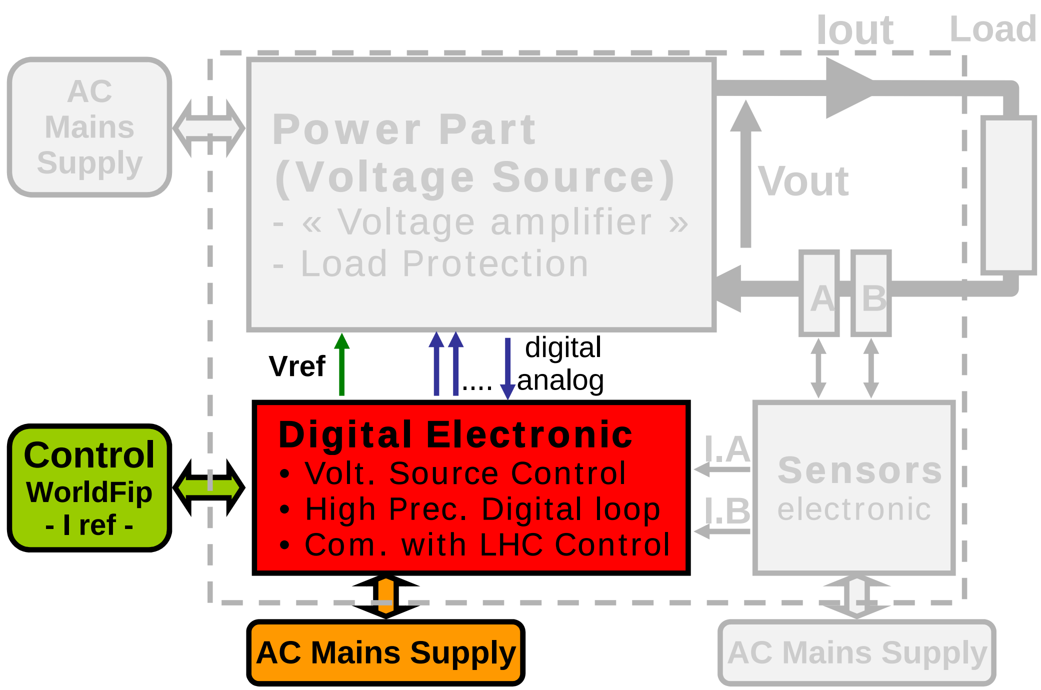
B

Component types
- ~~CPU, CPLD, DSP, RAM~~
- ~~Power Transistors & Drivers~~
- Optocouplers
- ~~DC-DC~~, AC-DC
- Traditional other circuits

Radiation Impact
- Standard analog components. No high potential risk

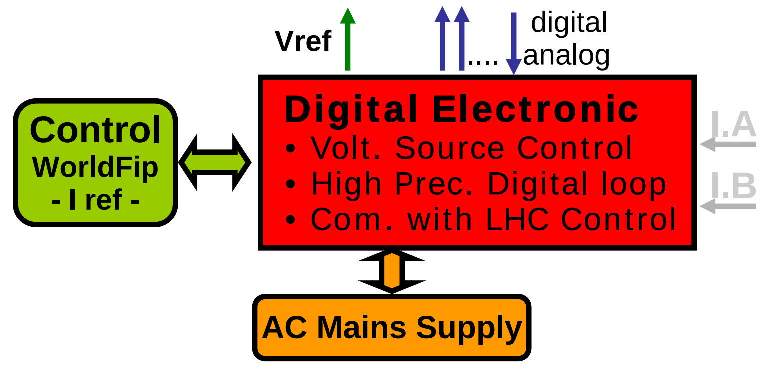
Not treated here since low S.E.E impact

The digital controller Design



How does a Digital Controller look like

- Digital controller
- Its PSUs
- Its chassis collecting all signals exchanged with power converter and field bus

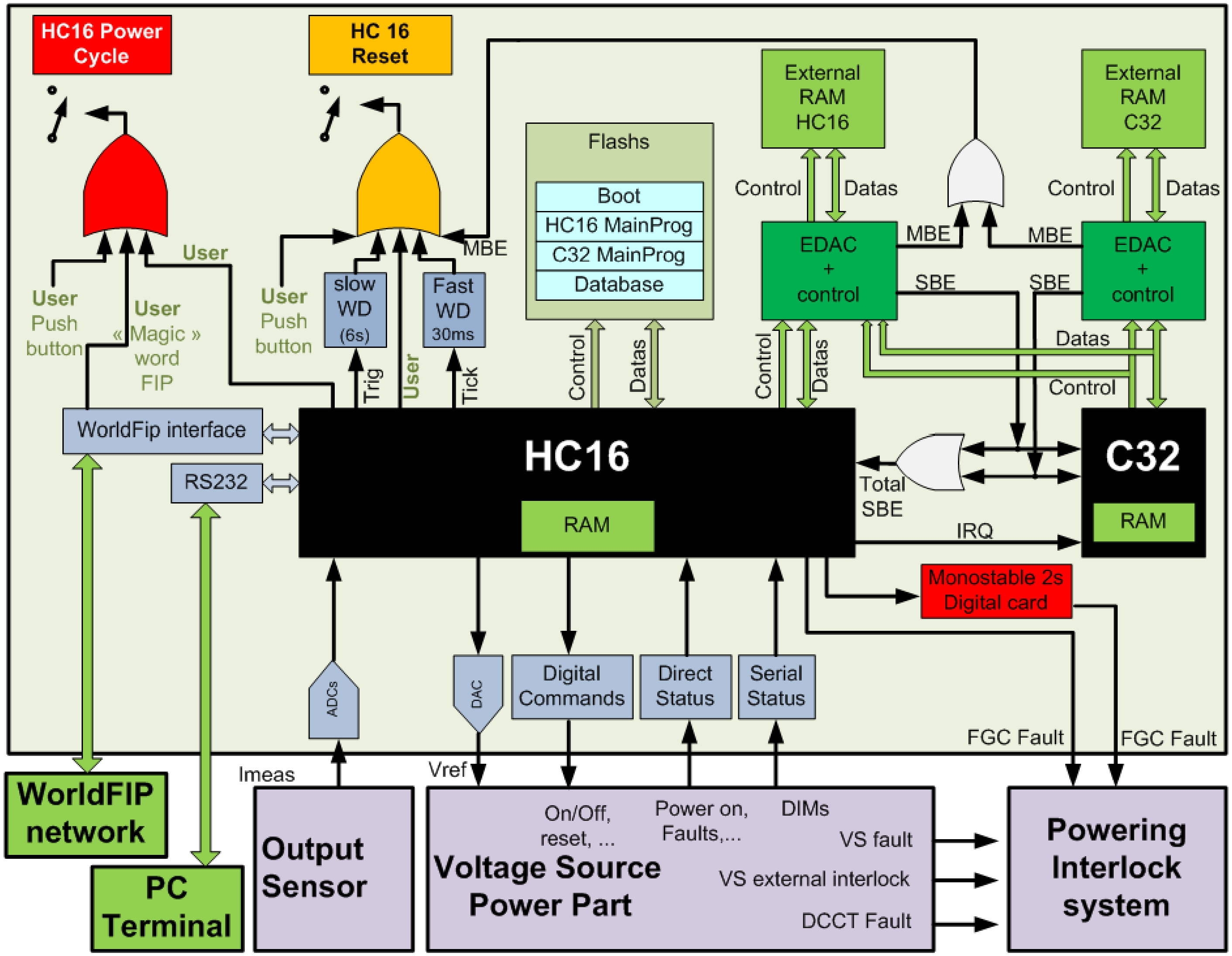


Electronic Chassis

PSUs AC-DC and / or DC-DC)

High Prec. Electronics cards

Overview of hardware internal components layout



Main Processor: HC16
- internal RAM not used

DSP Co-Processor C32
- internal RAM not used

Memories
- SEE Optimized
- Adequate Technology compared to use
- EDAC Corrections

Power Cycle
- advanced feature:
  - Push button
  - User command
  - Magic (long) packet on WorldFip

Reset
- advanced feature
  - Slow Watchdog
  - Fast Watchdog
  - User command

Microcontroller MCU (MC68HC16)

Function:	**Communication, command parsing, logging**
SEE sensitivity	**Internal Memory sensitive** **registers sensitive**
Market & Choices	**COTS possible combined with testing** **Fabrication technology** **Core voltage dependence? (we used 5V devices)**
SEE Improvement	**Use only component radiation tested & validated** **Do not use internal memory (if no EDAC)** **Only use registers (low cross section & less sensitive)** **Refresh registers all the time** **Program stored in Flash Memory** **Dynamic Data stored in EDAC + SRAM** **Slow & Fast Watchdog for reset** **Power Cycle feature** **Software Auto-check (code confidence & integrity test)**

Digital Control Unit: Components – criteria 2/4

DSP (TMS320C32)

Function:	Real-time function generation and current regulation
SEE sensitivity	Internal Memory sensitive registers sensitive
Market & Choices	COTS possible combined with testing Fabrication technology Core voltage dependence? (we used 5V devices)
SEE Improvement	Do not use internal memory (no EDAC) Only use registers (low cross section) Refresh registers all the time Since used as a co-processor only => almost transparent reset by MCU in case of corruption detection Program and Dynamic Data stored in EDAC x SRAM

Digital Control Unit: Components - criteria 3/4

CPLD

Function:	Interlock state machine, Link between MCU & DSP and their peripherals: memories, DACs, ADCs, I/Os
SEE sensitivity	Code not considered as sensitive since stored in FLASH Flip Flop Cells corruption
Market & Choices	COTS possible combined with testing Fabrication technology Core voltage dependence? (we used 5V devices)
SEE Improvement	Flip Flop Cells corruption solved where possible by synchronous logic only and triple logic with majority voting

FPGA

General approach	SRAM based FPGAs are better not to be considered Anti-fuse are good by not modifiable Rad-tol reprogrammable FPGAs do now exist but were not available when the FGC was being designed

Digital Control Unit: Components - criteria 4/4

SRAM

Function:	High Speed read & write Memories Dynamic variables: internal and worldFip communication regulation algorithm
SEE sensitivity	High Sensitivity (non-EDAC ones)
Market & Choices	COTS not possible, military possible but very expansive
SEE Improvement	Use ONLY with EDAC

FRAM

Function:	High Speed but Finite access Non Volatile RAM Store Local constants imported from DATABASE (Load parameters, operating limits…)
SEE sensitivity	None
Market & Choices	COTS (MRAM now preferred as non access limit)

FLASH

Function:	High Speed read only Memories Main Program and Constants for MCU and DSP storage
SEE sensitivity	Low sensitivity
Market & Choices	COTS
SEE Improvement	CRC Control (boot) Software Auto-check (code confidence & integrity test)

LHC Tunnel Practical Example

How sensitive ìs an SRAM

What can be the effect on a large installation like CERN

CMOS Static RAM memory
- **1 Meg: 128K x 8-Bit**
- **5 Volt**

$$\sigma_{SEU} = \frac{\text{Nbr of Errors}}{\text{Nbr of hadrons [cm}^{-2}]}$$

- **$\sigma_{seu} = 10^{-8}$ cm^{-2} per device**
- **8 SRAM memory per Digital Controller**
  1 Power Converter = 1 Digital Controller
- **240 converters in RRs**
  752 converters in Arcs
- **Let's assume Radiation Level**
  RR : 1×10^{08} hadrons/cm^2 (E>20 MeV) per year
  ARCs: 4×10^{10} hadrons/cm^2 (E>20 MeV) per year

Expected number of single event errors in SRAM :

$240 \times 8 \times 10^{-8} \times 1 \times 10^{8} \cong 2'000$ errors / year = ~ 10 / day !

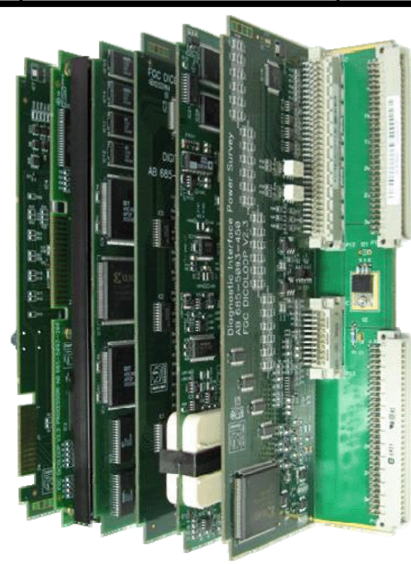
$752 \times 8 \times 10^{-8} \times 4 \times 10^{10} \cong 25 \times 10^{5}$ errors / year = ~ 10 / minute!!!

Memory "hardware Map"

Memory	Size KB	Vulnerable to Radiation?	Comments
HC16 internal SRAM	1	YES	Used as a SEU detector
C32 internal SRAM	2	YES	Used as a SEU detector
FRAM	64	NO	Used for non-volatile configuration
HC16 SRAM + EDAC*	256	YES but =>	Protected by an EDAC system
C32 SRAM + EDAC	512	YES but =>	Protected by an EDAC system
FLASH	512	NO	Holds Programs and Databases

* Dual port – also visible to C32

EDAC :
Error
Detection
And
Correction



When High Precision dictates its components

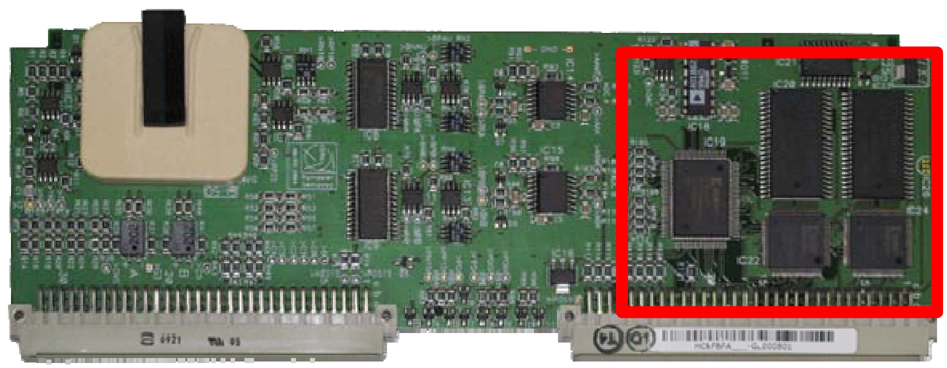
Function of the card: 2 ADC channels - 1 DAC channel

Analogue Medium Precision

Solution: Rad Tol tested COTS 16 bits ADC exists (LHC60A FGC)

Analogue High Precision

high performance ADCs are based on Sigma Delta design and require a digital filter based on a Xilinx Spartan 20 FPGA containing on 200 Kbits of corruptible SRAM



Solution:

Detect corruptions

- 2 channels / converter (2 DCCTs + 2 ADCs)
- Compare channels
- Detect unphysical behaviour in the measured signals

Implement a Reset on analog filters to clear SEE corruptions (few 1ms)

(DAC stays frozen during reset: transparent for converter & operation)

Implement Power cycle on analogue card (1 ms)

(DAC goes OFF, converter voltage goes down to 0V for ~2ms)

Global Reset: Action taken in case corruption detected

Fast Watchdog

Description	CPLD checks that software interrupt within +/-200us window
Speed & Delay	Trigger after 1.2ms – reset is 32ms later (time to log data)
Cause	Software crash in main program due to any cause

SlowWatchdog

Description	Simple monostable triggered by real-time OS context switch
Speed & Delay	~6s
Cause	Software crash in boot program

User

Description	Digital output under software control
Speed & Delay	On request by operator command
Cause	User requires a reset (e.g. for software update)

Multiple Bit Error

Speed & Delay	immediate
Cause	Multiple corrupted bits within 32-bit long data word detected by EDAC protecting the SRAM

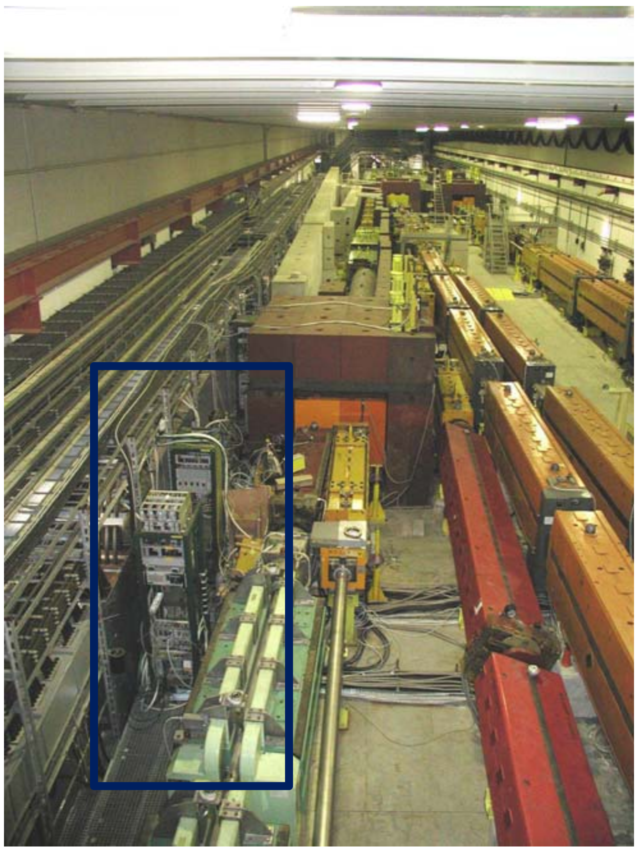
Consequence HC16 Reset + DAC frozen
=> Converter doesn't stop

Global Power Cycle: Action taken in case corruption => Total Crash

Cause	User Request Only (sending magic (long) frames across WorldFip network)
Mechanism description	User requests that the gateway sends a sequence of long (256 byte) messages (max length normally is 128 bytes) An analogue circuit detects the long messages and adds charge to a leaky capacitor for every message received If a threshold is exceeded a power cycle is triggered. The threshold is lower if the FGC is in the boot (after a crash) so crashed FGCs can be cycled separately to operating systems. Frame detection uses only the analogue FieldDrive device, not the MicroFip interface.
Consequence	Major Reboot trying to recover from major crash => Converter stop

CERN TCC2 (1999..2002)

A first radiation Experience for a lot of us.
Big size components can be tested.
Spectrum and Flux Not well known
Radiation not well characterized
T.I.D tests but *what* about S.E.E Results?



SPS experimental zone: test beam

Summary of equipment tested

A lot of basic components (PSU, DCDCs…) were tested and are up to know still installed in final equipment

- 1999 WorldFiP components
- 2000 Memory and microcontroller
- 2001 Analog component
- 2002 Complete power converter
- 2002 Digital Controller only

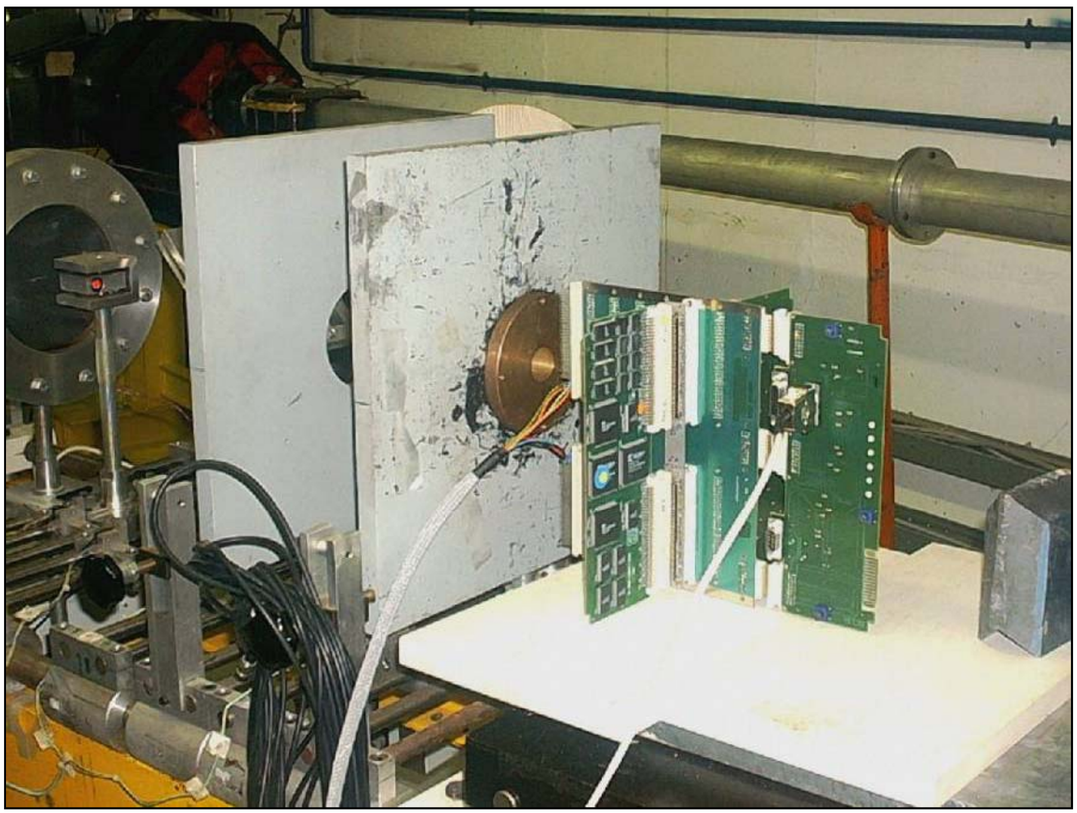
Critical components identified…

…but working ones limits and susceptibility is not really known.

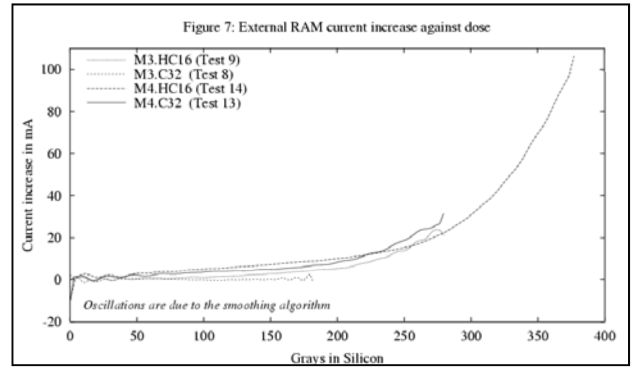
Not sufficient to ensure Rad-Hard characteristics.

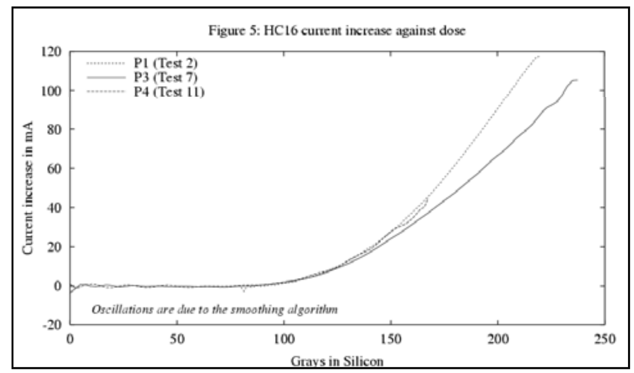
Louvain (2003)

- Small beam size so only a few components could be exposed at a time.
- Mono-energetic beam (60MeV protons)
- Well control flux and fluence
- Very high flux (up to 0.7 Gray/s)
- Quick tests (less than 15 minutes)

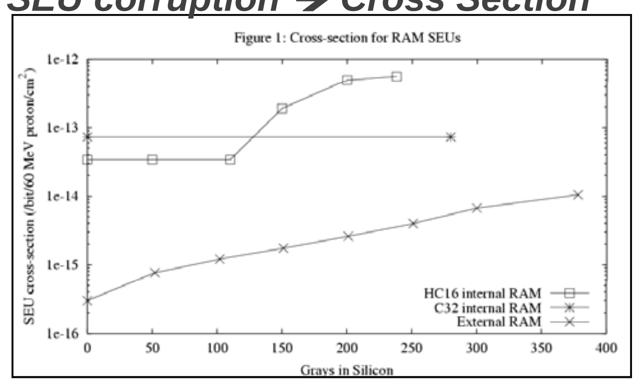


Current Consumption increase



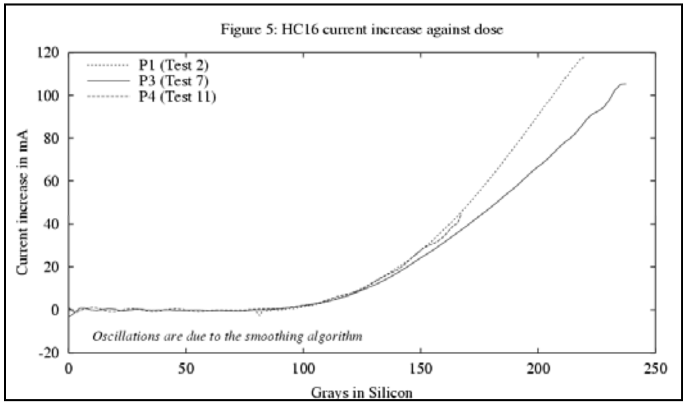


SEU corruption → Cross Section



Total Integrated Dose Effects

All components were measured and qualified concerning the T.I.D. effect.



Components	Current Treshold [Grays]	Failure Treshold [Grays]
MCU - HC16	100	240
DSP - C32	180	>280
EDAC	>200	>300
SRAM	200	>300
Flash Memory	200	>600
Xilinx CPLD	120	200

Single Event Upset

Protectable Items………………………..	External RAM		10^{-15} /bit/p/cm²
Unprotectable Items……………………	Xilinx CPLD latches	10^{2} bits	10^{-13} /bit/p/cm²
	Xilinx FPGA RAM	10^{5} bits	10^{-13} /bit/p/cm²
	Processor Registers	10^{3} bits	10^{-13} /bit/p/cm²
	Processor on-chip RAM	(not used)	10^{-13} /bit/p/cm²

Effect On Large Installation (750 LHC Tunnel Power Converters)

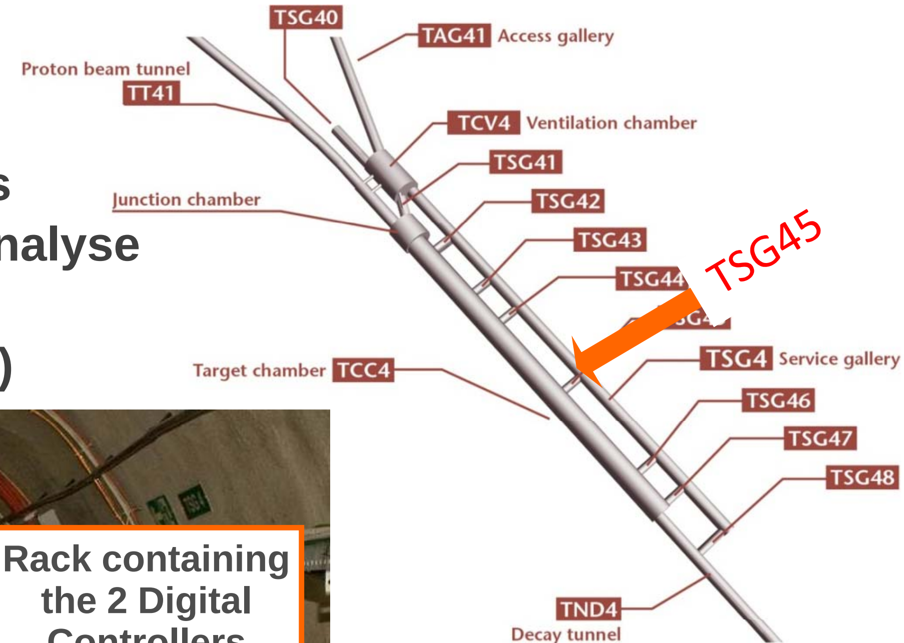
Processor register corruptions WILL cause crashes, but calculation shows that:

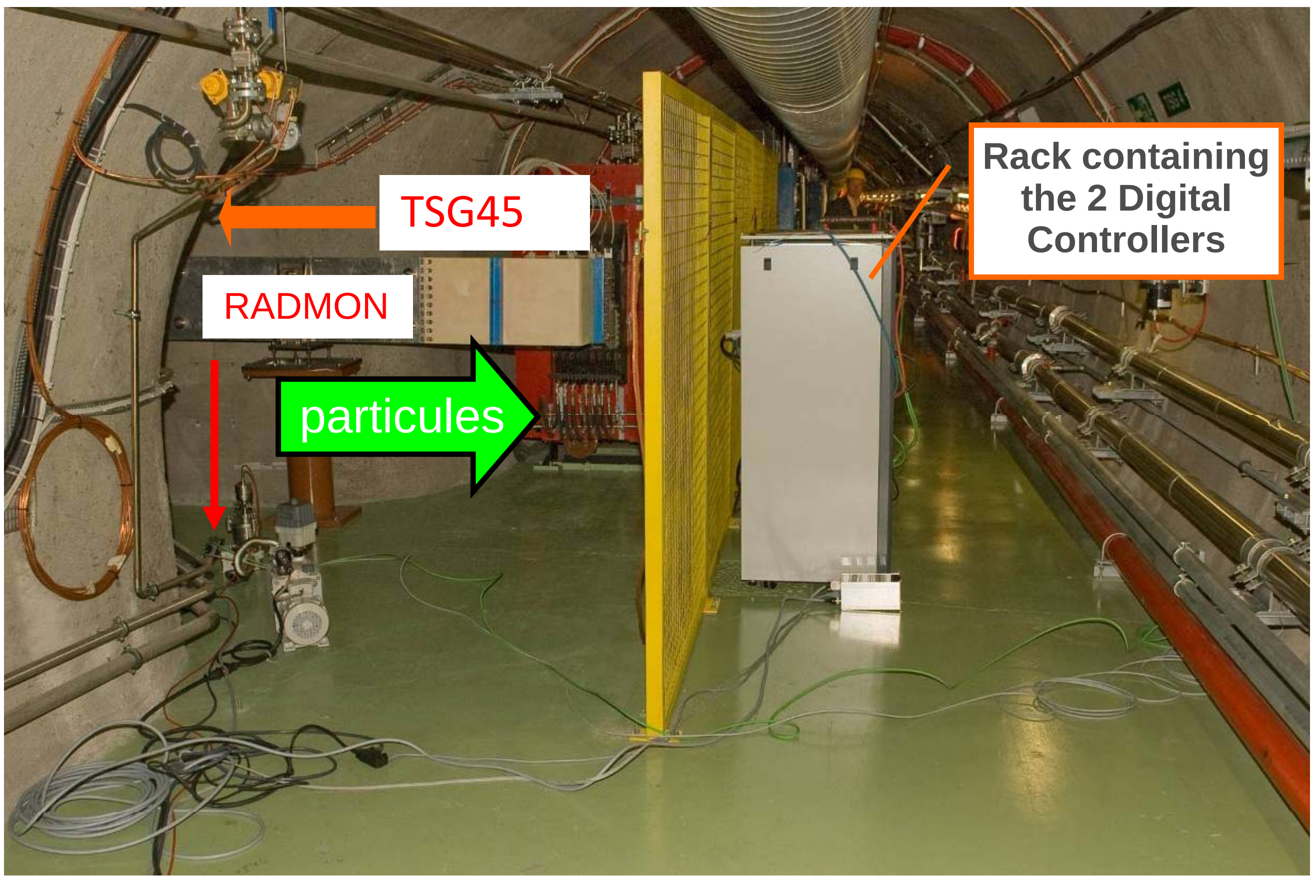
S.E.U. MTBF…………..1-4 week(s)
(some reset will be transparent)

Standard MTBF"…………………..1 week
(100,000 hours MTBF / system = 5.5 days /750 syst.)

CERN CNGS Gallery (2008)

Big size components can be tested.
LHC Tunnel conditions close to CNGS ones
Wide Energy spectrum, then less easy to analyse
Spectrum and Flux known and measured
A Great Parasitic Facilities (but parasitic!!!)





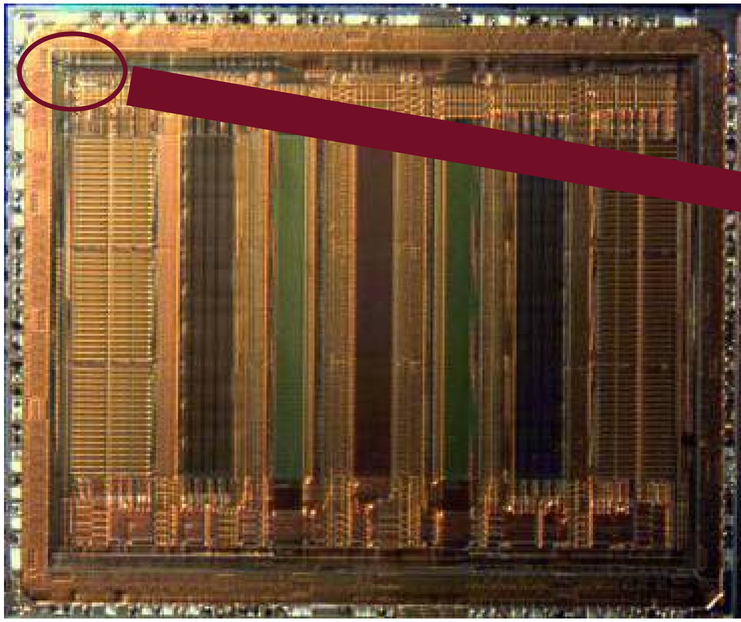
Since CNGS irradiation conditions are wide energy spectrum, and complete system are tested, diagnostic is not easy, and is harder since this experiment is parasitic to CNGS operation.

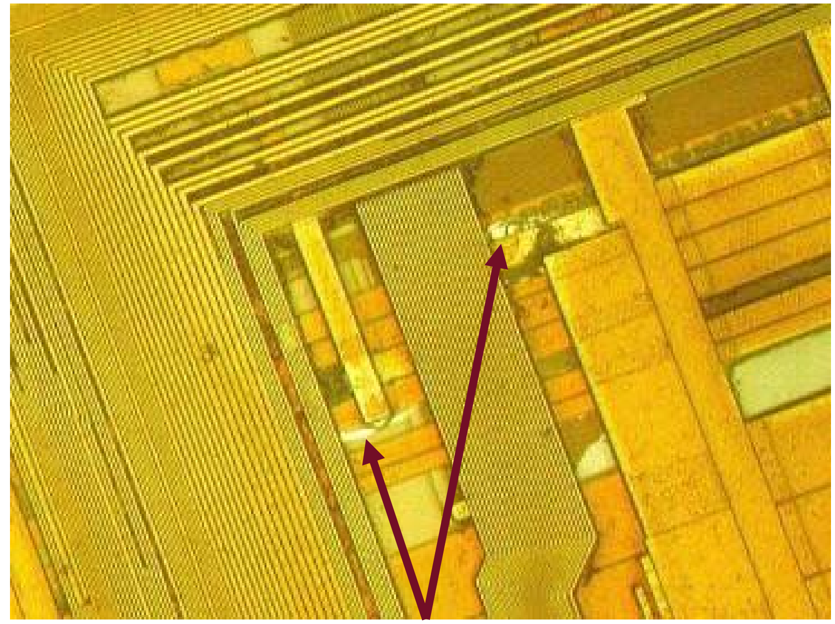
An irradiated item can only be accessed and removed following CNGS planning.

Digital Control Unit: Radiation Test – CERN CNGS Test Results

RESULTS on 2 Digital Controllers tested

- **7754 SEU counted on a FGC memories, all 100% corrected (EDAC)**
  ➔ EDAC and memory corruption detection works……………………………..
- **➔ 120 Gy on a FGC, and no influence seen on components (Louvain showed that critical limit was below 120 Gy).**
  CNGS = Louvain = Very good facilities (but parasitic!!)………………………
- **3-5 SEU on register C32 and HC16 (crash software if critical register)**
  ➔ Software Update with corruption detection feature for 2009………………
- **6 Stops (slow watchdog detection) but auto-recovering resetting software**
  ➔Auto recovery system works…………………………………………………
- **Analog Card High Precision Digital filter corrupted many times as expected showing the corruption process and major impact**
  ➔ Soft Update with digital filter corruption detection feature for 2009……..
- **3 crashes not explained on both FGC + 1 Lethal crash for one but manual-recovering using hardware Power Cycle implemented feature each time except for final lethal crash on one FGC**
  ➔ CPLD Single Event Destructive Latchup………………………………………





Single Event Destructive Latchup

Reminder: Louvain Test: "*only 13 CPLDs being tested*"

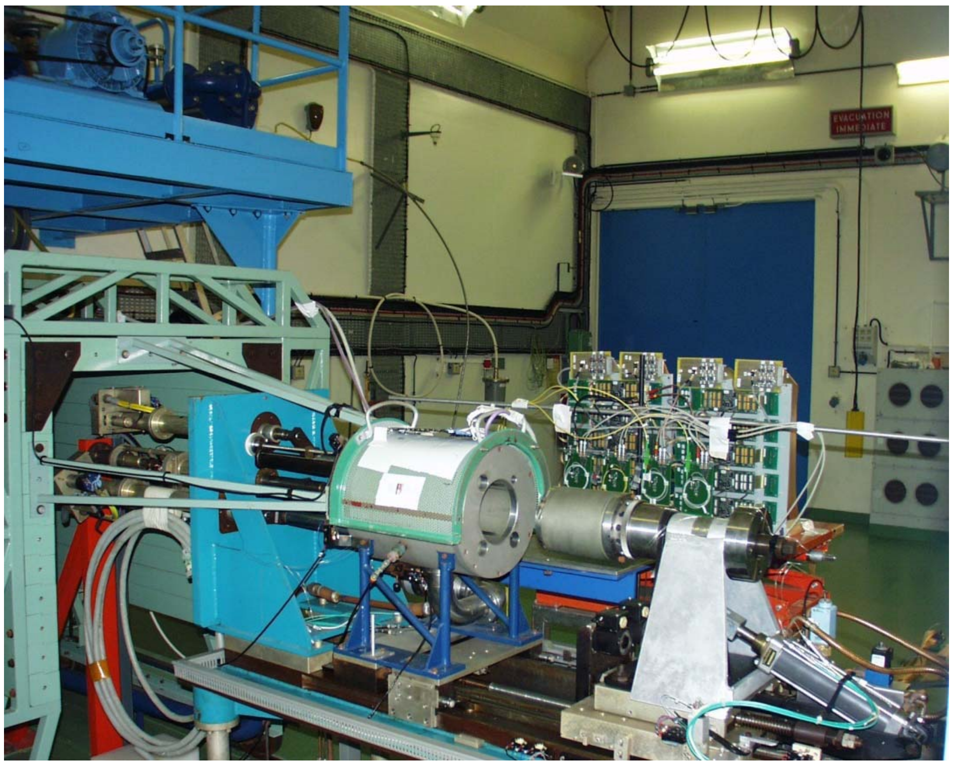
Single Event Effects

Protectable Items………………………….	External RAM		10^{-15} /bit/p/cm²
Un-protectable Items……………………	Xilinx CPLD latches	10^2 bits	10^{-13} /bit/p/cm²
	Xilinx FPGA RAM	10^5 bits	10^{-13} /bit/p/cm²
	Processor Registers	10^3 bits	10^{-13} /bit/p/cm²
	Processor on-chip RAM	(not used)	10^{-13} /bit/p/cm²

Actions: a 2009 CNGS Test campaign on 100 Xilinx CPLDs will gives the probability of such a destructive event.

Prospero (2009)

Source of Neutrons: Reactor
Big size components can be tested.
Mostly Mono-energetic neutron beam
1MeV peak, 10MeV maximum
Fluence : 1.5x10^{-12} neutrons/3h

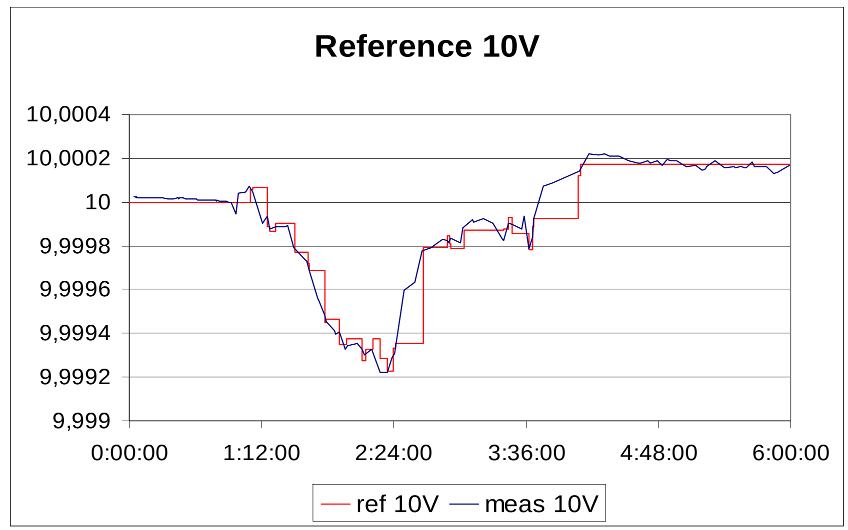


SEU should be less visible with Only 1Mev neutron. Impact on analog devices is assumed, and degradation effects of these 1MeV neutron on die is expected…

SEU corruption ➔ Cross Section

Current Consumption increase measurement

Reference Voltage source



RESULTS on 2 Digital Controllers tested

- **1468 SEU counted on FGC external memories*, all 100% corrected**
  ➔ EDAC and memory corruption detection works……………………………..

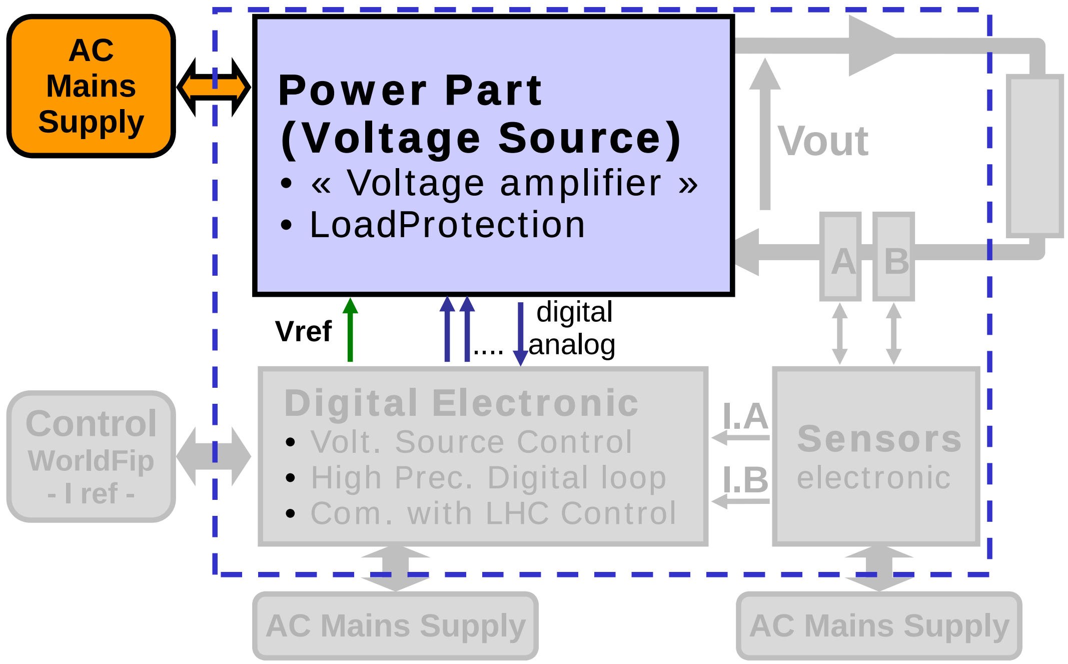
- **No SEU on register C32 and HC16**
- **No SEU on Internal* RAM C32 and HC16**
- **No corruption on Analog Card High Precision Digital filter**
- **Small Deviation (tolerable) on voltage references used for high precision**
  ➔ 1-10MeV Neutron impact on Digital Controller is low……………….…….

Comparison between CNGS and Prospero (different flux)

Item	CNGS SEU [/ year]	Prospero SEU [/ year]
Internal HC16 RAM	115	0
Internal C32 RAM	40	0
External RAM HC16	2 000	110
External RAM C32	500	37

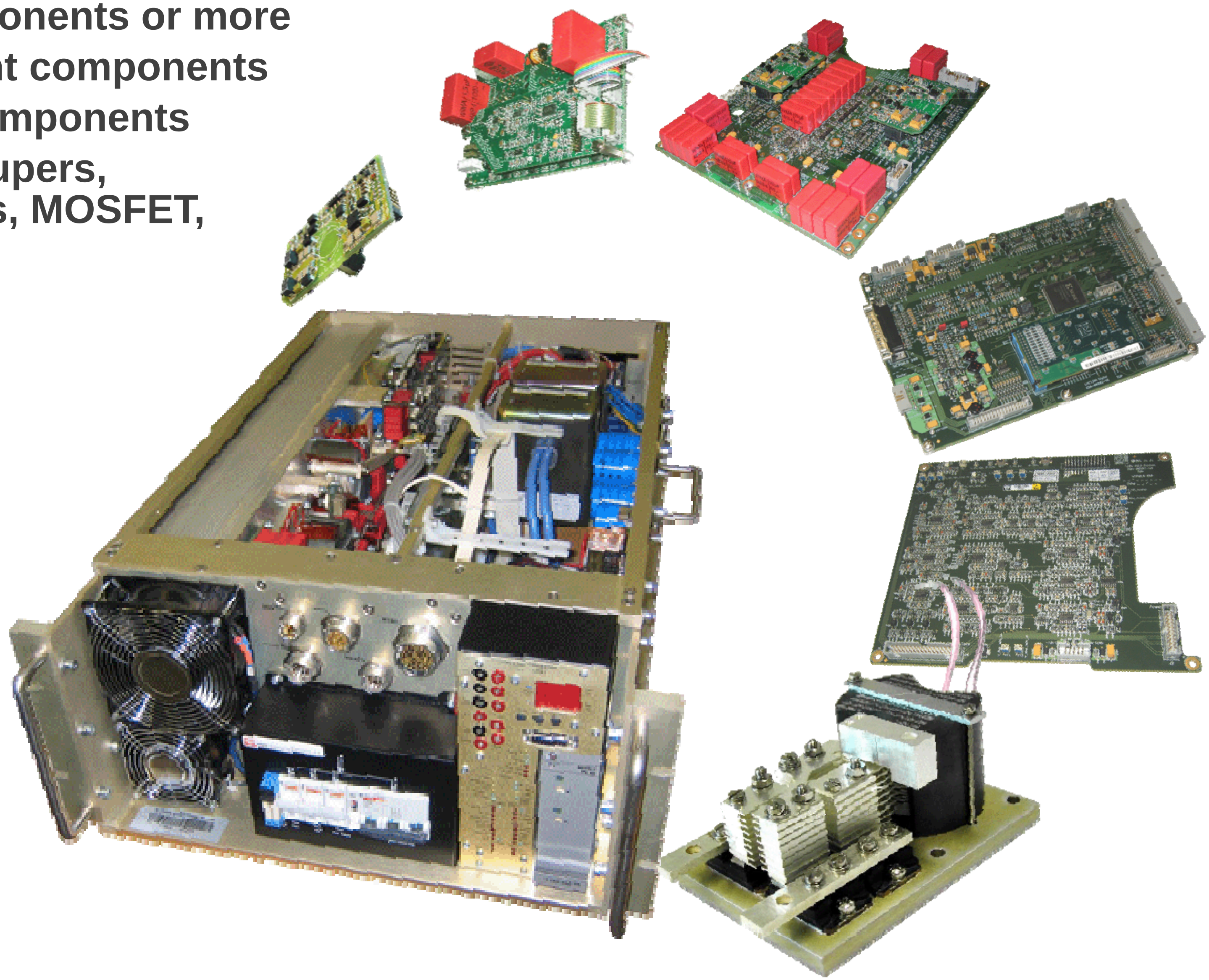
Prospero = 1-10Mev Neutrons
CNGS = Wide Energy spectrum particles

The Power Part Design

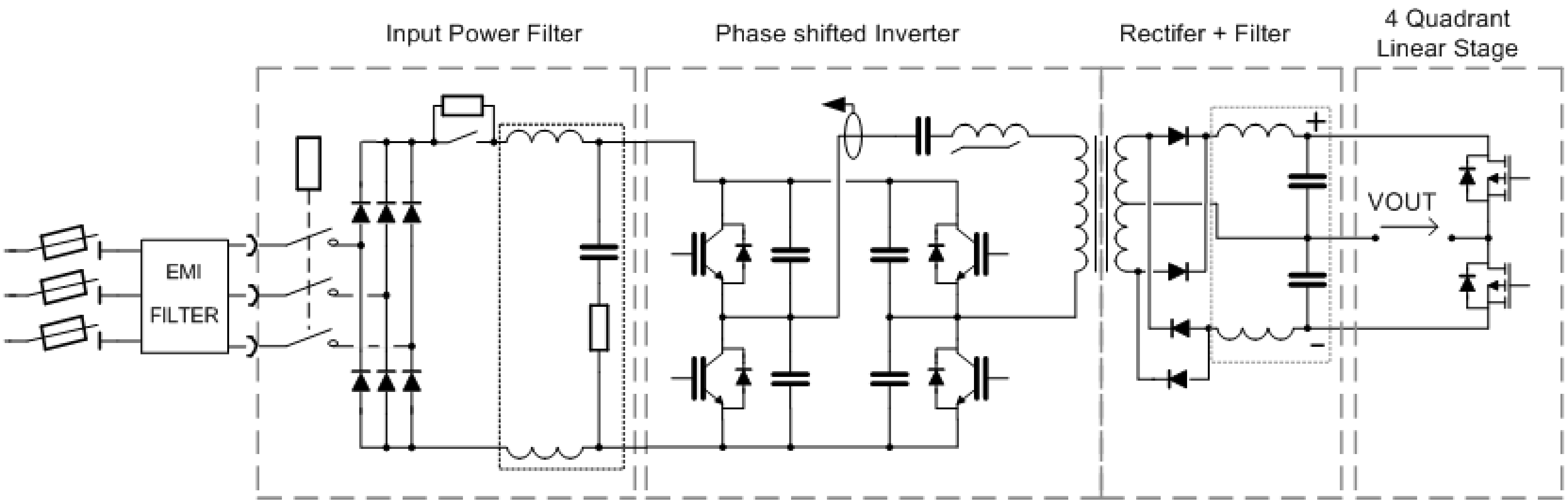


How does a Power Part look like

- Up to 4 000 components or more
- Up to 700 different components
- Analog mainly components
- Sensors, Optocoupers, Transistors IGBTs, MOSFET, Bipolars
- AC-DC PSU
- DC-DCs



Overview of hardware internal components layout



A power converter can be designed with relatively basic components excepts some inner controller like PWM or Power Transistor Drivers.

Main well known worries come from

- Diode and Power Transistors switching:

➔ Voltage Over Rating is always applied (mandatory at CERN regarding the CERN mains network which can dramatically increases)

- Optocouplers often used in DCDC or isolating some signals.

➔ Use radiation hard COTS components (tests)
➔ Design shall tolerate gain degradation

Design Rules applied at CERN

- Minimise the number of components
  LHC60A-08V converter is made using very low number of components compared to other types.

- Use already tested op-amp, comparator, voltage reference circuits as much as possible (radiation impact already known)

- Pay attention on Material used: tantalum capacitor not used, insulation material critical

- When component is not known, test of it (PWM, IGBT Drivers)

- Test new advanced / complex components and / or design some backup pure analog (radiation tolerant components only) old fashion controller in case of doubts on some PWM, Driver, CPLD, DCDC, AC-DC…

- Implement degradation known effect in design
  - MOSFET drive ±15V when possible for VGS threshold lowering with TID
  - Optocouplers are driven with minimum polarisation current and taking in account the predictable loss of gain

IGBT High Frequency Driver Example

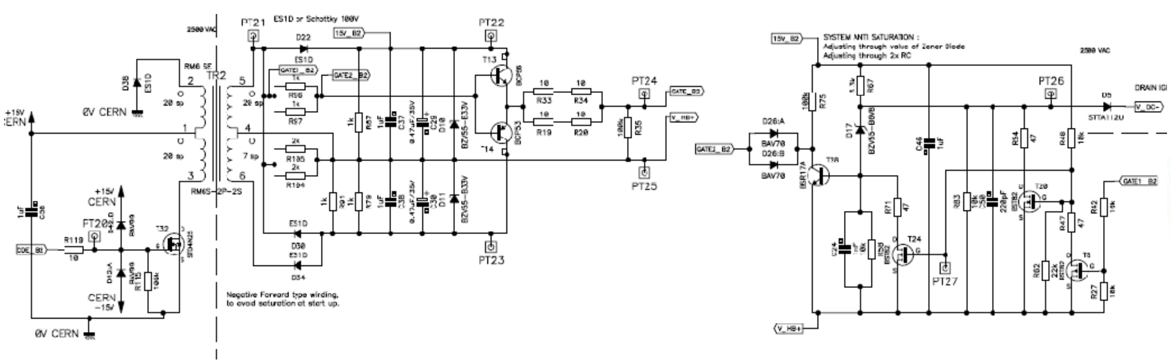
- High Performances Drivers can be selected, simplifying a lot the design phase of a converter.
- When some doubt exist on its S.E.E susceptibility, an alternate design can be proposed in case of.

Product from specialist Manufacturer

- Was tested in TCC2.
- Valid up to a T.I.D of 50-60 Gy.

OR: Same Function CERN designed

- Design based only on very basic radiation tolerant components. (magnetic + transistors + resistance and capacitors). No optocoupler to transmit the insulated control to Transistor Gate.



DC-DC

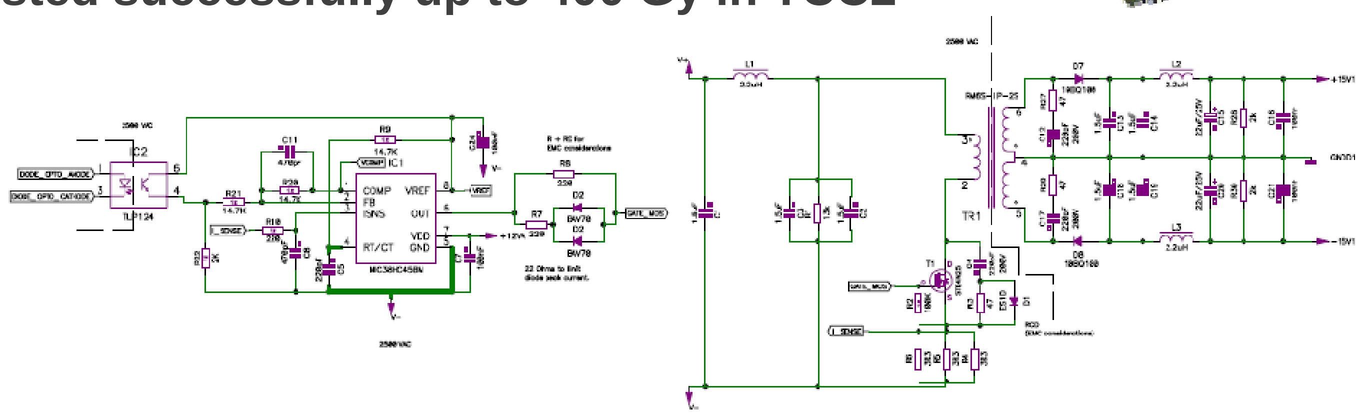
- COTS DC-DC manufacturers aims a very high efficiency for their product (size reduction, loss reduction, competitive market).
- Margins on power diodes and MOSFETs are not always respecting the rule of a 2x margin factor in voltage.

Product from specialist Manufacturer

- Selected ones tested in TCC2.

OR: Same Function CERN designed

- Design based only on radiation tolerant components
- Margin on power components are very high: 200V Mosfet main switch on 15V bus being switched (50V max VDS)
- Tested successfully up to 400 Gy in TCC2



CERN TCC2 (1999..2002)

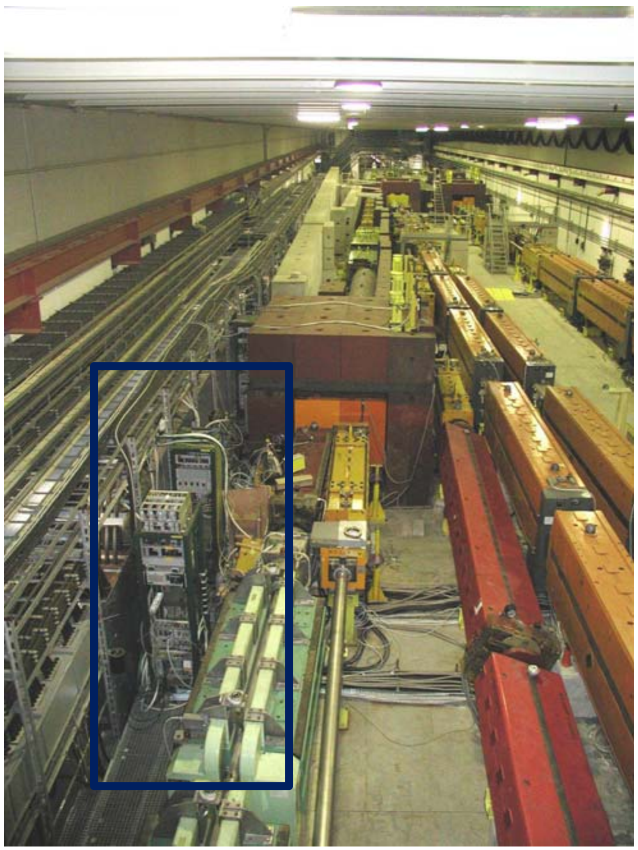
A first radiation Experience for a lot of us.

Big size components can be tested.

Spectrum and Flux Not well known

Radiation not well characterized

T.I.D tests but *what* about S.E.E Results?



SPS experimental zone: test beam

Summary of equipment tested

A lot of basic components (PSU, DCDCs…) were tested and are up to know still installed in final equipment

- **2001 Analog component**
- **2002 Complete power converter**

Critical components identified…

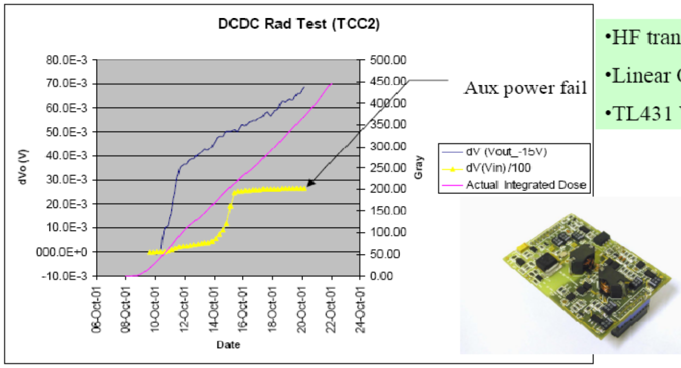
…but working ones limits and susceptibility is not really known.

Not sufficient to ensure Rad-Hard characteristics.

Some circuits Tested (integrated items)

- AC-DCs PSU, Drivers, DC-DCs, DCCTs...

Sub-Circuits – DC/DC



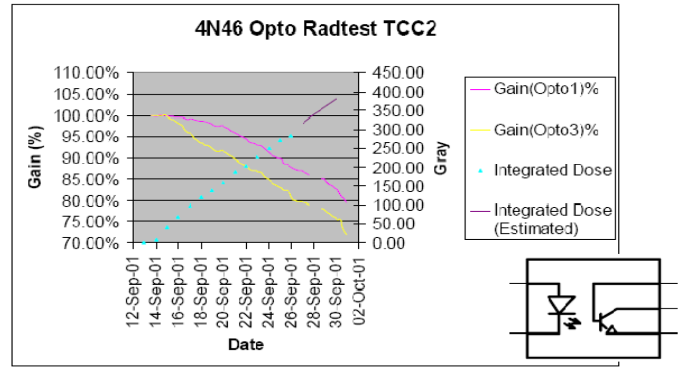
•HF transformer
•Linear Output
•TL431 Vref

AC-DC Power Supplies

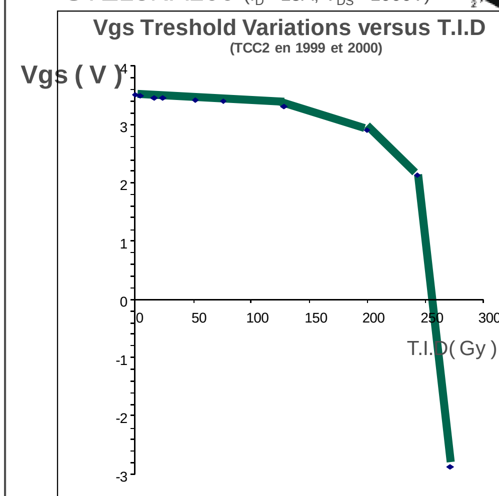
Some Components tested

- MOSFETs, LEM, PWM, Optocouplers...

Sub-Circuits - Optocoupler

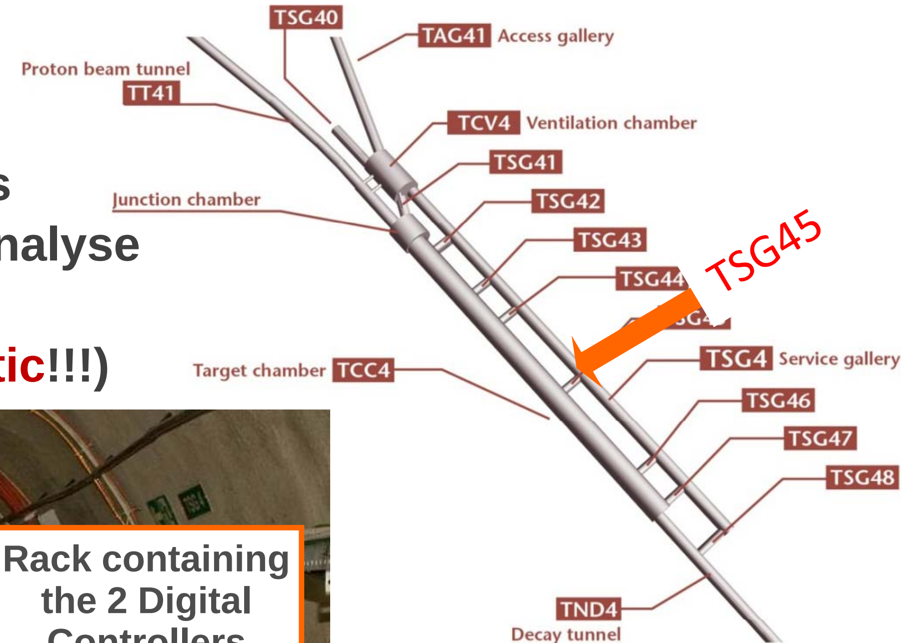


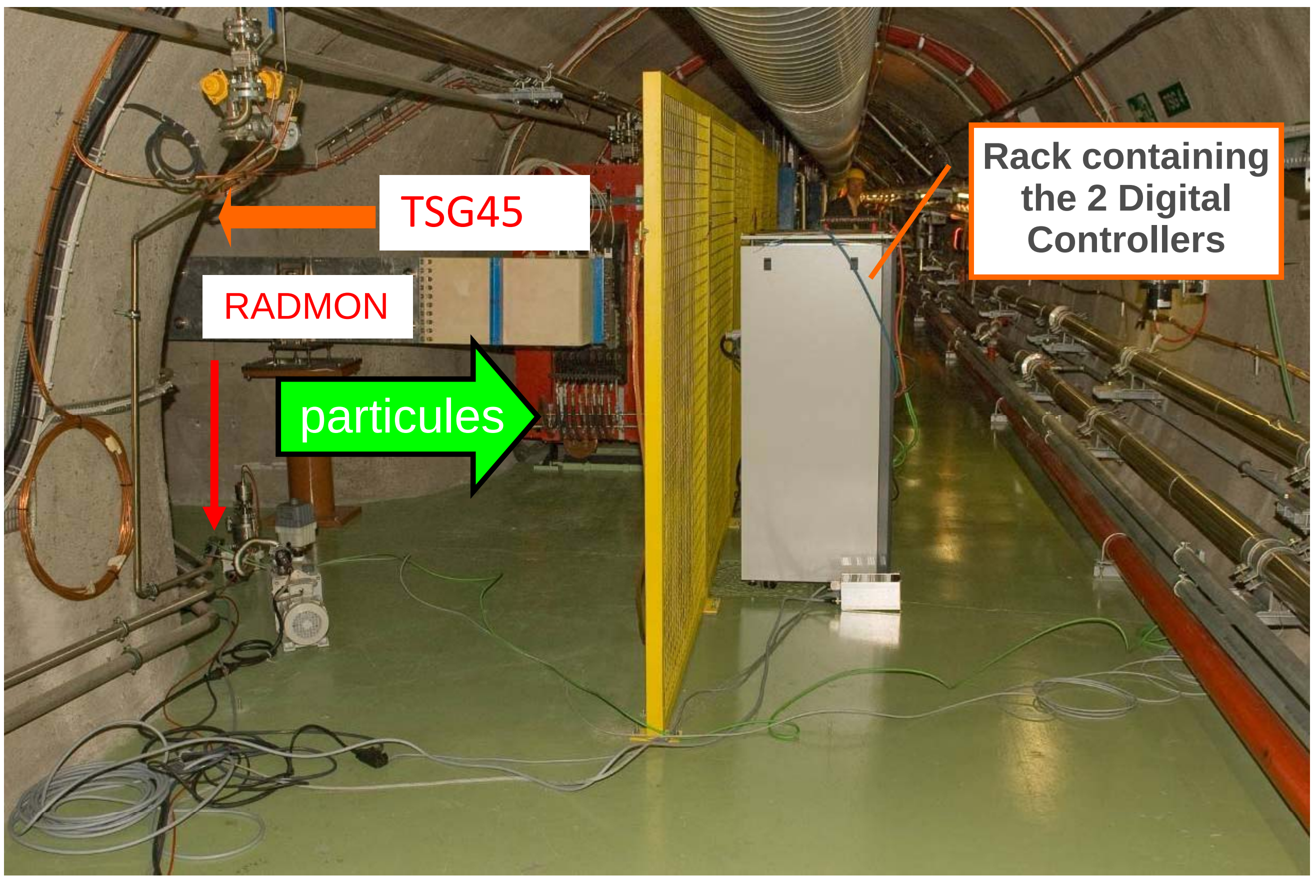
N - CHANNEL ENHANCEMENT MODE
FAST POWER MOS TRANSISTOR
STE15NA100 (I_D= 15A, V_{DS}= 1000V)



CERN CNGS Gallery (2008)

- **Big size components can be tested.**
- **LHC Tunnel conditions close to CNGS ones**
- **Wide Energy spectrum, then less easy to analyse**
- **Spectrum and Flux known and measured**
- **A Great Parasitic Facilities (but still parasitic!!!)**

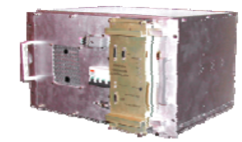




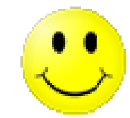
Since CNGS irradiation conditions are wide energy spectrum, and complete system are tested, diagnostic is not easy, and is harder since this experiment is parasitic to CNGS operation.

An irradiated item can only be accessed and removed following CNGS planning.

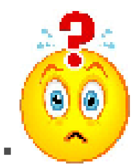
RESULTS on 2 LHC60A-08Vconverters tested



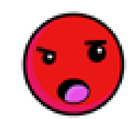
- **Aux DCDC & PSUs chosen survived up to 100 Gy ($5E^{10}$ part/cm^2)
  All control electronics also survived same conditions
  ➔Test in TCC2 were ok regarding to test condition in CNGS………………..**



- **Since converter was always tested using a FGC Digital Controller, it was powered ON (delivering power to its load) only for some days due to Digital Controller crash.
  ➔Tests are not complete since power components were not 'active' (switching) due to Digital Controller crash………………………………………….**



➔One Power Mosfet in input power filter crashed (short circuit), even being a 1000V one. Study and other test foreseen in CNGS…………………....



Test of a whole power converter is costly (loss of a complete unit) and difficult since it requires Digital Controller to work with all diagnostic being available from field bus.

➔A crash in the digital controller then jeopardize the power part test.

➔ Necessity to mount a test without the Digital Controller, but high effort required to get status from the experience

Conclusions

- **People designing Power Converters are not familiar to S.E.E phenomena since almost never facing it.**
- **Since all sensitive devices and components were placed in the digital controller, goal to achieve is more severe on this part regarding S.E.E.**
- **Nevertheless, this “sectorization” of power and control function was a good choice since it didn’t add extra risks and work to Power Part Converter design team**
- **Power part was mainly designed respecting the basic known rules, and selecting tested devices only when more complex components or sub-assemblies were considered.**
- **Sometimes it is good to look backwards how old fashion electronics were design to re-design now fully integrated function in S.E.E sensitive items.**
- **Test is a major issue when dealing with power converters. Equipments are big size when a final test is required, and some are even water cooled.**