A Hadron Calorimeter with Resistive Plate Chambers

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Argonne National Laboratory

Presented by

Andy White
University of Texas at Arlington

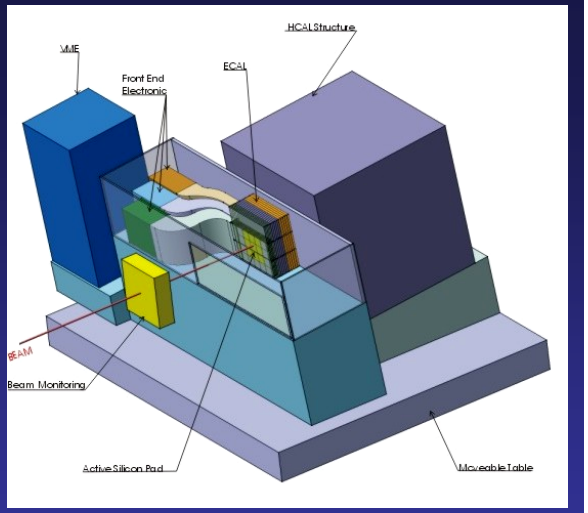
LCWS 2006, Bangalore, India, March 9 – 13, 2006

Collaborators

Institute	CALICE	Contributions to date
Argonne	Yes	R&D on RPCs Conceptual design of electronic readout system Specification of front-end ASIC Measurements with prototype front-end board Evaluation of front-end ASIC prototype
Boston	Yes	
Chicago	Yes	Measurement of geometrical acceptance
Fermilab	No	Design of front-end ASIC
Iowa	Yes	Investigation of HV supplies
IHEP Protvino	Yes	R&D on RPCs
Regina	Yes	

197 Physicists 34 Institutes 9 Countries 3 Regions

HCAL R&D Goal



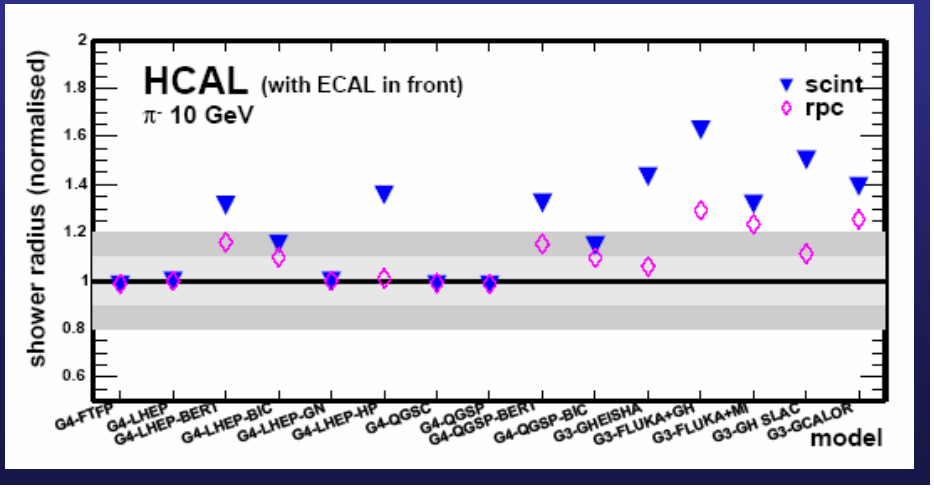
Prototype section (PS)

1 m^3 (to contain most of hadronic showers)
40 layers with 20 mm steel plates as absorber
Lateral readout segmentation: 1 cm^2
Longitudinal readout segmentation: layer-by-layer
Instrumented with Resistive Plate Chambers (RPCs) and Gas Electron Multipliers (GEMs)

Motivation for construction of PS and beam tests

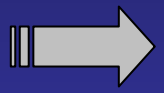
Validate RPC and GEM approach (technique and physics)
Validate concept of the electronic readout
Measure hadronic showers with unprecedented resolution
Validate MC simulation of hadronic showers
Compare with results from Scintillator HCAL

Comparison of hadron shower simulation codes by G Mavromanolakis



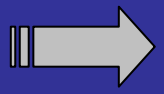
Staged approach

I R&D on RPCs
Development of conceptual design of electronic readout



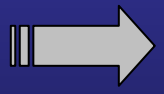
Tests with cosmic rays and in particle beams **Done**

II Prototyping of RPCs for prototype section (PS)
Prototyping of all components of electronic readout for PS



Slice test in particle beam **Planned for November 2006**

III Construction of PS



Detailed test program in Fermilab test beam **Earliest in 2007**

IV Design of Hadron Calorimeter for ILC detector **Started**

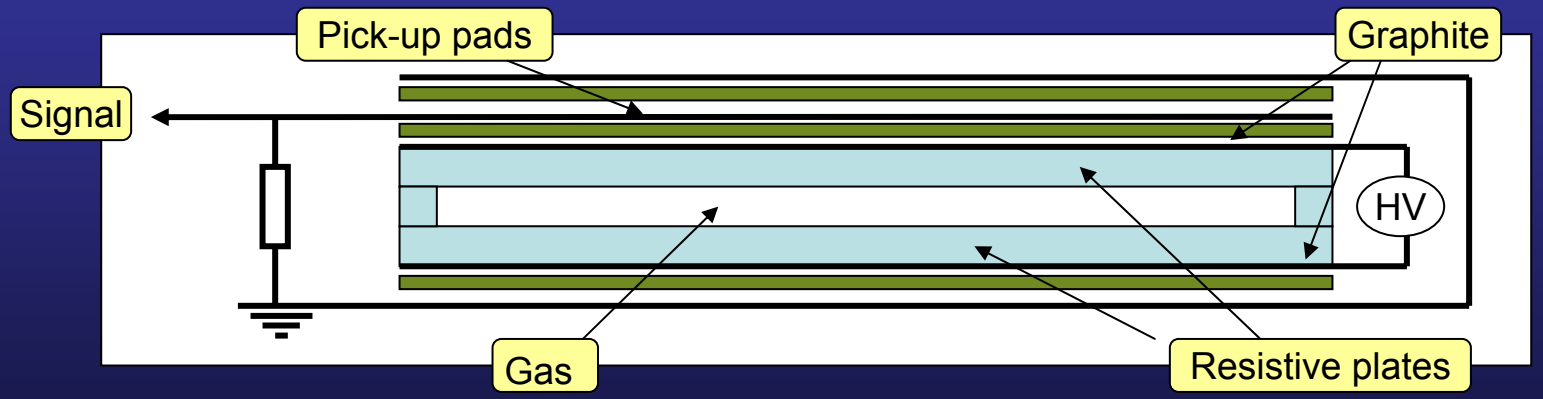
Status of RPC R&D

Measurement	RPC Russia	RPC US
Signal characterization	yes	yes
HV dependence	yes	yes
Single pad efficiencies	yes	yes
Geometrical efficiency	yes	yes
Tests with different gases	yes	yes
Mechanical properties	?	yes
Multipad efficiencies	yes	yes
Hit multiplicities	yes	yes
Noise rates	yes	yes
Rate capability	yes	yes
Tests in 5 T field	yes	no
Tests in particle beams	yes	yes
Long term tests	ongoing	ongoing
Design of larger chamber	yes	ongoing

Virtually all R&D completed

Default RPC chamber designs for PS

Layer	Russia	US
Resistive layer anode	Anode readout pads	1÷50 MΩ/□
Glass thickness in [mm]	0.55	1.1
Gas gap in [mm]	1.2	1.2
Glass thickness in [mm]	0.85	1.1
Resistive layer cathode	~1 MΩ/□	1÷50 MΩ/□



Recent Tests in Fermilab's MT6 Test Beam

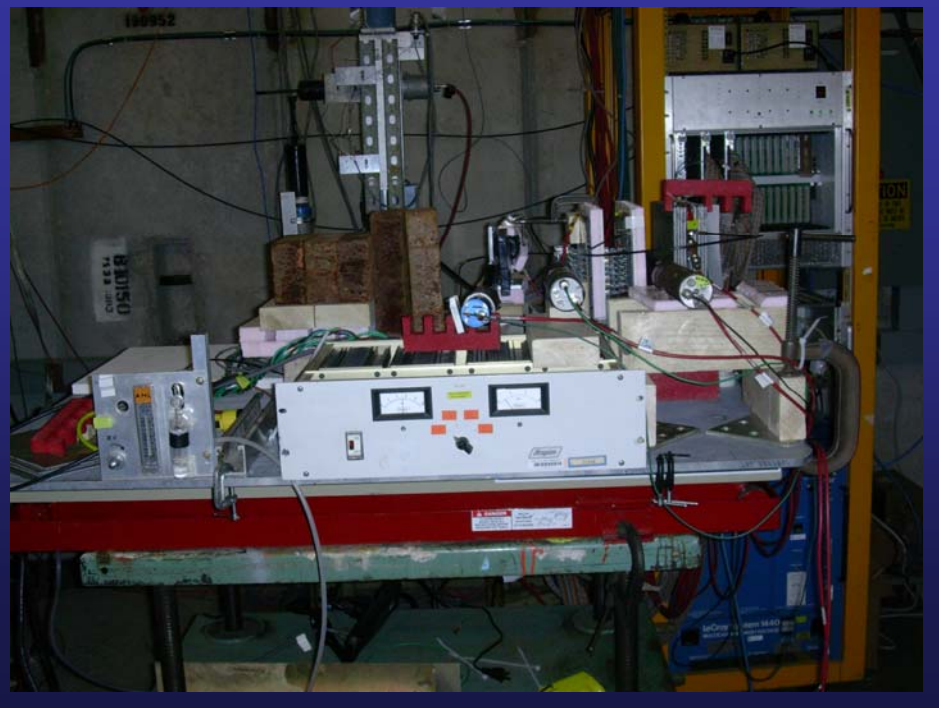
Signed MOU in December 2005

Dave Underwood spokesperson

T955

Started setting-up behind beam dump in January 2006

2 RPCs with 64 channels and VME readout (events in the two chambers can be correlated)
→ Chambers based on different design (1 vs 2 glass plates)
1 RPC with 32 channels and shift register readout (independent DAQ)
Beam telescope with 4 scintillation counters
→ Trigger area ~ 4 cm^2



Moved into beam on February 22

Took data for ~2 x 6 hours
Beam = 120 GeV/c protons
4 second spill every 2 minutes
Requested variation of beam intensity between 70 and 5000 Hz/cm^2
Also took data with block of steel in front of RPCs

Experiences at MT6

a) Safety

Trouble getting gas system approved by safety review committee
Committee requested
- use of approved tanks
- use of gas fittings (worse) instead of water fittings (much better)
- detailed description of gas mixing procedure

Spent weeks in trying to accommodate safety committee

b) Environment

February was particularly cold and wet
Freon liquefied in tanks and gas lines (when outside beam area)
Roof leaks → puddles, high humidity

c) Beam intensity

Easily adjusted to requested values
Usually new setting established between spills (no beam losses for data taking!)
→ Many thanks to FNAL beam crew for excellent performance

d) Results soon

Measurement of efficiency and pad multiplicity as function of particle rate
→ Used fixed threshold, but ran with different high voltage settings
Measurement of correlation of pad multiplicity between 2 RPCs

Electronic Readout System for Prototype Section

400,000 readout channels

Conceptual Design of Readout System

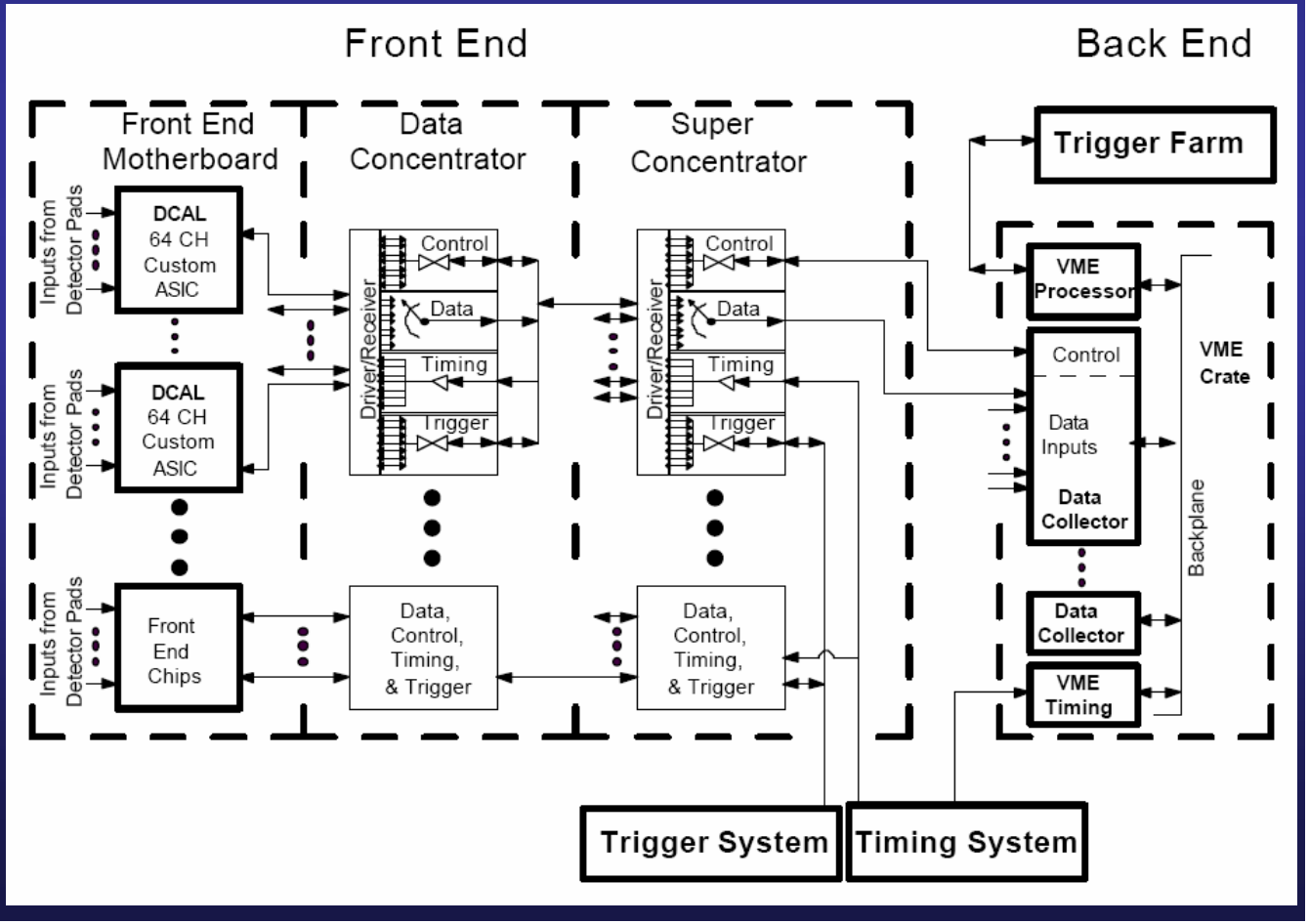
I Front-end ASIC and motherboard

II Data concentrator

III Super Concentrator

IV VME data collection

V Trigger and timing system



Specification of system completed

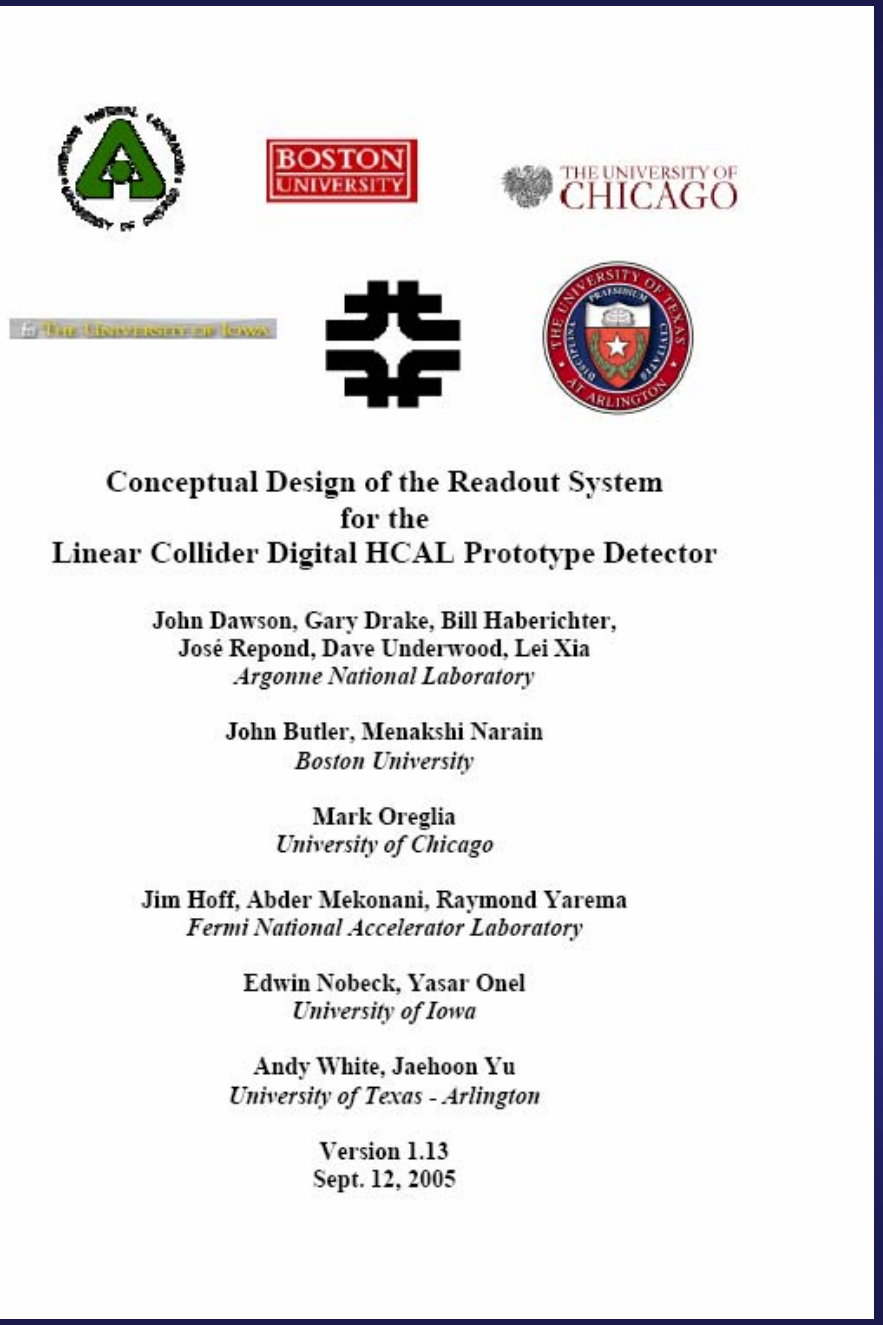
Document

Written by Gary Drake (ANL)

Released in September 2005

Contains all details of system

Basis for design work of subsystems
Counts 57 pages



Conceptual Design of the Readout System for the Linear Collider Digital HCAL Prototype Detector

John Dawson, Gary Drake, Bill Haberichter, José Repond, Dave Underwood, Lei Xia
Argonne National Laboratory

John Butler, Menakshi Narain
Boston University

Mark Oreglia
University of Chicago

Jim Hoff, Abder Mekonani, Raymond Yarema
Fermi National Accelerator Laboratory

Edwin Nobeck, Yasar Onel
University of Iowa

Andy White, Jaehoon Yu
University of Texas - Arlington

Version 1.13
Sept. 12, 2005

Multiplexing of readout system for PS

Component	#/chamber	#/plane	#/channels/unit	Total # of units
Planes	0.333	1	9216	40
Chambers	1	3	3072	120
DCAL ASIC	48	144	**64**	5760
FE motherboards	2	6	1536	240
Data concentrators	4	12	**768**	480
Super concentrators	0.667	2	**4608**	80
Data collectors	-	0.166	**55,296**	7
VME crates	-		**387,072**	1

Front-end ASIC…

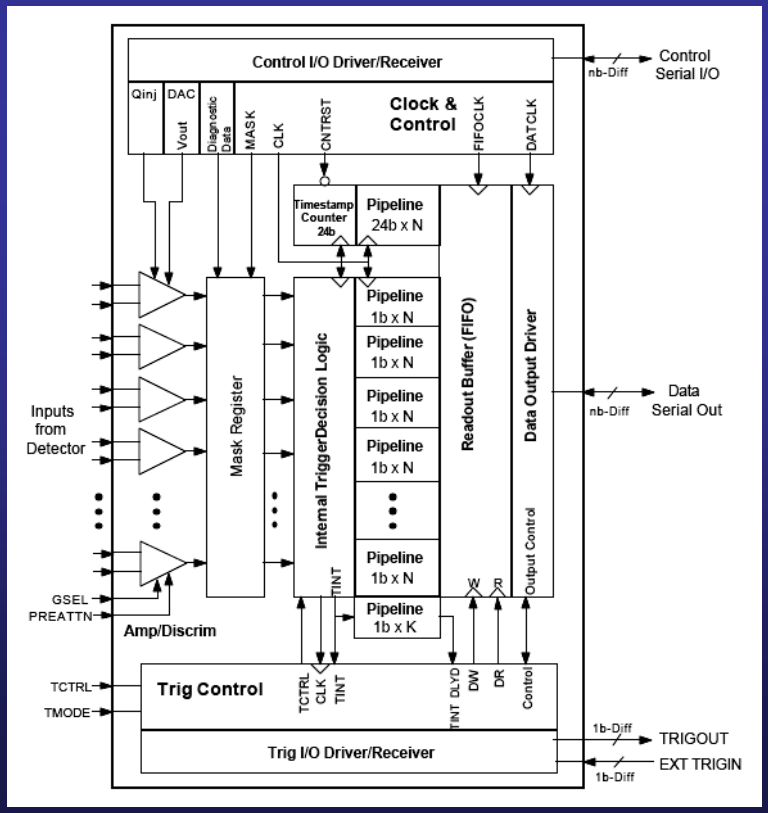
64 inputs with choice of input gains

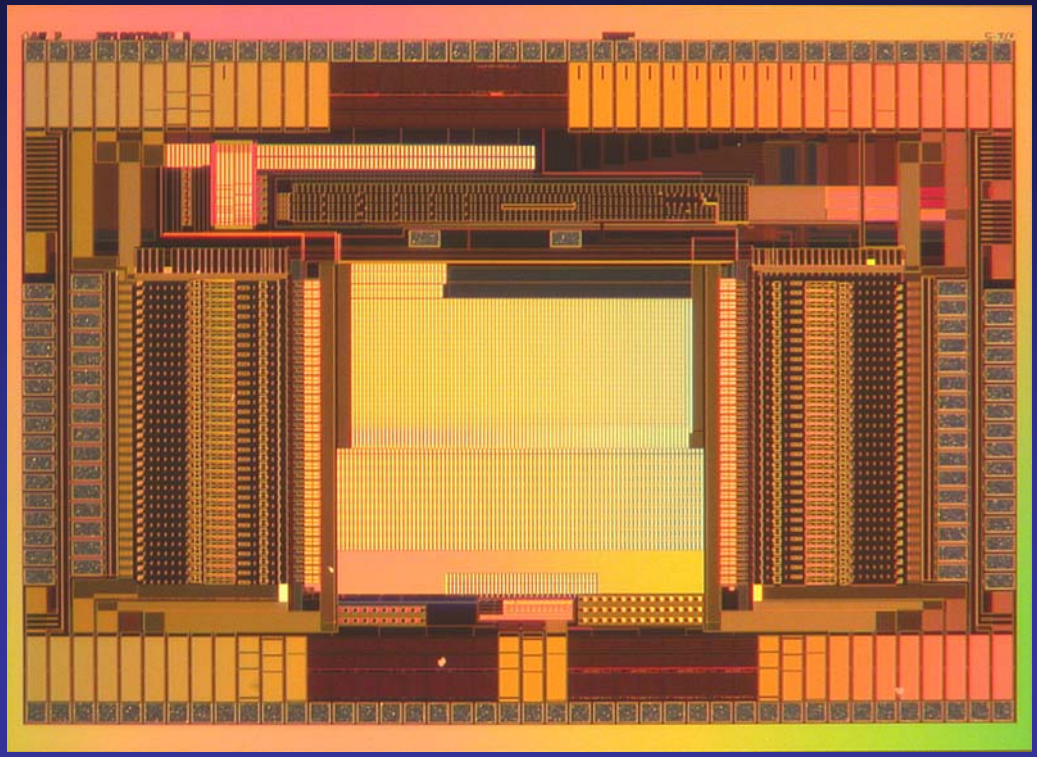
RPCs (streamer and avalanche), GEMs…

Triggerless or triggered operation

100 ns clock cycle

Output: hit pattern and time stamp





Design work at FNAL

Abderrezak Mekkaoui
James Hoff
Ray Yarema

Design work started in June, 2004

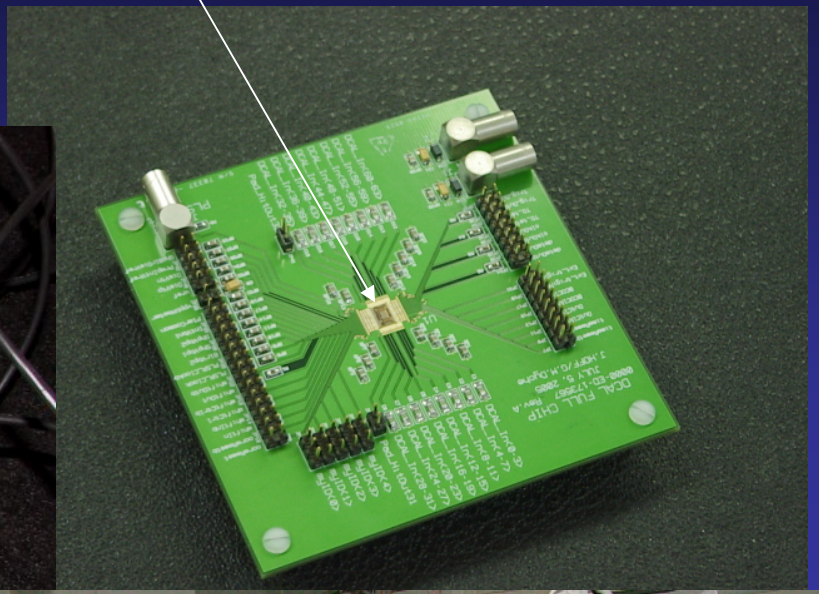
Prototype run submitted on March 18th 2005

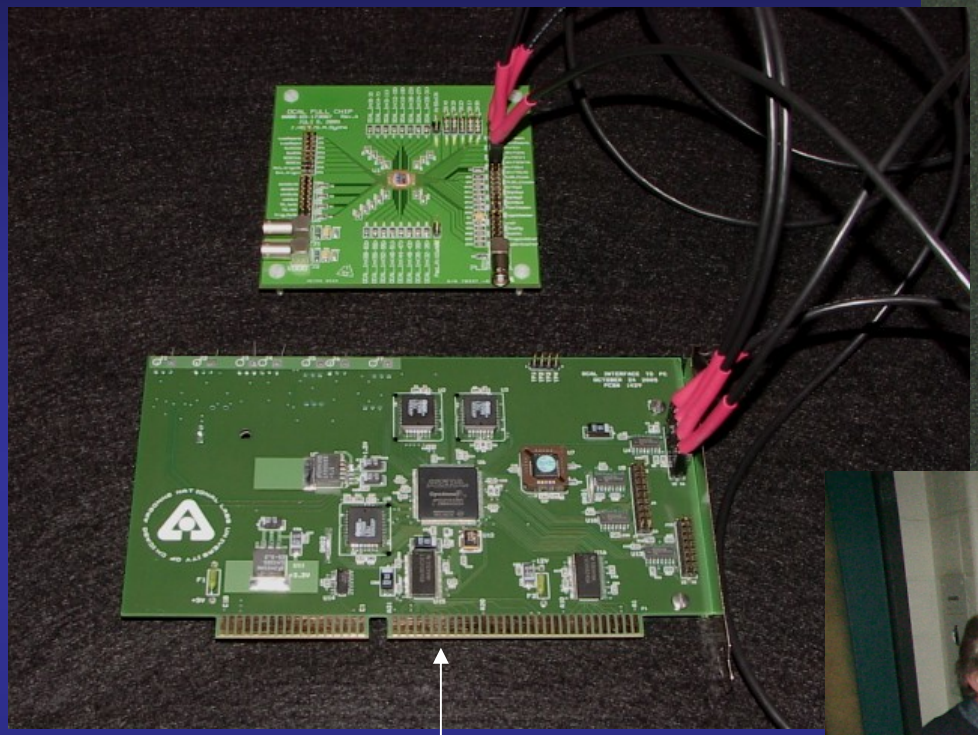
40 unpackaged chips in hand

Tests started…

Tests of ASIC at Argonne

Unpackaged chip housed on small test board





Built computer interface for test

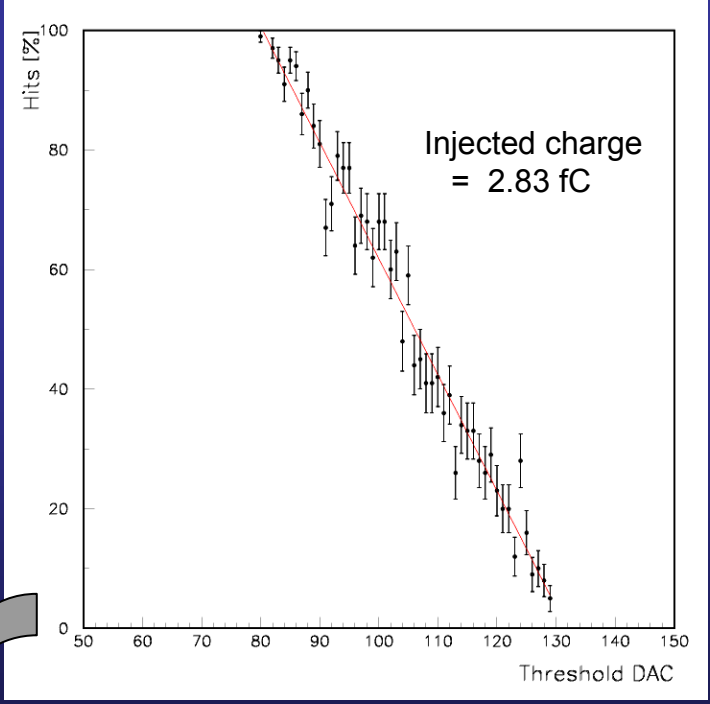
Wrote software for automated tests

First Results

a) All digital functions seem operational

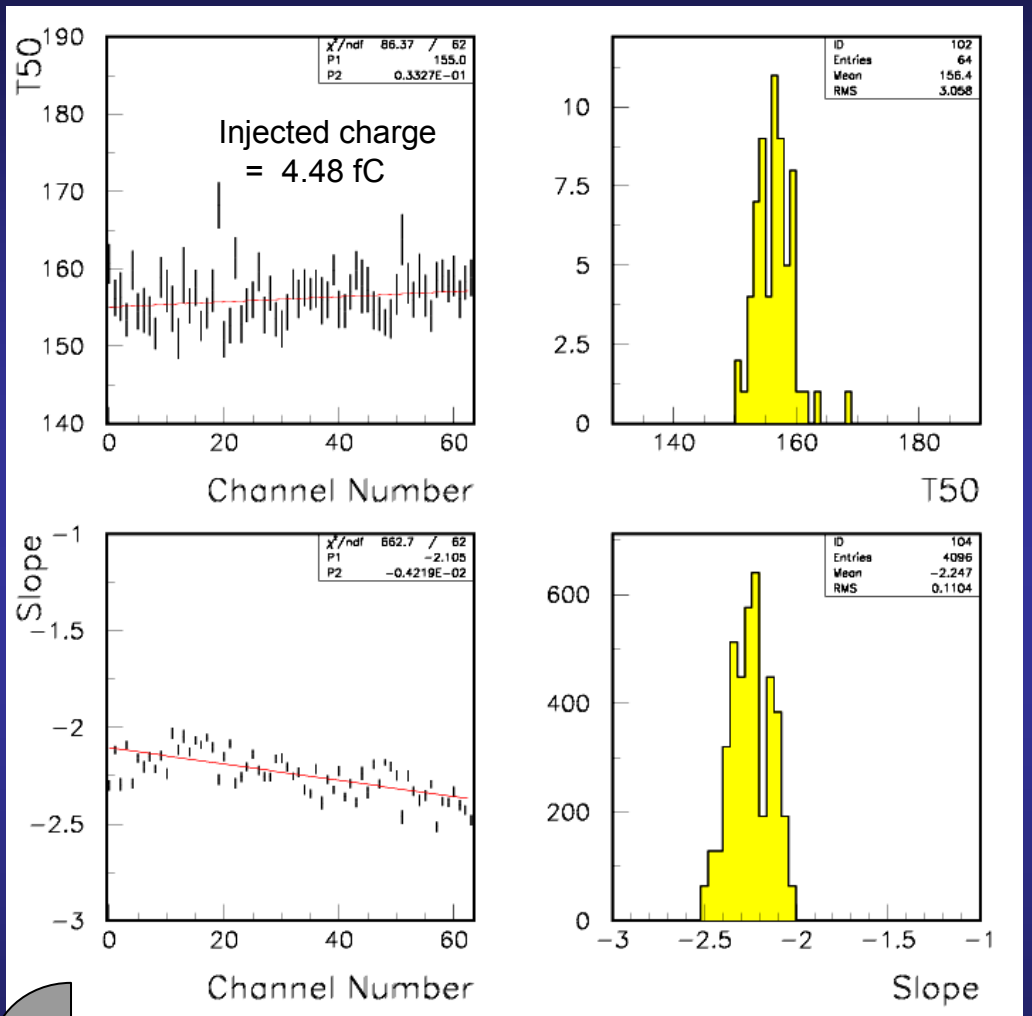
b) Detailed tests with injected charges so far look good

Threshold curve for Q = 2.83 fC



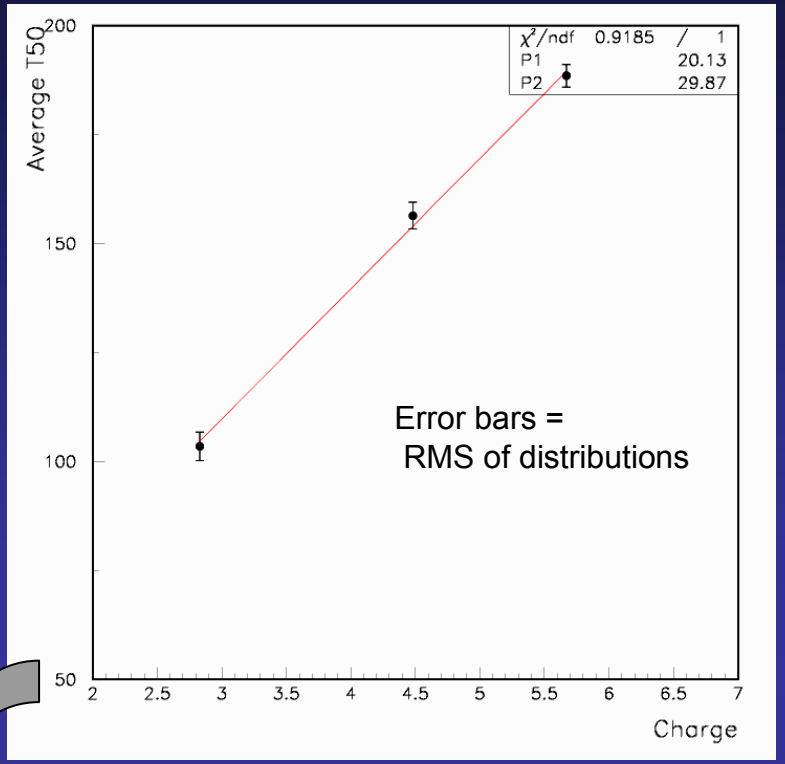
- Fit to straight line satisfactory
- Define T50 as threshold with 50% efficiency

Measurements across all channels in ASIC



- T50 values uniform across all 64 channels
- Overall small spread in T50 values
- Slope of threshold curves uniform across all channels
- Small spread in slopes

Results as function of input charge



Nice linear dependence!

2nd Iteration of ASIC Prototype

- Decrease of input sensitivity by x 10 – 20

  Currently upper threshold corresponds to 7.6 fC
  Smallest RPC signals ~ 100 fC
  Noise from digital lines ~ 11 fC (preliminary)

- Possibly decrease of serial line speed by x 10

  Currently 10 times faster than 10 MHz clock speed

- Other minor changes needed

- Submission on May 22nd

  Redesign will start in late March

Cooling…

Chip consumes about 300 mW (measured)

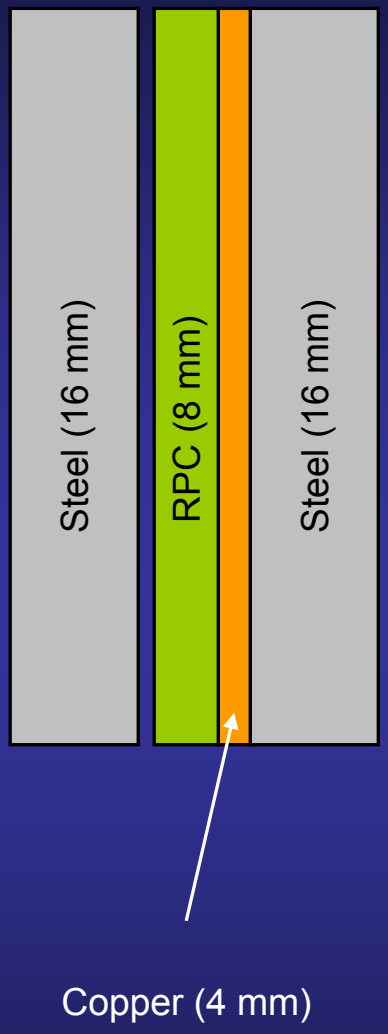
144 chips/plane → 50 W/plane

Thermal conductivity of steel not sufficient to dispose of heat

Copper x10 better thermal conductivity than steel

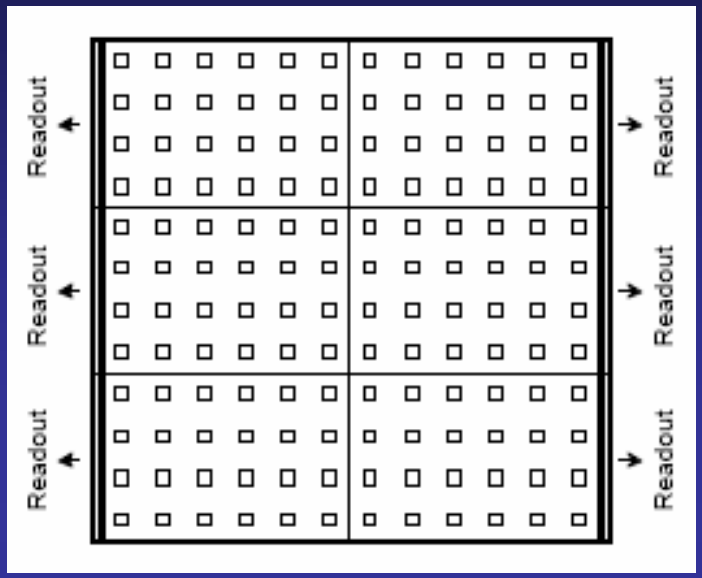
Consider replacing 4 mm support plates with copper plates

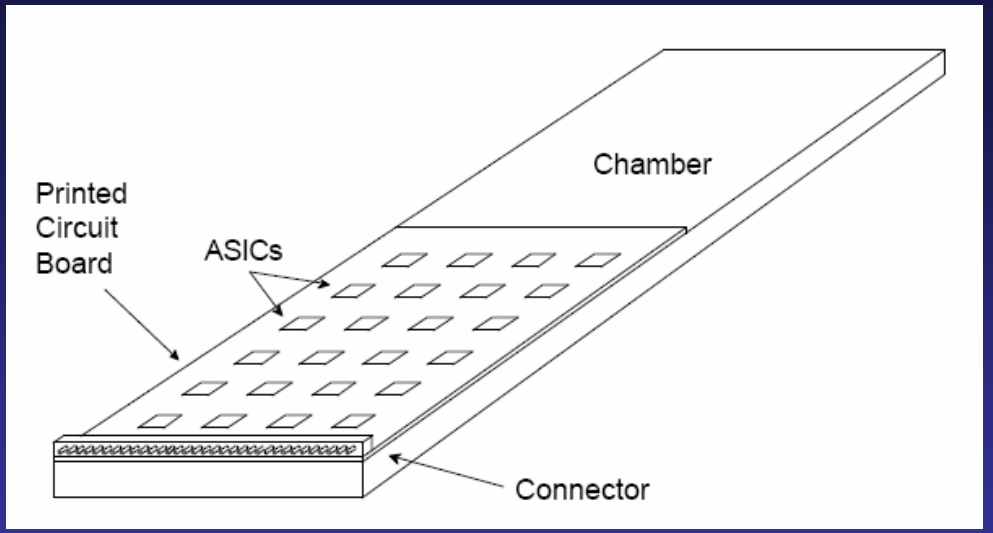
Cost OK
Magnetic properties not relevant for test beam
Properties for EM and HAD showers similar

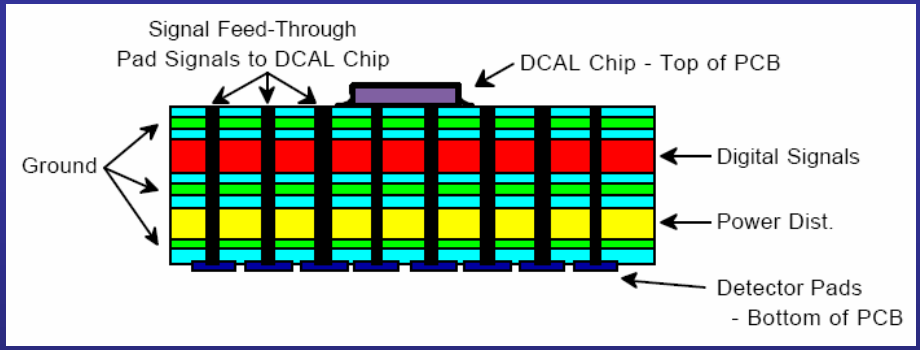


Material	A/Z	λ_I [cm]	X_0 [cm]	λ_I/X_0	$t_{passive} \equiv 4\lambda_I$ [cm]	Number of layers	t_{active}/ layer [mm]
Fe	56/26	16.8	1.8	9.3	67	38	8.7
Cu	64/29	15.1	1.4	10.8	42	60	9.5

Front-end boards…







2 boards/chamber or 6 boards/plane
8 layer boards
Overall thickness < 3 mm

Functionality

Houses ASICs (24)
Provides readout pads for RPCs
Routes signals to ASICs
Distributes power and ground to ASICs
Distributes clocks and control signals to ASCIs
Routes output signals (LVDS) to receivers

} Analog signals

} Slow control

} Digital signals

Design challenge

Digital → analog crosstalk…

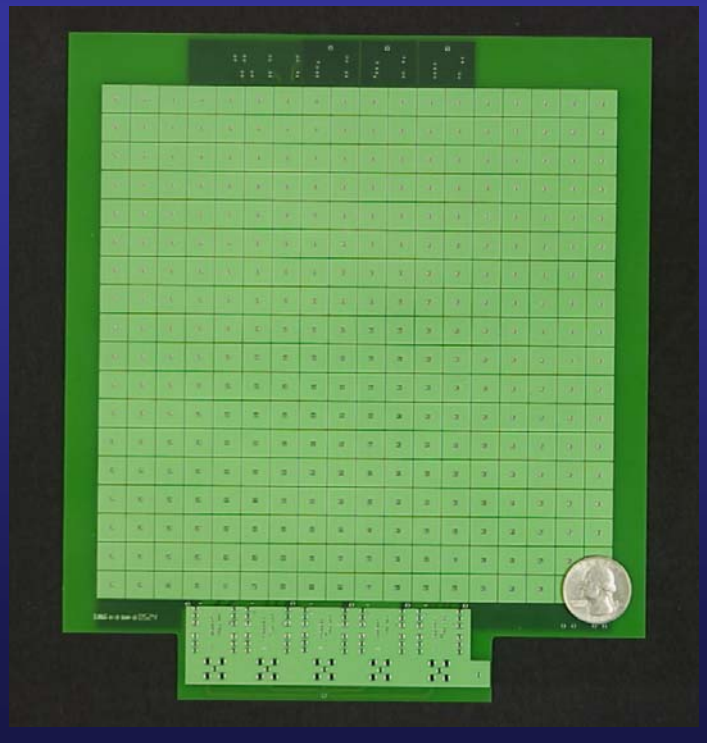
Measurements with test board

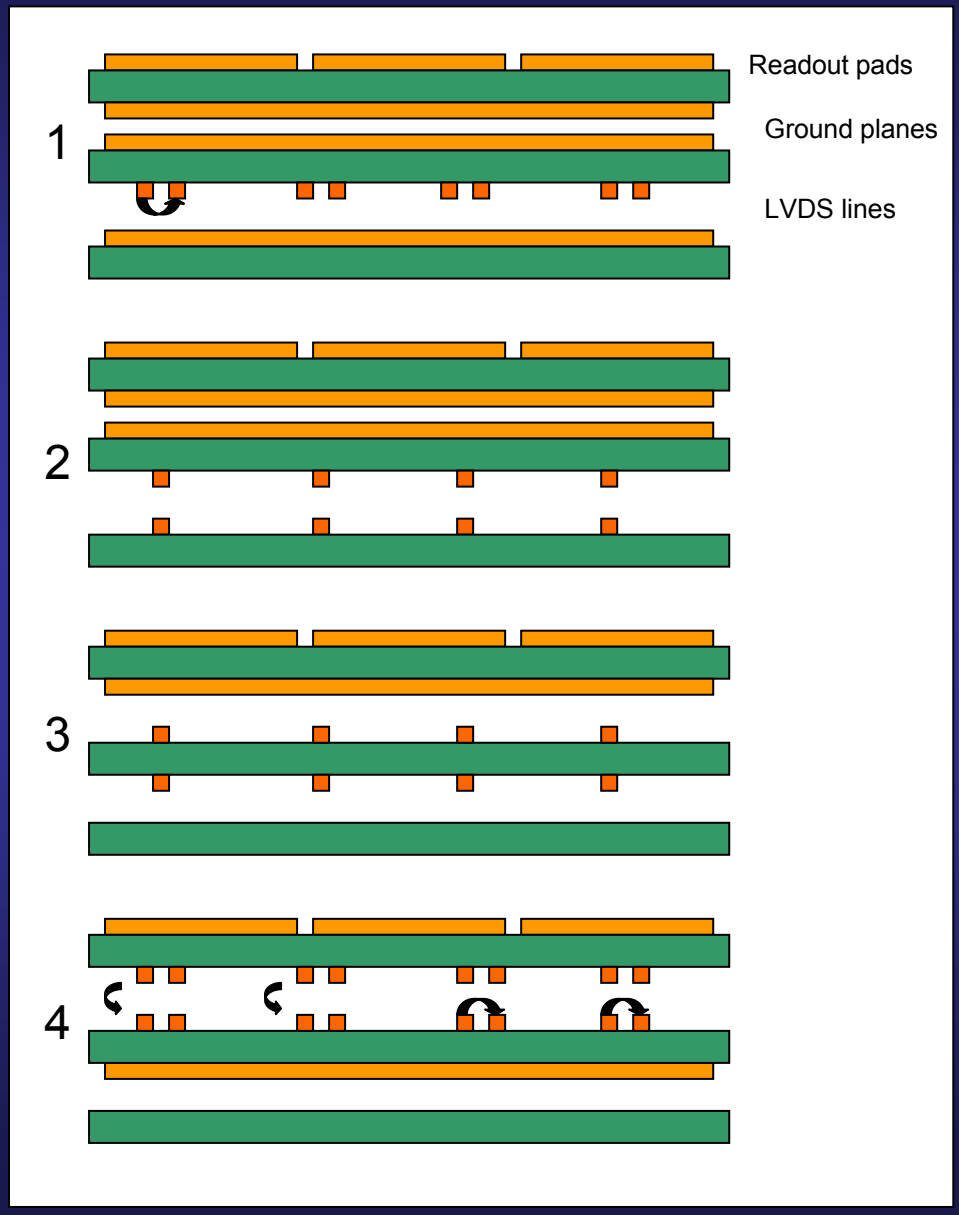
LVDS signals routed close to pads

4 different configurations

Each with 4 different distances to the center of the pads

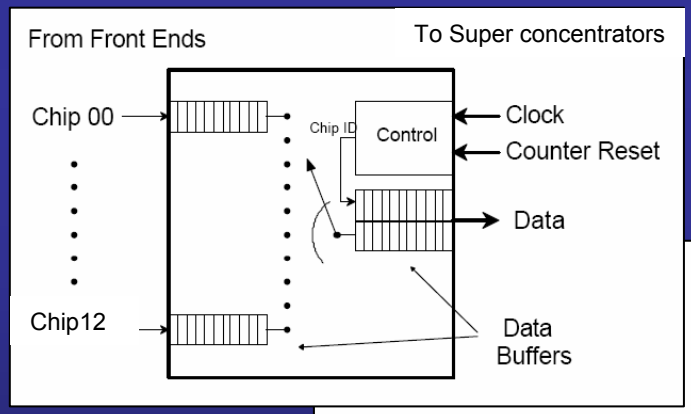
First indicate cross-talk of ~11 fC, but more tests needed…

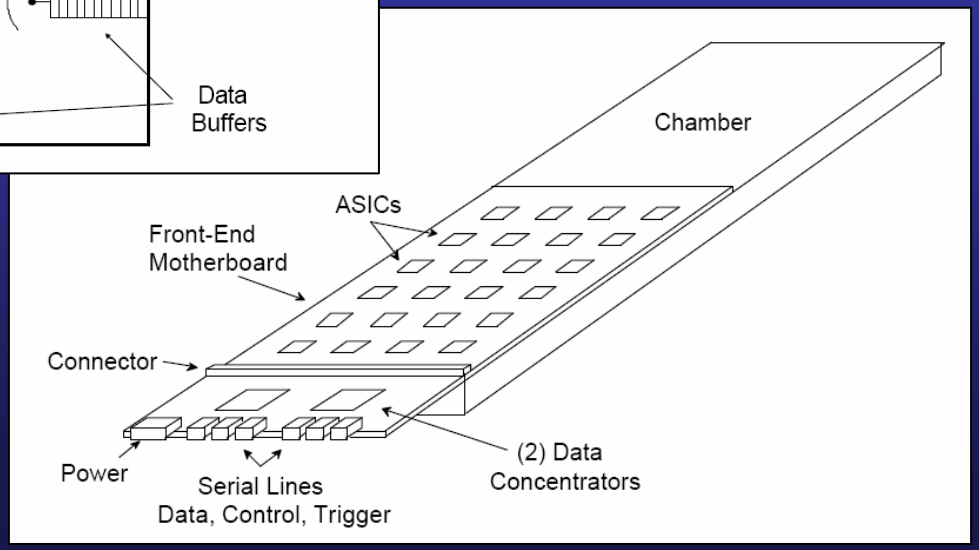


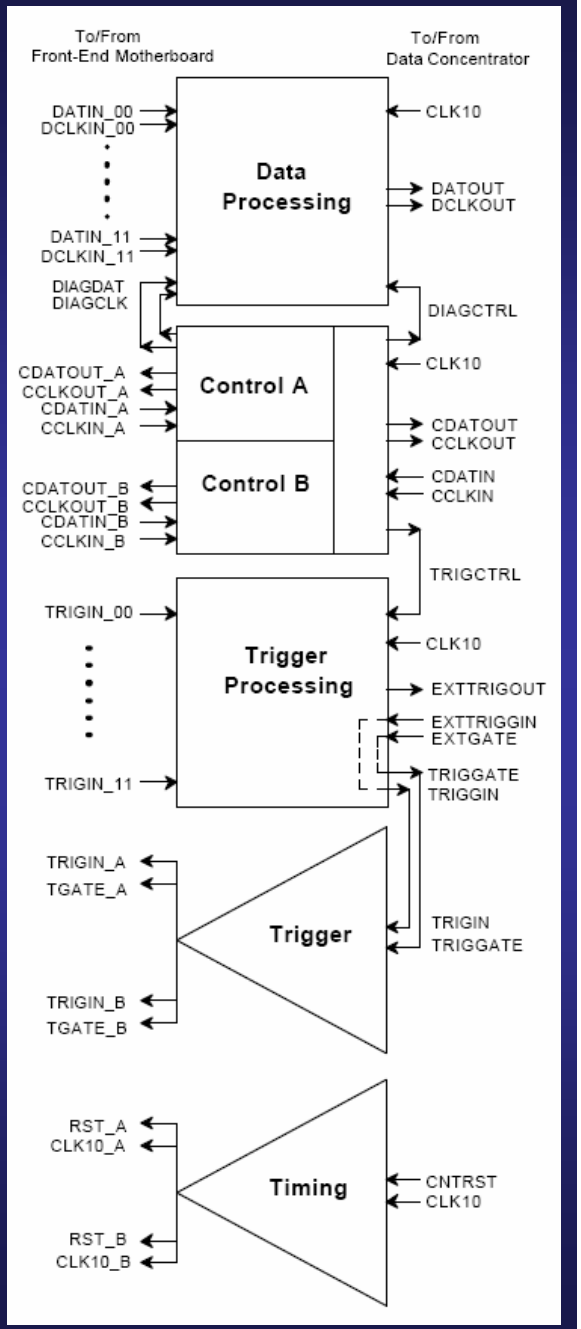


Data concentrators…

Read out 12 ASICs (serial lines)
Located on sides of section
Can buffer events
Distribution of trigger and timing
(bus connection)
Essentially FPGAs
All transmissions in LVDS







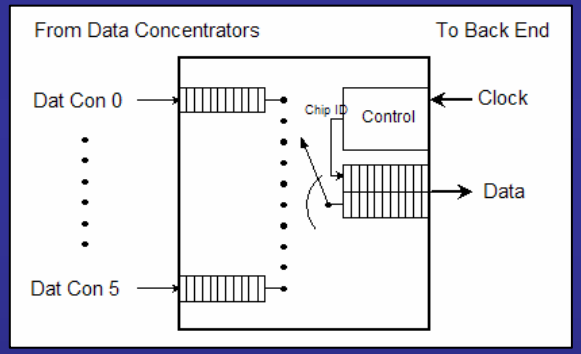
Super concentrators…

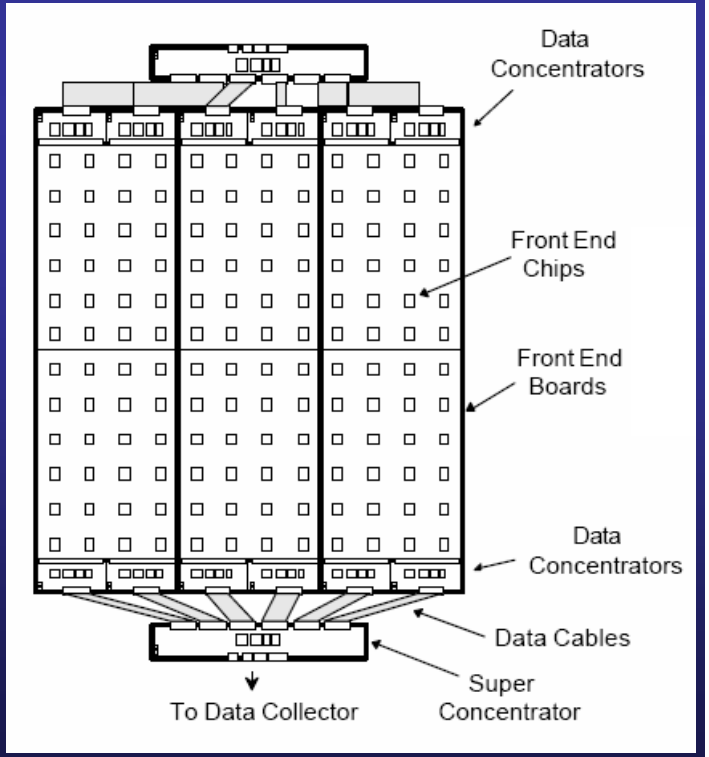
Introduced by urge to reduce cost of back-end

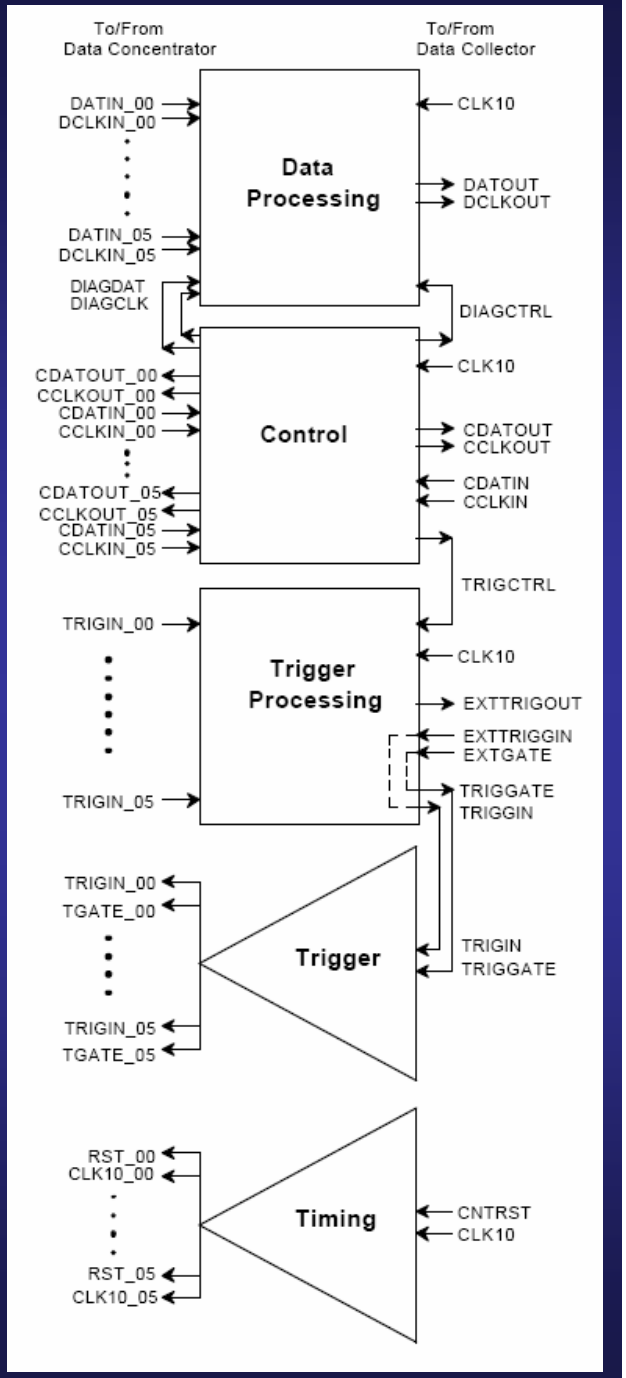
Reads out 6 data concentrators

Located on side of module

Similar design to data concentrator





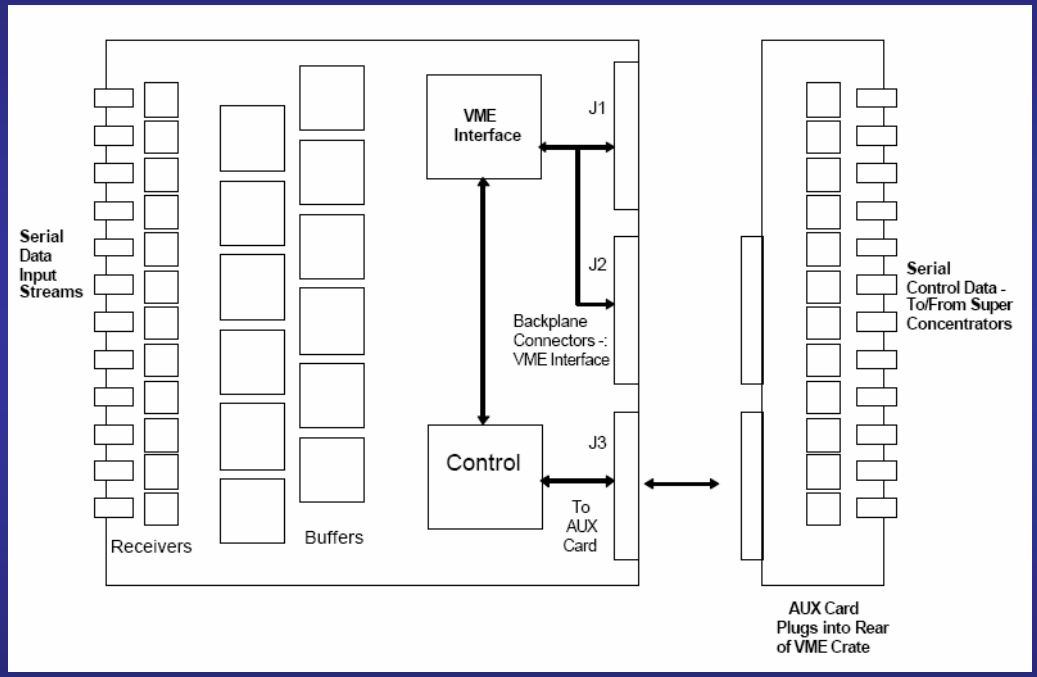


Data collector…

VME based system

Each card reads out 12 super concentrators

Need only 7 cards and 1 VME crate



Investigating possibility of using
CALICE-AHCAL back-end
or
Fermilab's test beam
DAQ system

Work by Lei Xia

Study of rates…

Simulation of response of 1 m^3 prototype section to 50 GeV π^+

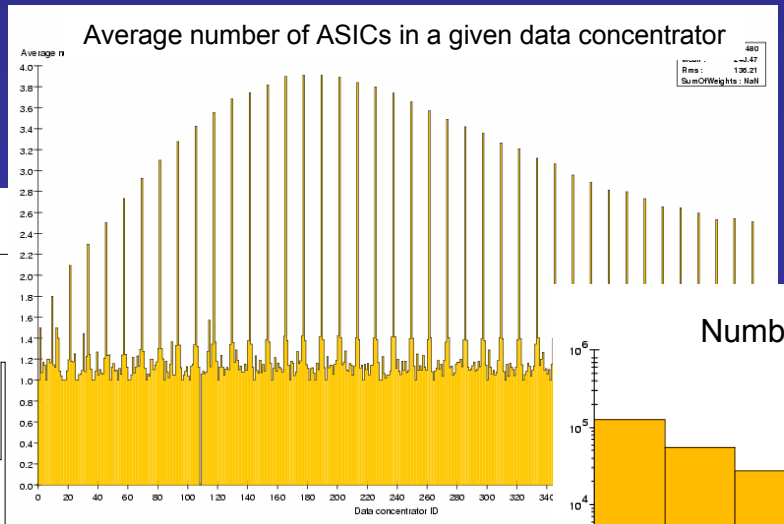
Study of data rates in different components of the readout system

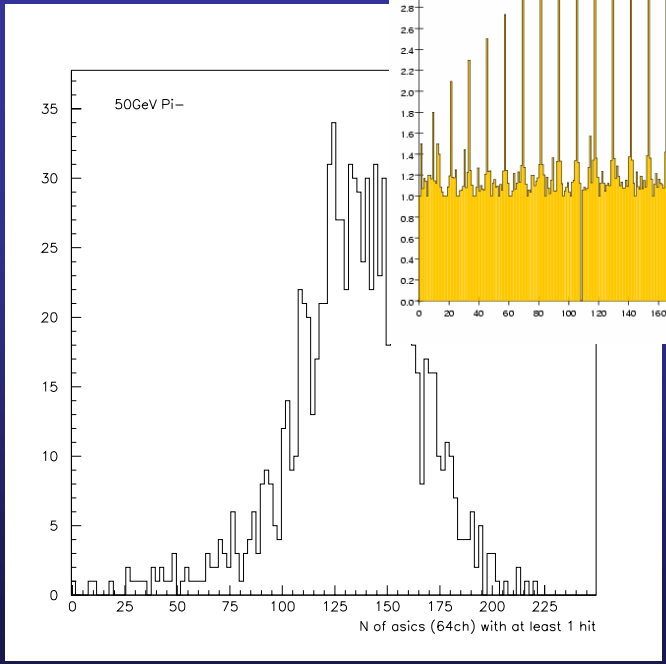
System capable of handling ~10x more data than expected

Examples…

Readout speed 10 Mb/sec

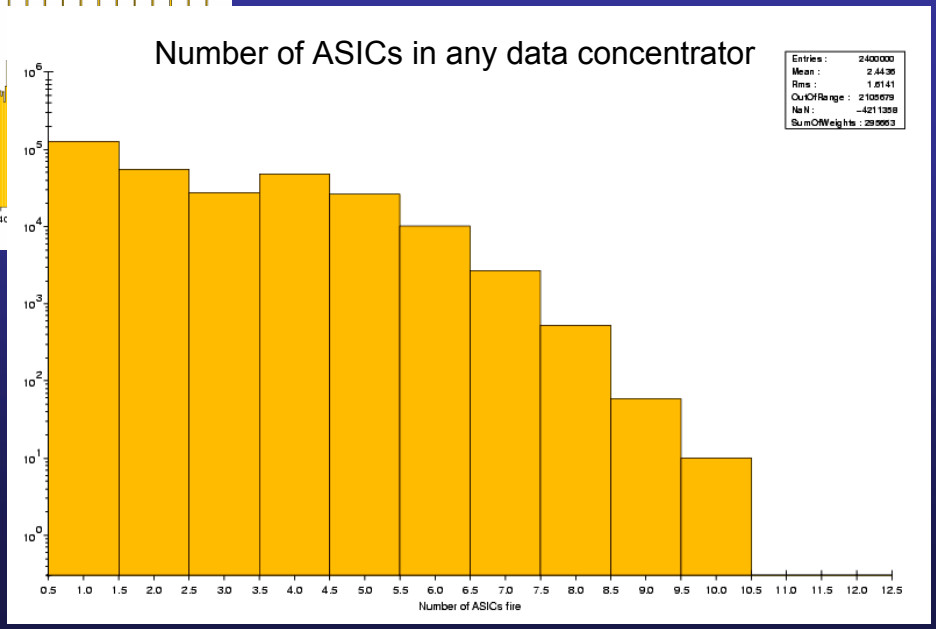
Average number of ASICs in a given data concentrator





Number of ASICs in a given event

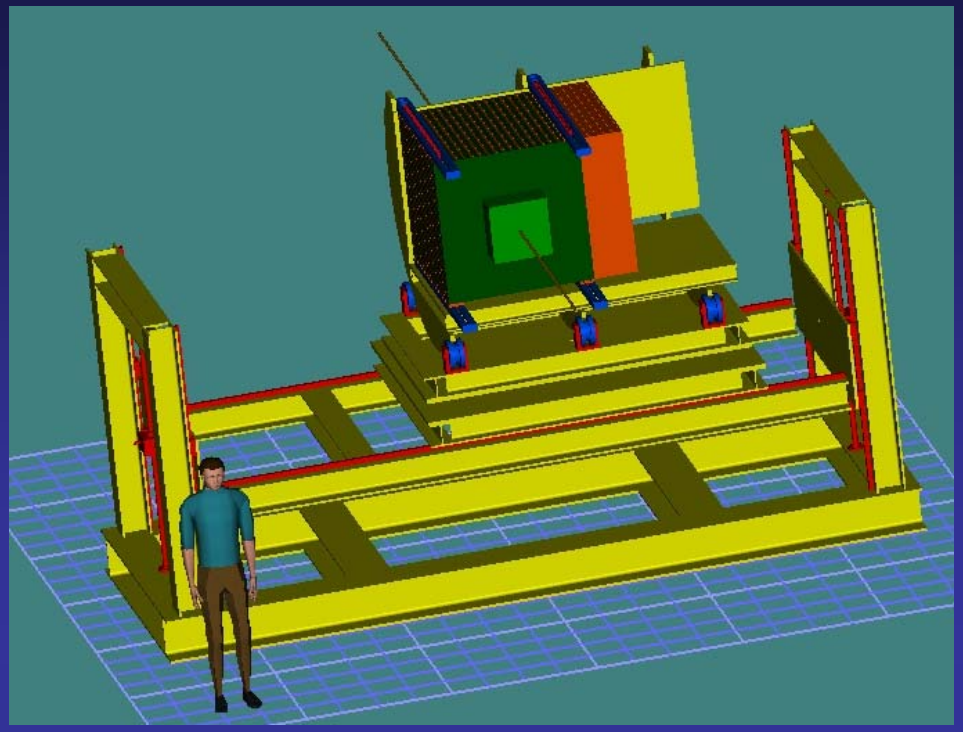
Number of ASICs in any data concentrator



List of subtasks

1	Overall engineering and design	**ANL**
2	ASIC engineering and design	**FNAL**
3	ASIC testing Test board design Test board production Measurements	ANL **FNAL**
4	Front-end PC board engineering and design prototyping and testing	**ANL** **FNAL**
5	Data concentrator engineering and design prototyping and testing	ANL Chicago
6	Data super concentrator engineering and design prototyping and testing	ANL Chicago
7	Data collector engineering and design prototyping and testing	ANL Boston
8	DAQ system: VME processor and programming	**Washington**
9	Timing and trigger system engineering and design prototyping and testing	**UTA**
10	High voltage system	**Iowa**
11	Gas mixing and distribution system	**Iowa**
12	Chamber construction	ANL Regina Russia

Mechanical Structure for PS



CALICE builds versatile structure

Absorber 20 mm **Steel** → 1 X_0 sampling
40 layers → 4 λ_I at 90^0

Recent simulation studies indicate that Tungsten with

Thickness of 0.7 cm → 2 X_0 sampling
58 layers → 4 λ_I at 90^0

might result in better PFA performance and safe on cost (coil)

Questions

a) Do we need to test a Tungsten prototype?
b) If yes, can we re-use the CALICE structure?
c) What is the optimum sampling depth for W?

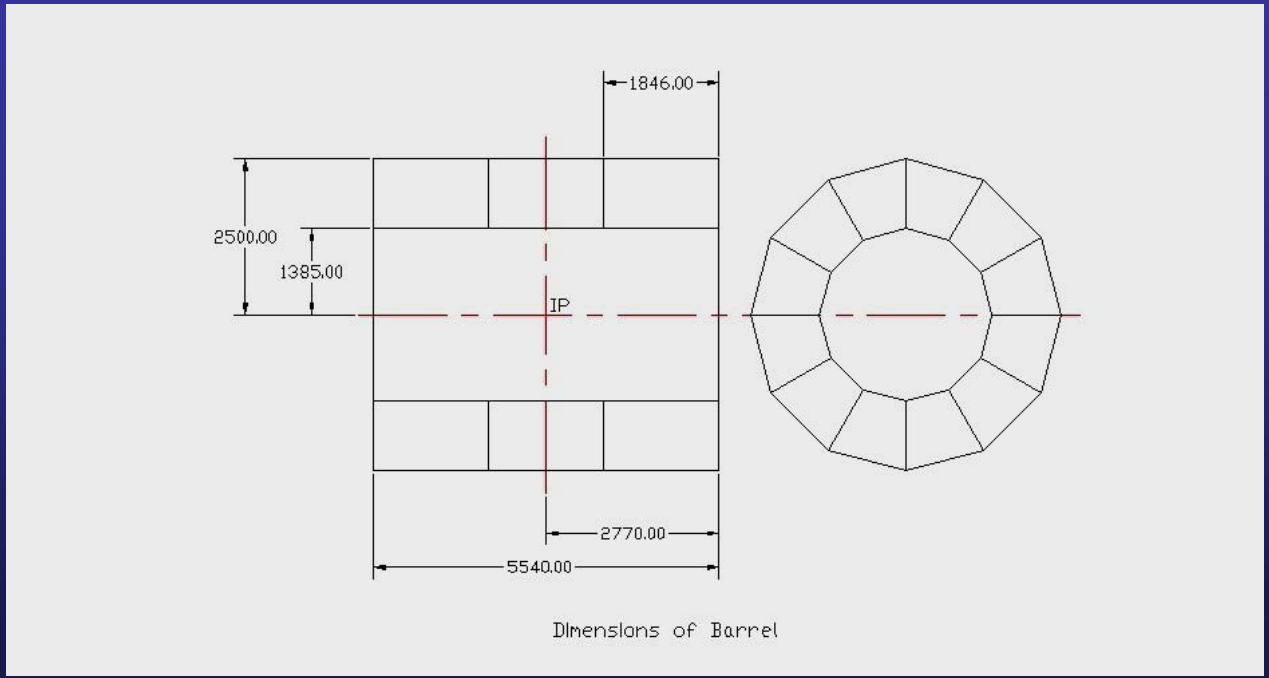
Mechanical Structure for ILC Detector

Initiated study in context of SiD concept

3 barrels in z

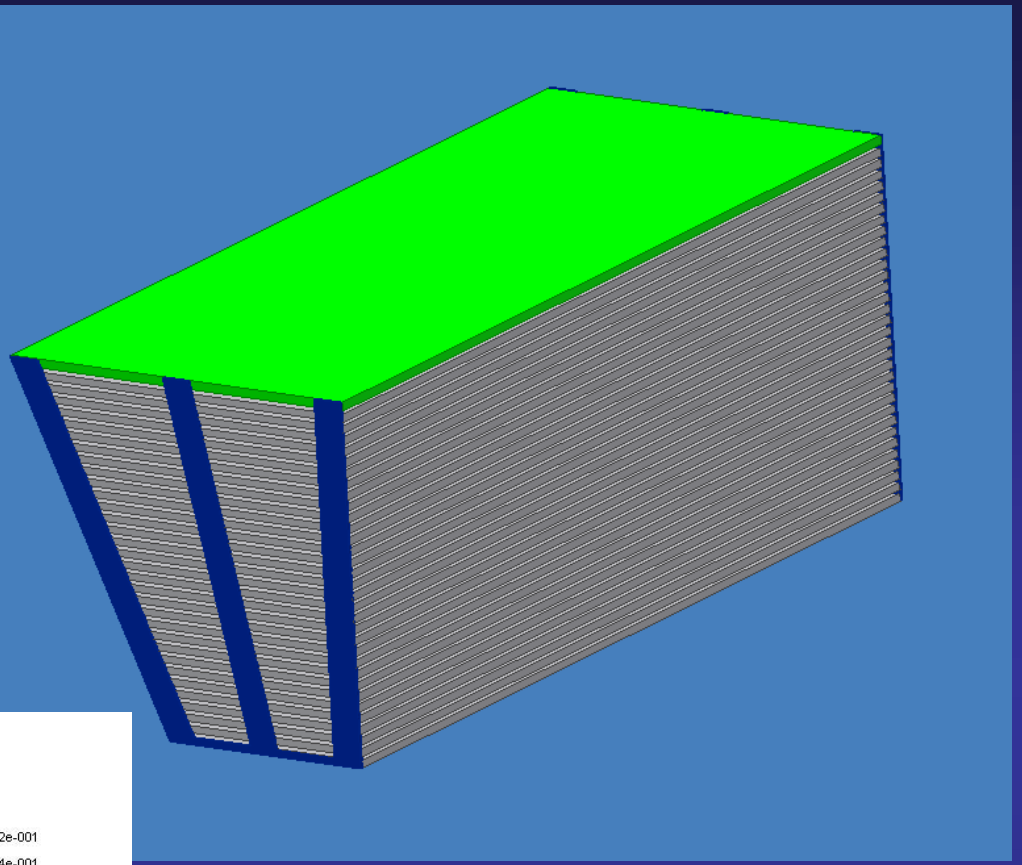
- to provide space for readout cables, gas supplies…
- to minimize deflections along z and for modules in 90^0 position

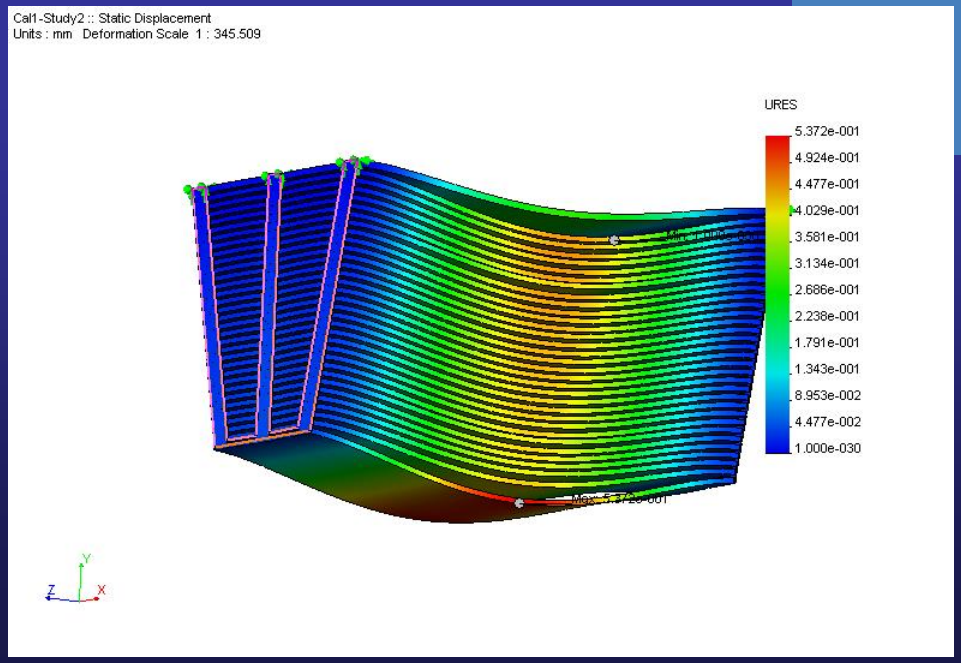
12 modules in φ



Plates held in place by
'picture frames'
↓
space for routing cables…

Gap between active areas
approximately 2 cm



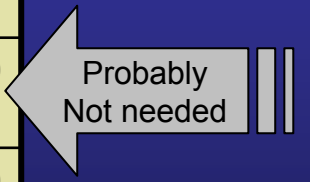


Deflections everywhere
smaller than 0.53 mm

(If considering single barrel with
supports only at the ends,
largest deflection 44 mm)

Cost estimate for PS (M&S only)

Item	Cost	Contingency	Total
RPC chambers	20,000	7,000	27,000
FE-ASICs	208,000	11,600	219,600
FE-boards	110,000	55,000	165,000
Data concentrators	106,000	53,000	159,000
Super concentrators	25,000	12,500	37,500
Data collectors including crates…	51,500	19,250	70,750
HV and LV supplies, gas system, cables…	132,500	45,750	178,250
Total	**653,000 + 204,100 = 857,100**		



Recent Proposals to Funding Agencies…

Agency	Institutes	Request	Award
LDRD (ANL directorate) used for manpower mostly	ANL	400,000	150,000
LCRD (DOE)	ANL, Boston, Chicago, Iowa	105,000	?
U of C Collaborative Grants	ANL, Chicago	50,000	?
US-Japan	ANL	50,000	0
MRI DHCAL prototypes	UTA	798,000	?

Time scales

FY2006	Develop and test design of larger chambers
	ASICs: finalize design for production
	Design and prototype all subsystems
FY2007	Perform slice test of prototype section
	Produce chambers
	Produce ASICs
	Produce other subsystems
FY2007 or FY2008	Move to test beam
	Take data

This part
Is funded

Only possible with additional funding