

# An ECAL for the SiD detector

## Topics:

- Motivation and Concept
- Silicon Sensors
- Mechanical Design
- Electronics
- Sensor Tests

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**Mechanical  
Design**

**Electronics**

**Bump Bonding**  
Mechanical Design  
**Cabling**

**Electronics**  
Mechanical Design  
Simulation

**Si Detectors**  
Mechanical Design  
**Simulation**

## Design Requirements

*Optimal contribution to the reconstruction of multijet events:*

- Excellent separation of photons from charged particles
- *Efficiency*  $> 95\%$  for energy flow
- Excellent linkage of ECAL with tracker (important for SiD)
- Good linkage of ECAL with HCAL
- Good reconstruction of  $\pi^\pm$ , detection of neutral hadrons
- Reasonable EM energy resolution,  $\sim 15\%/\sqrt{E}$

Physics case:

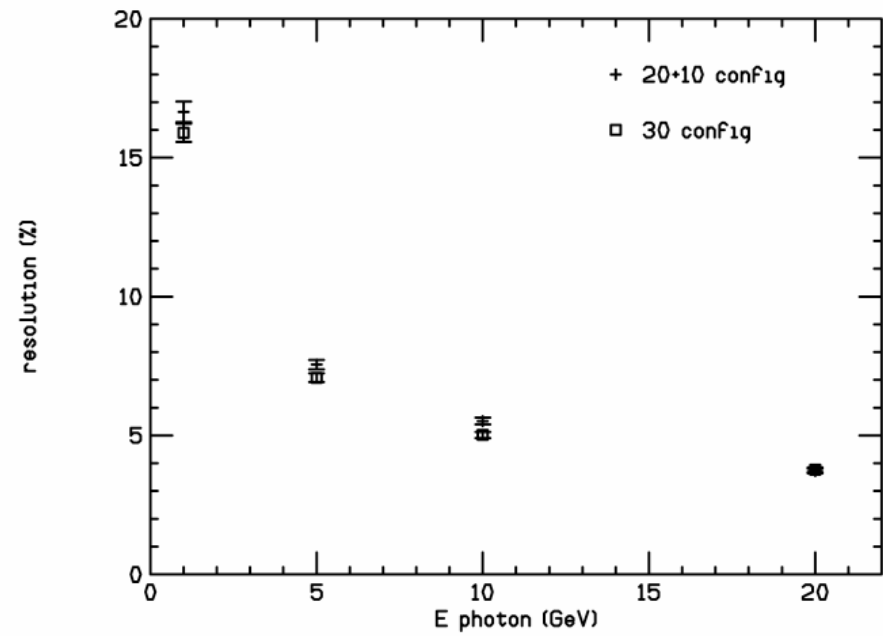
*Jet reconstruction important for many physics processes.*

## Longitudinal Sampling

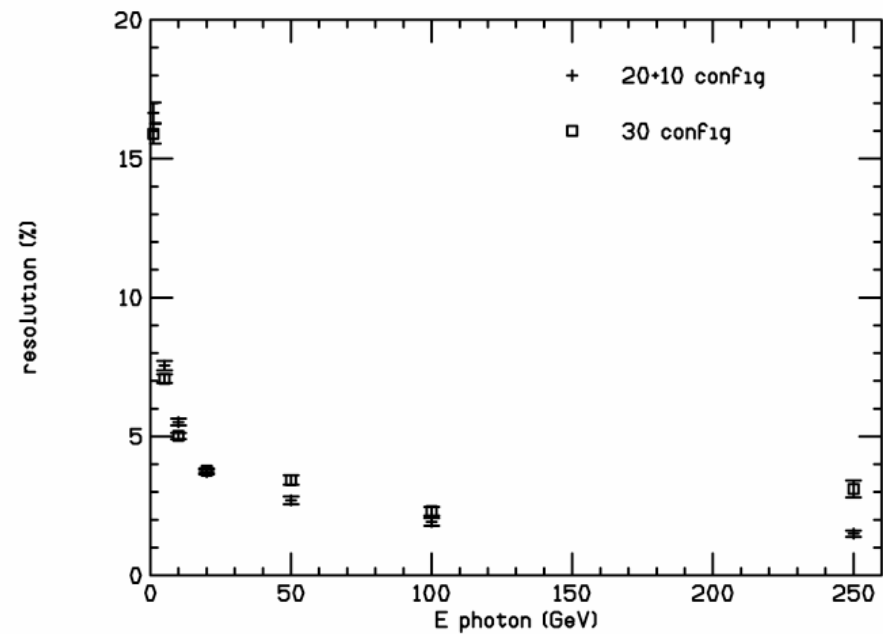
- Energy resolution is  $\sim 20\%/\sqrt{x/E}$  where  $x$  is the sampling fraction in  $X_0$  (if HE showers contained)
- Implies we need approximately  $\sim 30 X_0$  for highest  $E$
- Energy flow is not critically dependent on ECAL energy resolution
- Consider designs with fine sampling in front and coarser sampling in back

Possible Scheme	20 layer $0.71 X_0$ (2.5mm)
	10 layer $1.42 X_0$ (5.0mm)

Resolution for 1-20 GeV  
photon energy comparable  
for two configurations

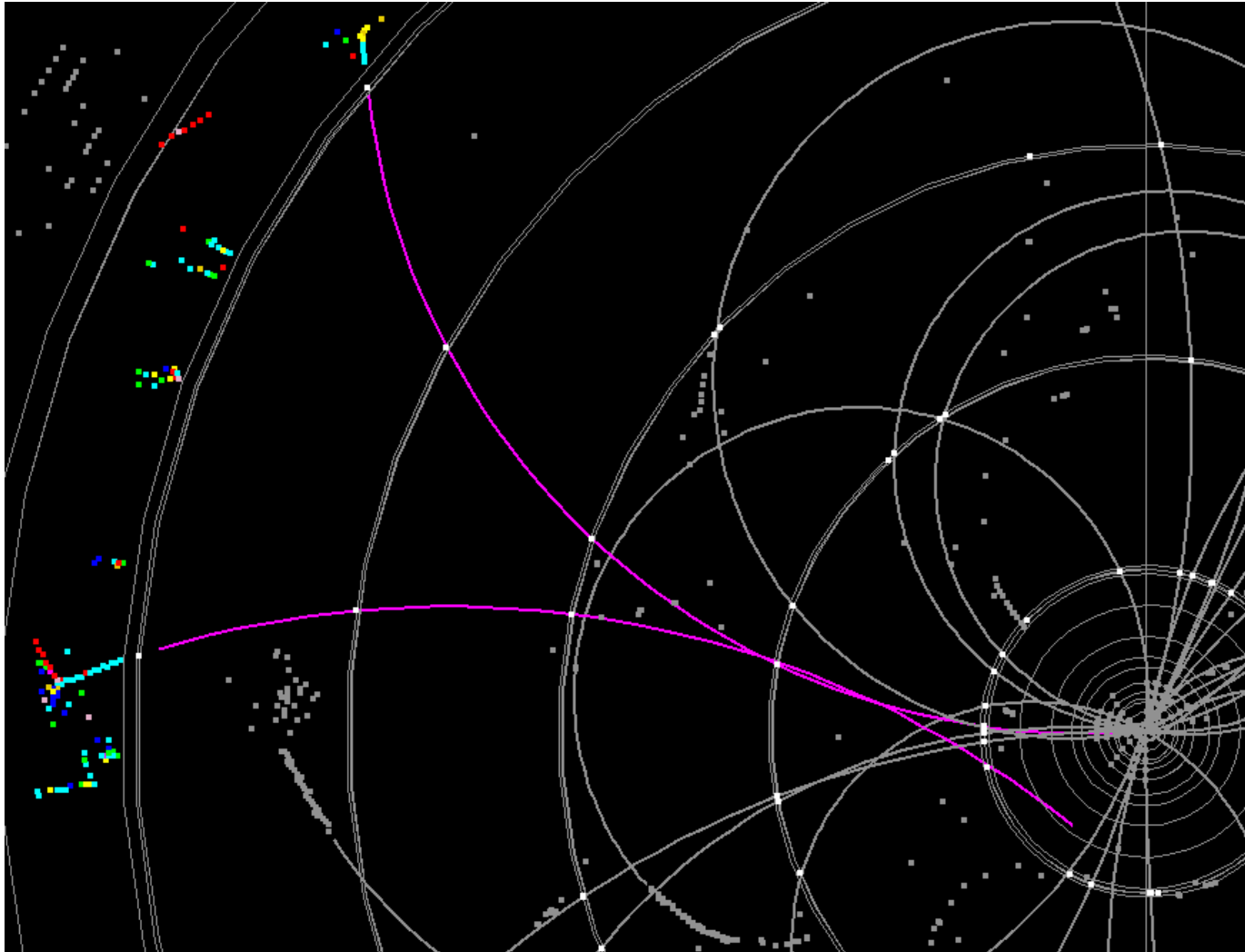


Resolution at the highest  
energies is considerably  
better for 20 + 10  
configuration (leakage)



*NB results are for ecal only, assume pure W*

Large number of samples useful for tracking, 100% efficiency not required:



K0s tracking from von Toerne

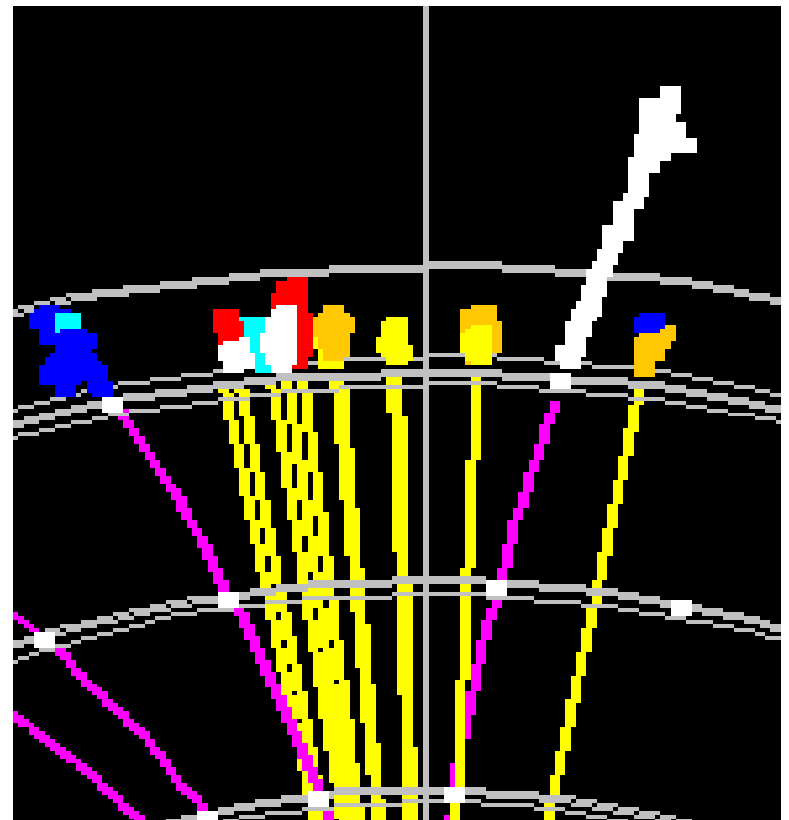
LEP granularity, difficult to resolve individual photons

*Can't benefit from cluster-centroid track matching*

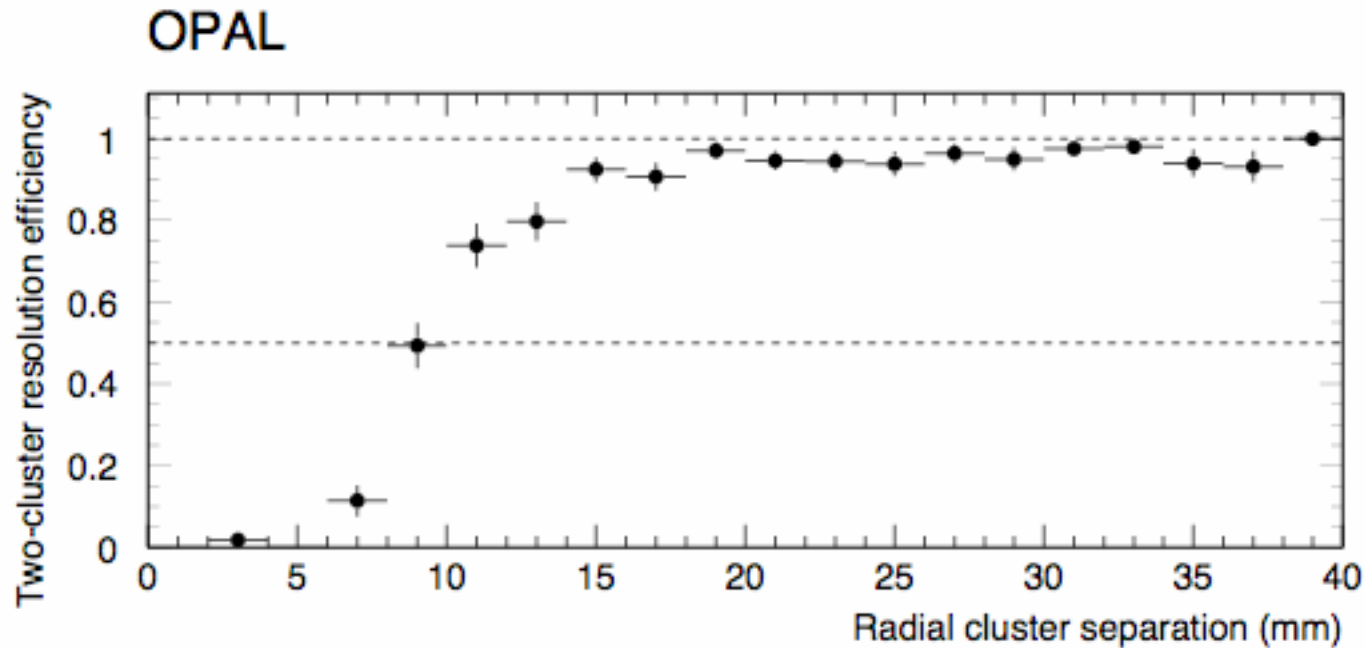


ILC granularity must be sufficient to resolve photons

*Can benefit from cluster-centroid track matching*



Example: OPAL SiW luminosity monitor  
( $1X_0$  radiator, 3mm gap, 2.5mm pads,  $R_M \sim 17\text{mm}$ )



Cluster can be resolved when separated by 9mm,  
corresponding  $\sim 0.5 R_M$ .

Must be able to resolve photons to successfully match tracks and clusters, suggested figure of merit for energy flow  $f_E$ :

$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

Here,  $R_{cal}$  is the radius of the calorimeter,  $R_M$  is the Moliere radius and  $d_{pad}$  is the pad size.

We can resolve clusters to  $0.5 R_M$  if pads are  $0.25 R_M$

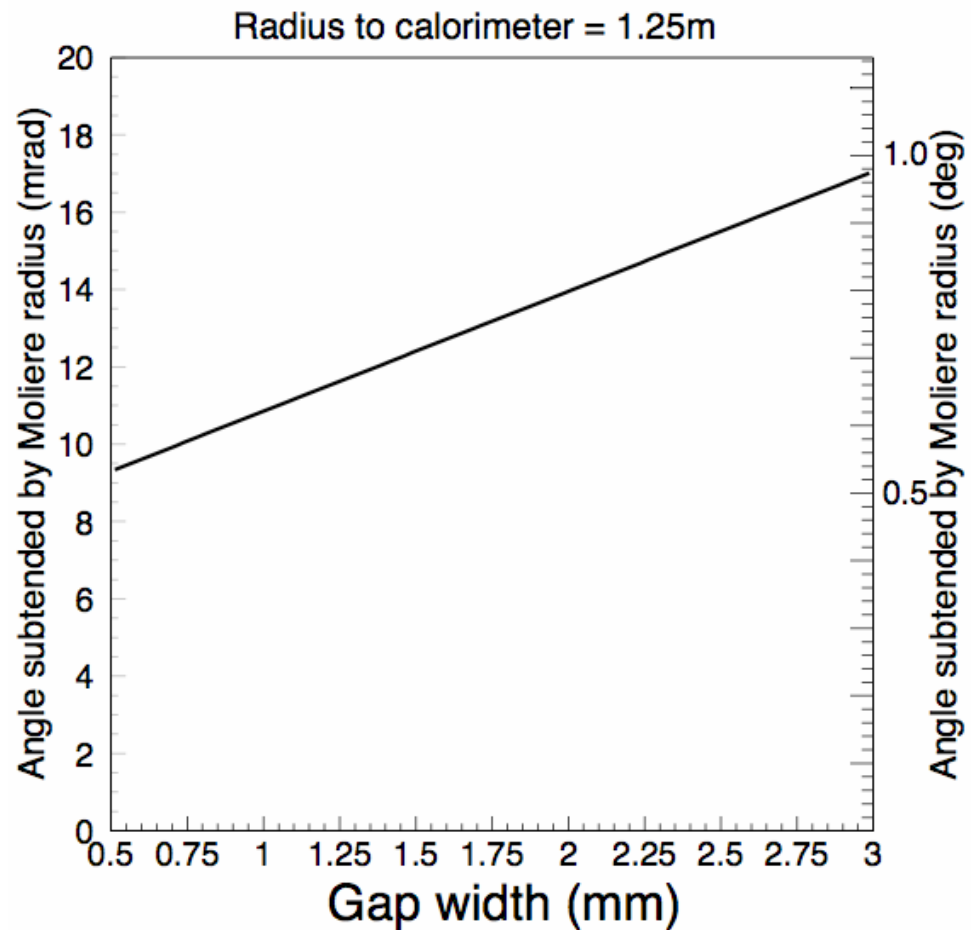
Increasing  $R_{cal}$  increases the cost of the whole detector  
 $\Rightarrow$  concentrate on  $d_{pad}$  and  $R_M$



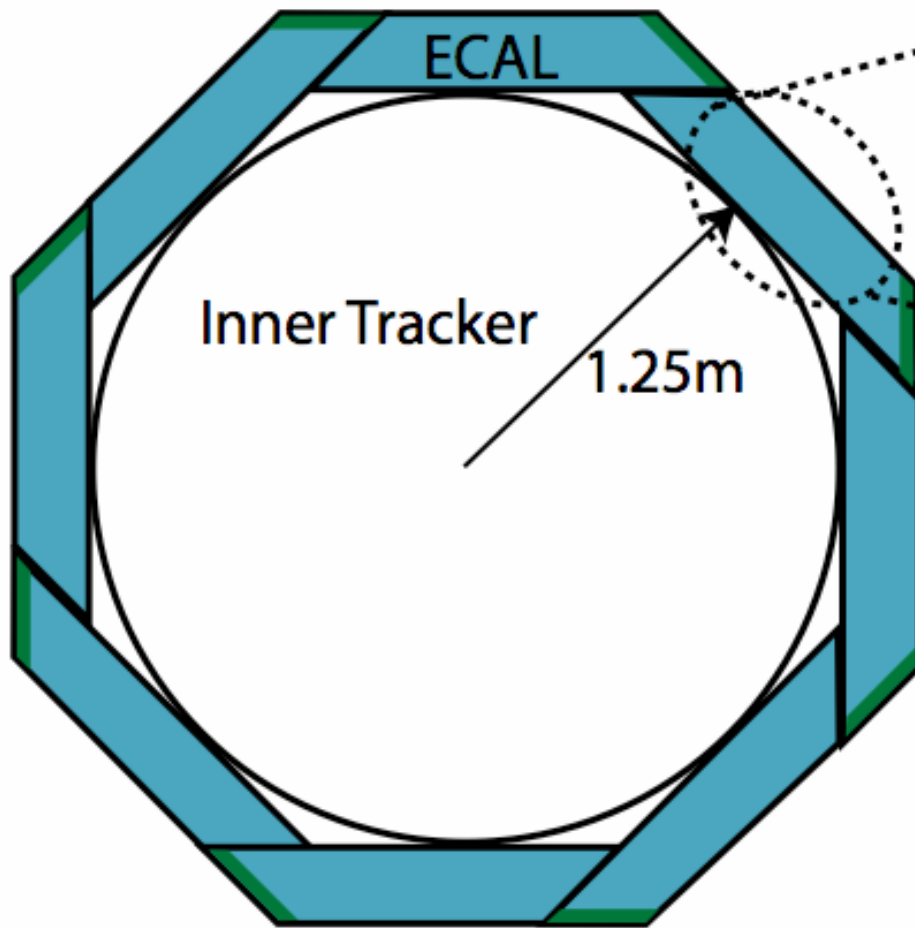
Critical parameter for is  $R_M$  the gap between layers

Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm

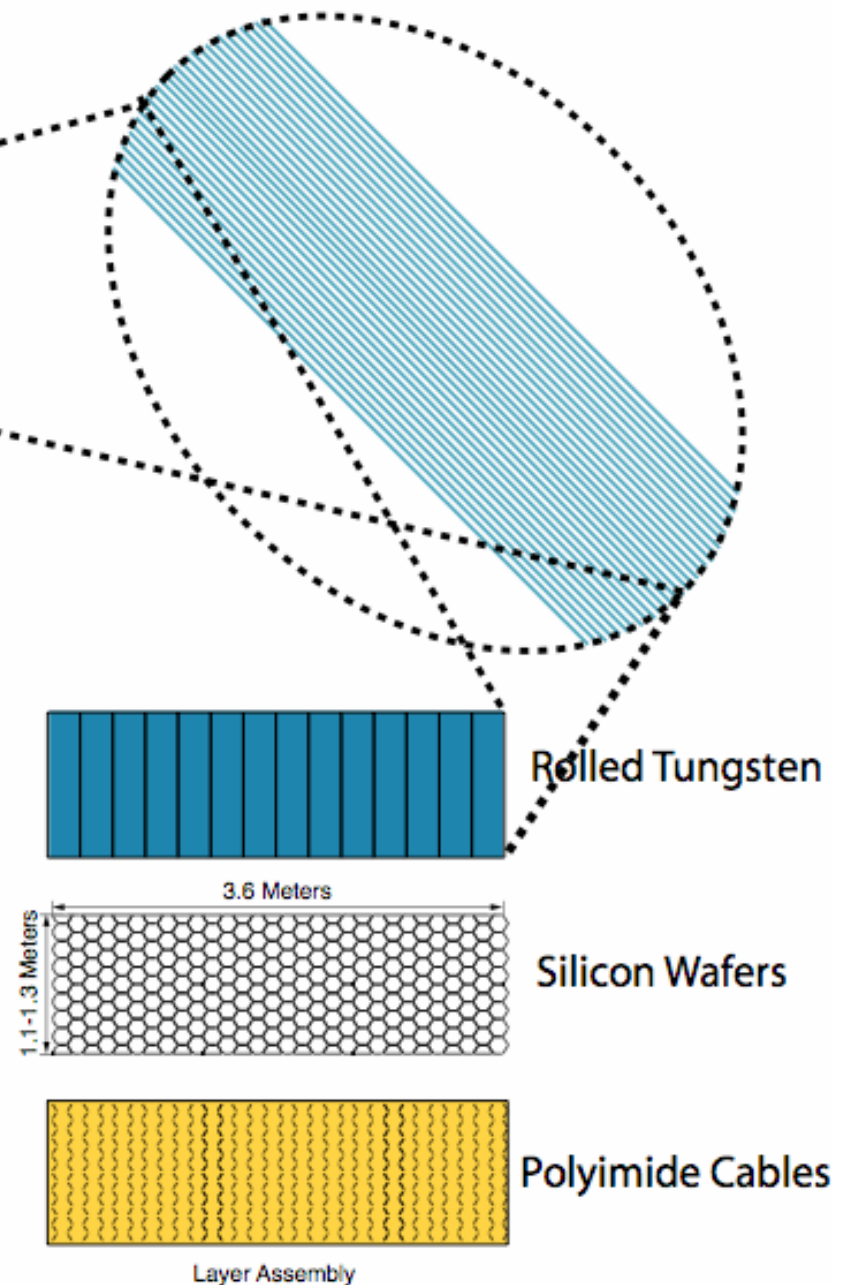
Assumes 2.5mm thick tungsten absorber plates



# Si-W Calorimeter Concept

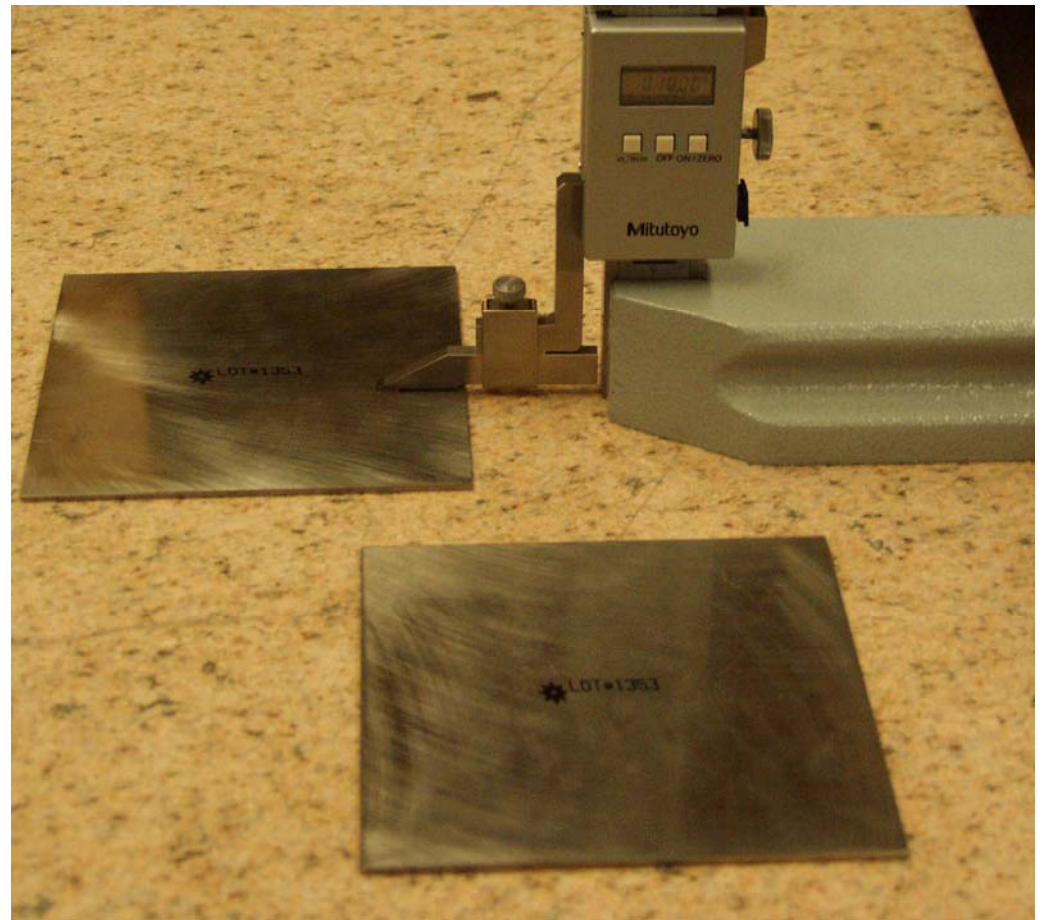


Transverse Segmentation  $\sim 5\text{mm}$   
30 Longitudinal Samples  
Energy Resolution  $\sim 15\%/E^{1/2}$



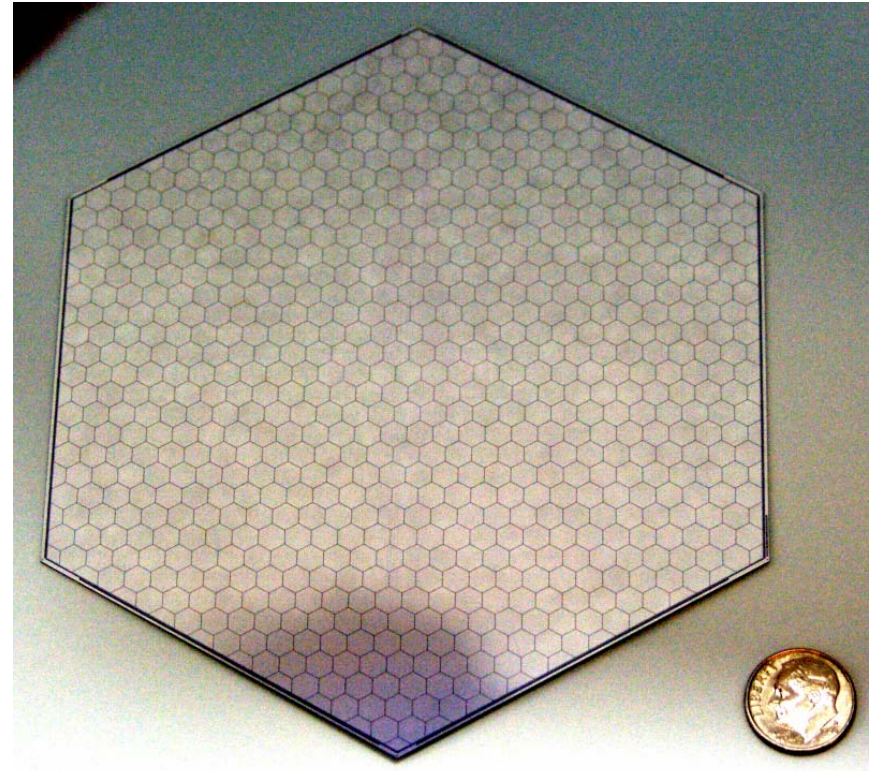
# Tungsten Absorber

- Excellent Tungsten vendor located
- Test beam tungsten in hand (10cm x 10cm)
- Vendor can roll plates as large as 10cm x 100cm
- Tolerances look okay



# Silicon Sensors

- Silicon is likely to be the main cost driver
- Use a hexagonal shape to use as much of the silicon wafer as possible
- Silicon sensors can be segmented very finely
- Limit on granularity given by electronics power, second order costs from electronics



# Detector Segmentation

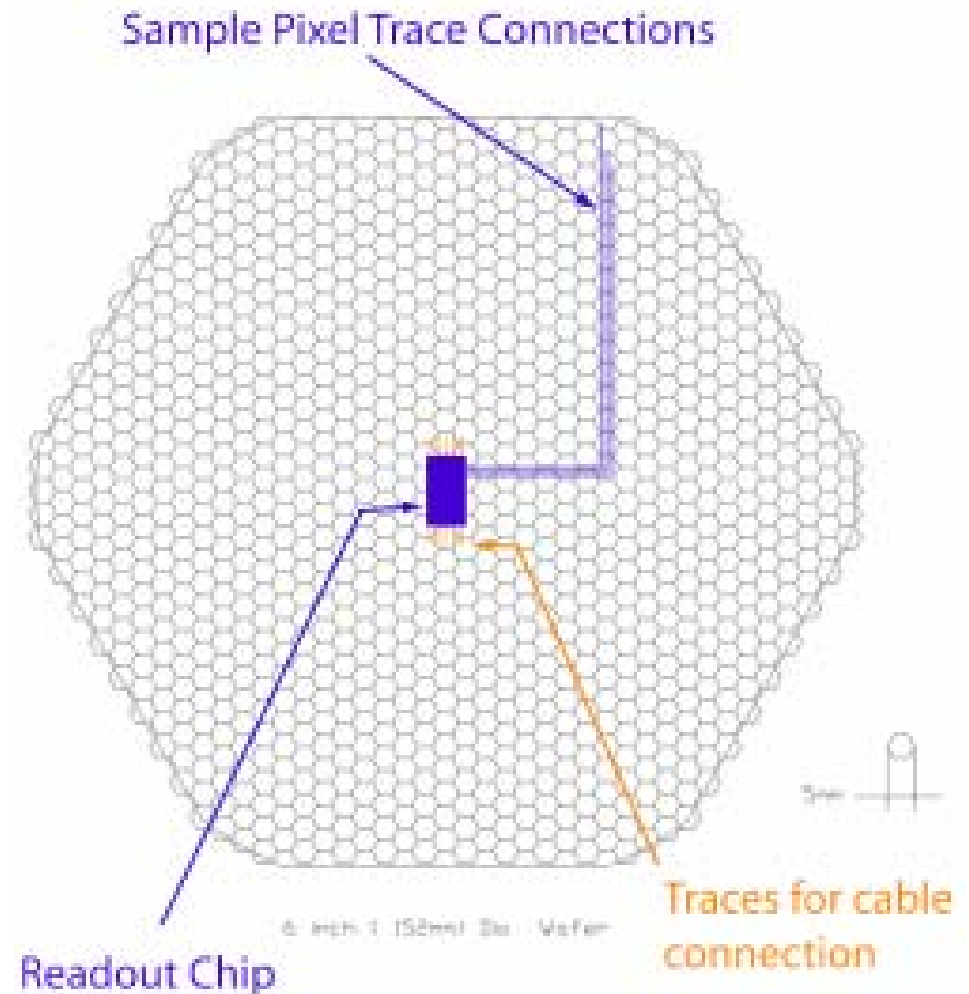
Readout each wafer with a single chip

Bump bond chip (KPiX) to wafer

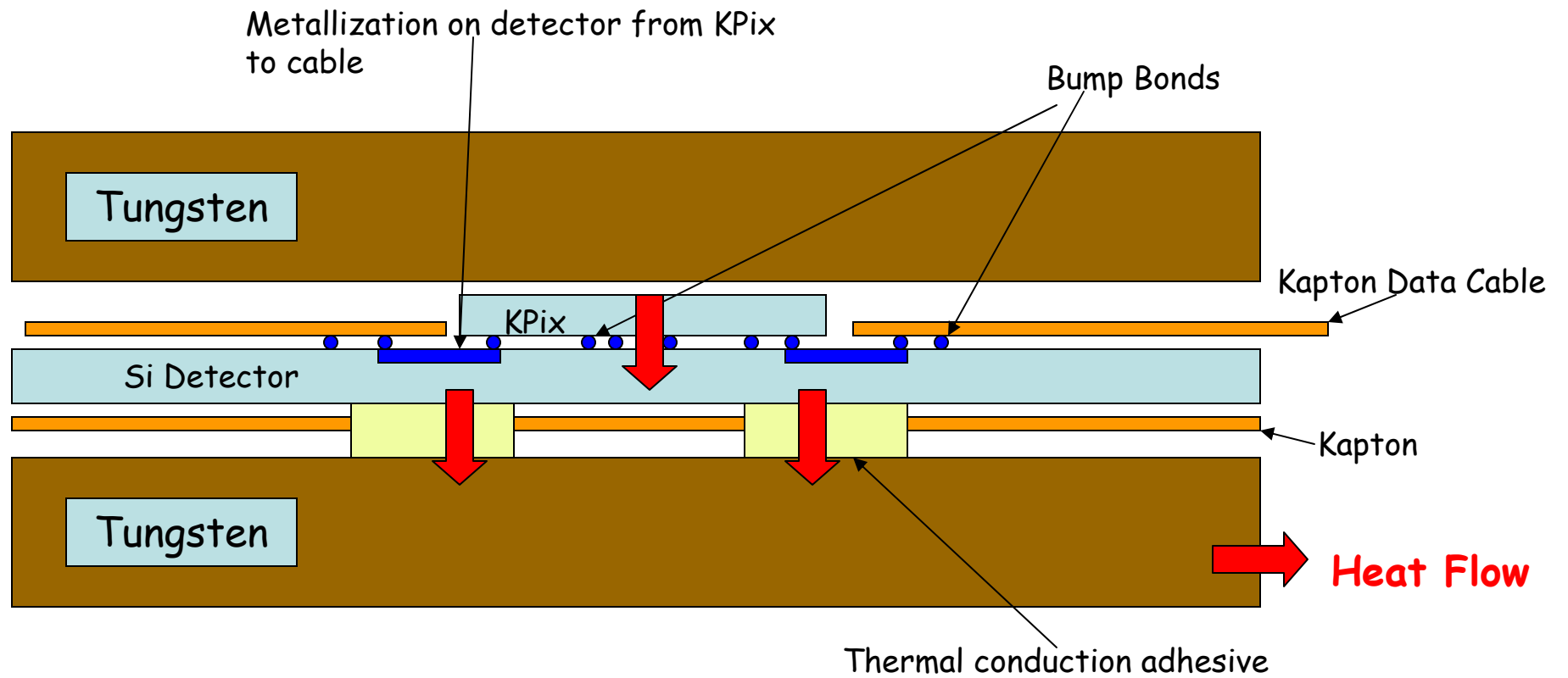
To first order cost independent of pixels /wafer

Hexagonal shape makes optimal use of Si wafer

Channel count limited by power consumption and area of readout end chip

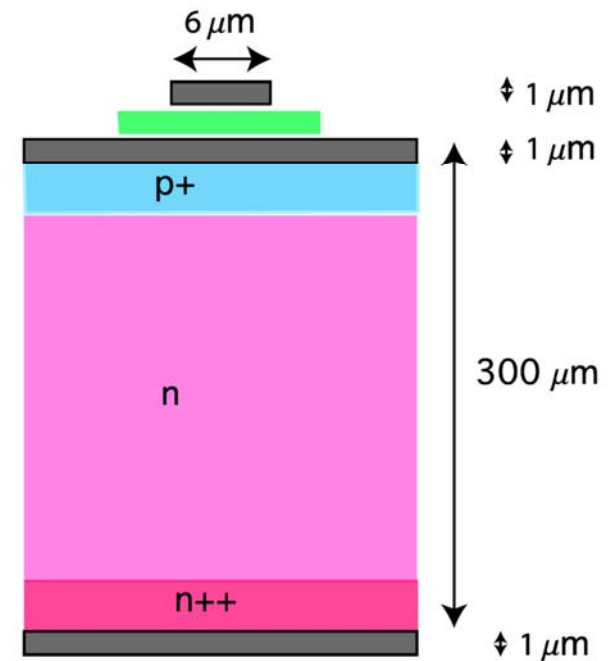


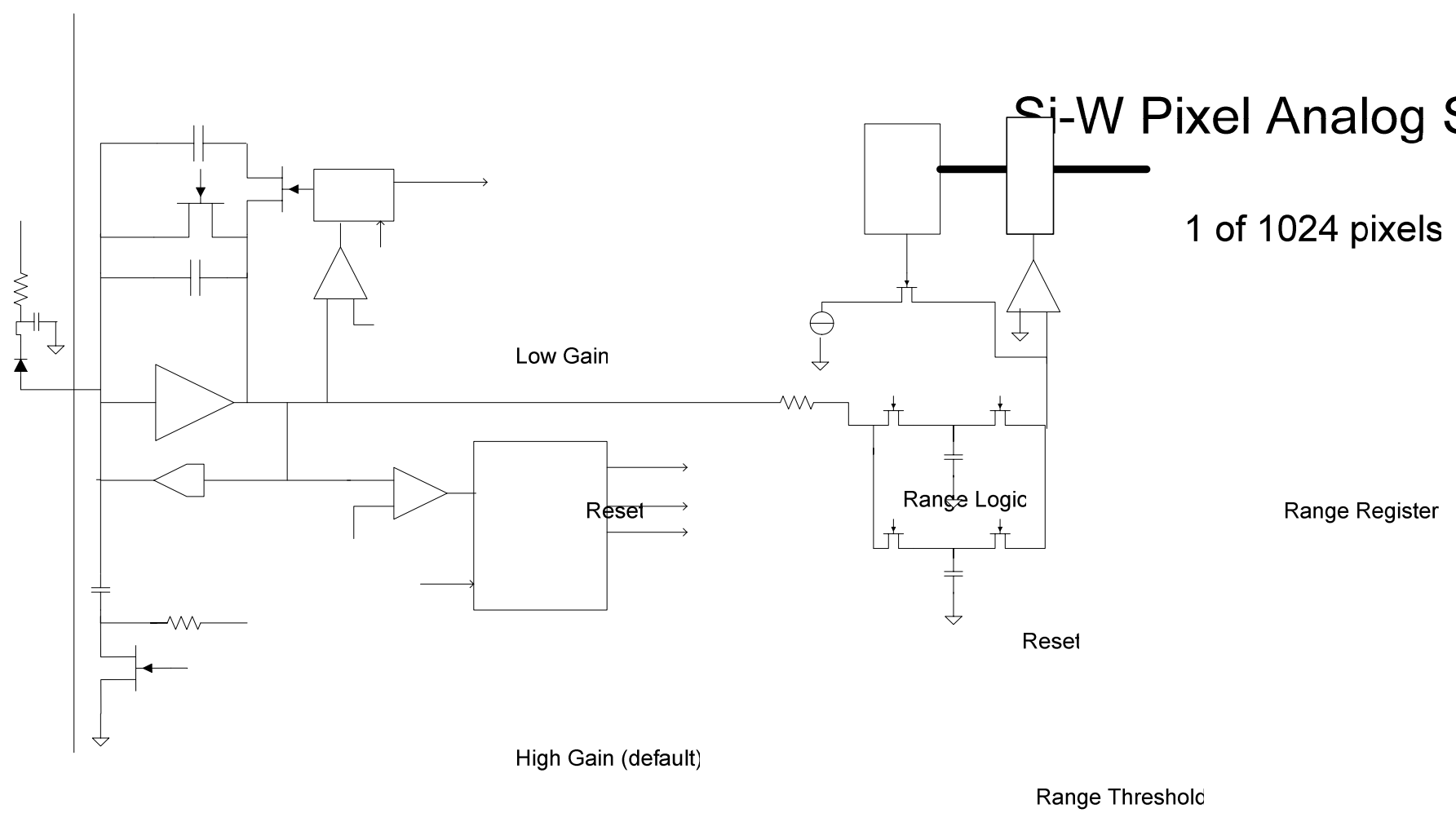
# EMCal Schematic Cross section



# Electronics requirements

- Signals
  - <math>< 2000 e</math> noise
  - Require MIPs with  $S/N > 7$
  - Max. signal 2500 MIPs (5mm pixels)
- Capacitance
  - Pixels: 5.7 pF
  - Traces:  $\sim 0.8$  pF per pixel crossing
  - Crosstalk:  $0.8 \text{ pF/Gain} \times C_{in} < 1\%$
- Resistance
  - 300 ohm max
- Power
  - $< 40 \text{ mW/wafer} \Rightarrow$  power cycling  
(An important LC feature!)
- Provide fully digitized outputs of charge and time on one ASIC for every wafer.





**Control Logic**  
 Pulses to Timing Latch,  
 Range Latch, and Event  
 Counter

Leakage Current Servo



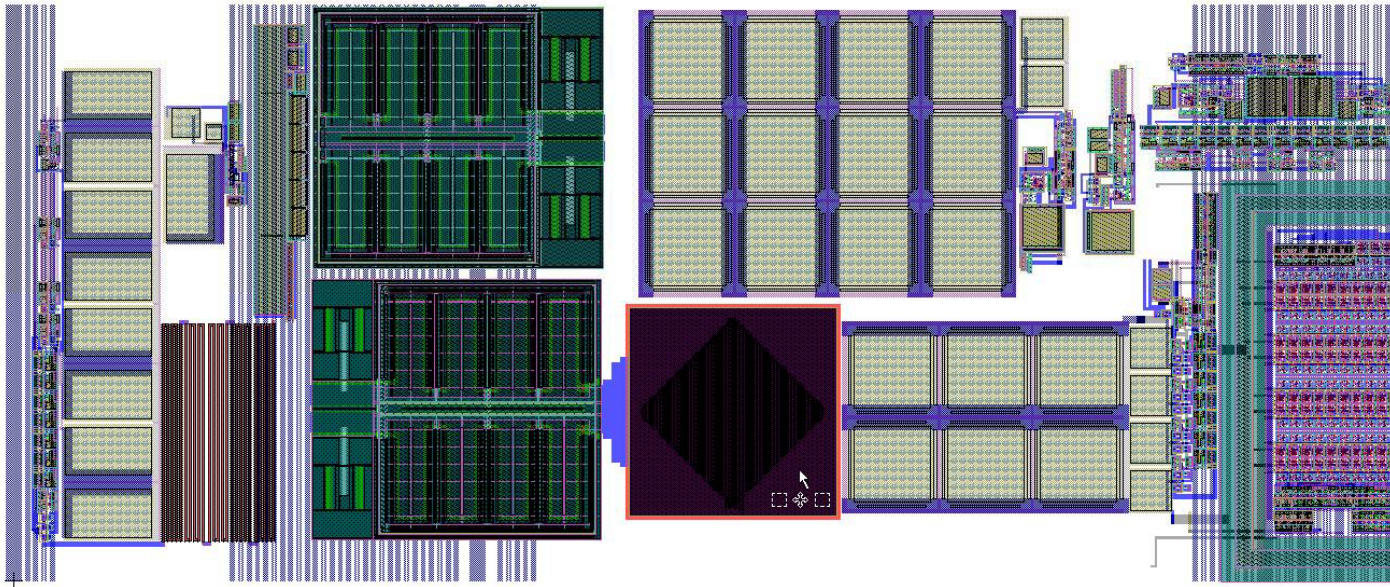
## Pulse “Shaping”

- Take full advantage of synchronous bunch structure:
  - Reset (clamp) feedback cap before bunch arrival. This is equivalent to double correlated sampling, except that the “before” measurement is forced to zero. This takes out low frequency noise and any integrated excursions of the amplifier.
  - Integration time constant will be  $0.5 - 1 \mu\text{sec}$ . Sample *synchronously* at  $2 - 3$  integration time constants.
  - Time from reset  $1 - 3 \mu\text{sec}$ , which is equivalent to a  $1 - 3 \mu\text{sec}$  differentiation.
- Noise:  $\sim 1000 e^-$  for  $\sim 20 \text{ pF}$ . (100 microA through input FET).

## Power

Cold Train/Bunch Structure							
Phase	Current (ma)	Instantaneous Power (mw)	Time begin (us)	Time End (us)	Duty Factor	Average Power (mw)	Comments
All Analog "on"	370.00	930.00	0.00	1,020.00	5.10E-03	4.7	Power ok with current through FET's
Hold "on", charge amp off	85.00	210.00	1,021.00	1,220.00	9.95E-04	0.2	
Analog power down	4.00	10.00	1,020.00	200,000.00	9.95E-01	9.9	
LVDS Receiver, etc		3.00	0.00	200,000.00	1.00E+00	3.0	Receiver always on.
Decode/Program		10.00	1.00	100.00	4.95E-04	0.0	Sequencing is vague!
ADC		100.00	1,021.00	1,220.00	9.95E-04	0.1	
Readout		50.00	1,220.00	3,220.00	1.00E-02	0.5	
Total						18.5	Total power OK

## KPix Cell 1 of 1024

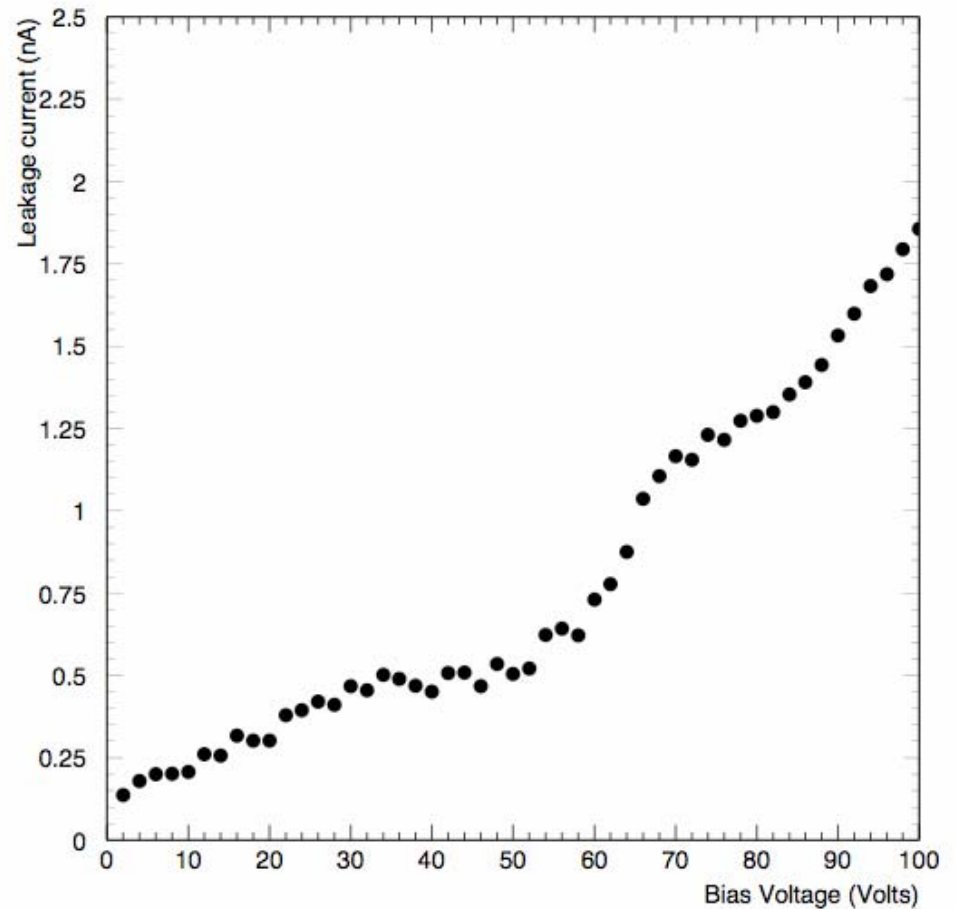


- First prototypes currently under test at SLAC
- Next submission will include external trigger for test beam

# Measurements on Prototypes

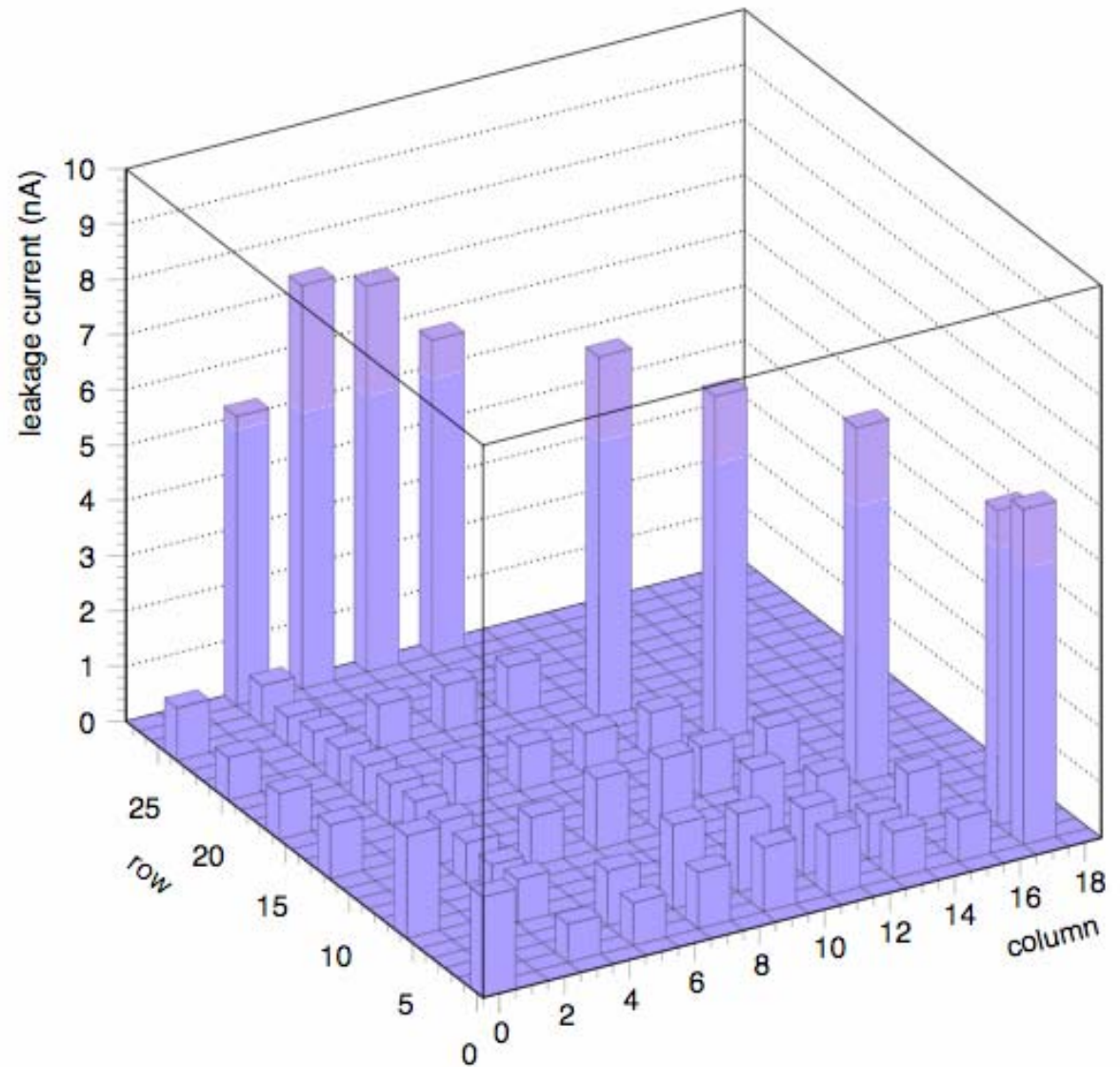
Leakage current looks fine:  
(10nA for 1microsecond gives  
only 250 electrons noise)

*Neighboring pixels not grounded*



Spot check of leakage current in one quadrant is as expected.

*Edge pixels have larger currents. In these tests the guard ring was left floating.*



Measurement of resistance slightly larger than nominal

Series resistance for 1 micron  $\times$  6 micron traces:

Expected (pure Al)

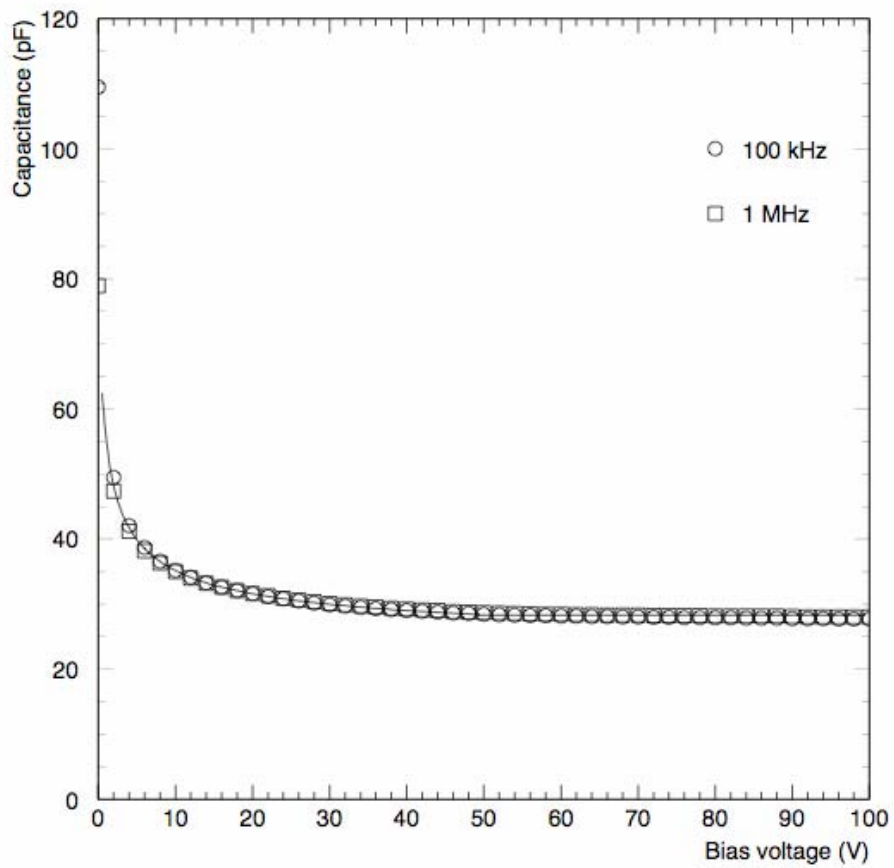
47 Ohms/cm

Measured

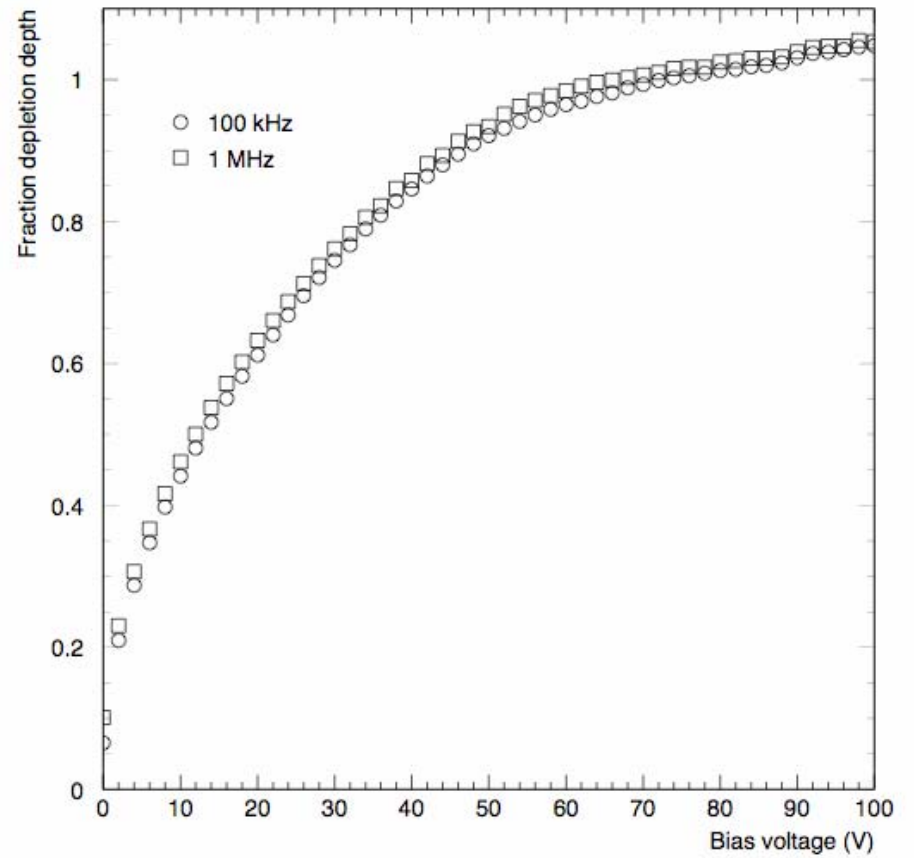
$(57 \pm 2)$  Ohms/cm

*Additional measurements underway*

Total resistance for longest traces can be a noise driver.



C-V curve as measured in the lab



Relative depletion

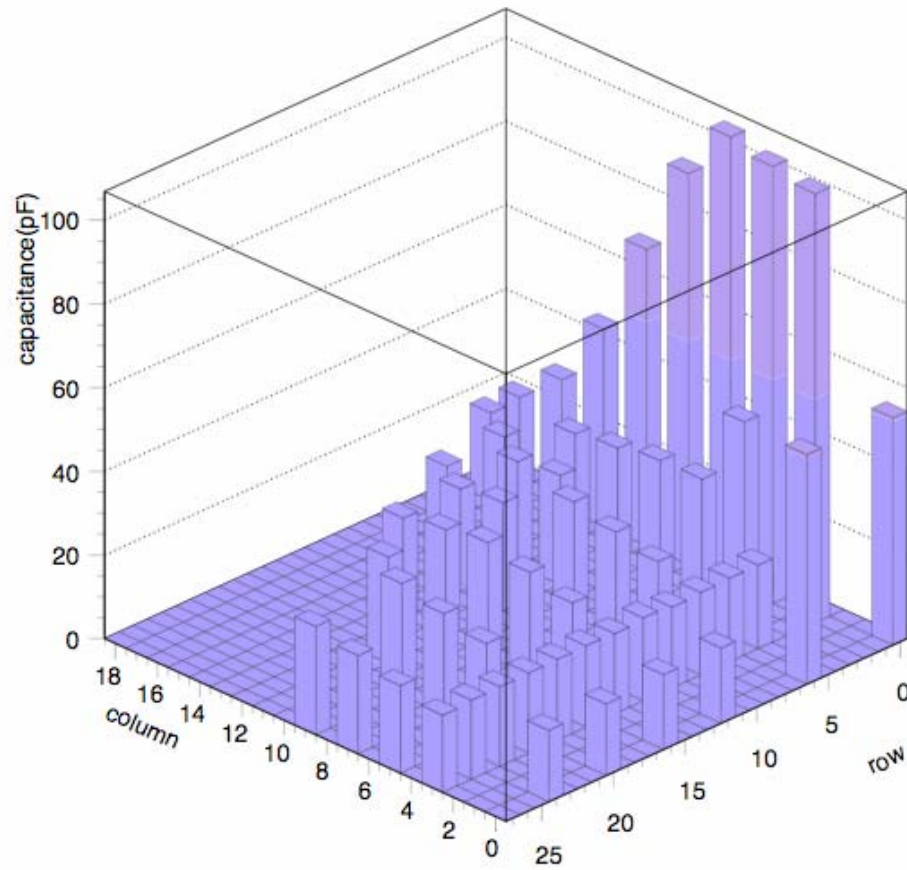
## Comparison expected and measured stray capacitance

Pixel	Column	Row	Calculated Capacitance(pF)	Measured Capacitance(pF)
567	7	9	23.35±0.61	25.07±0.25
564	7	15	22.96±0.61	24.70±0.24
561	7	21	22.56±0.61	24.23±0.24
558	7	27	22.17±0.61	23.60±0.21
515	5	3	44.00±0.90	46.55±0.42
512	5	9	21.63±0.61	22.55±0.23
509	5	15	21.18±0.61	22.06±0.22
506	5	21	20.73±0.61	21.73±0.22
503	5	27	20.28±0.61	21.00±0.20

Measurement agrees with expectation for 0.9 micron thick oxide and 6 micron wide traces (3.1 pF/cm)



Spot check of capacitances in one quadrant is as expected.



# Impact of Detector Technology on Detector Design

In a warm machine, exceptional pixels with large capacitance or series resistance lead to degraded time tag measurements

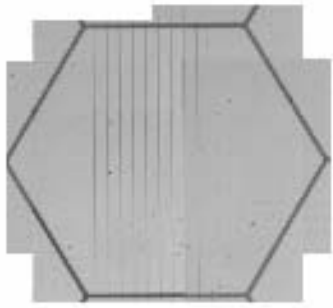
*Small impact on tagging performance since bad channels can be de-weighted in determining the average time of a track*

In a cold machine, exceptional pixels with large capacitance or series resistance lead to a higher rate of noise events in buffers

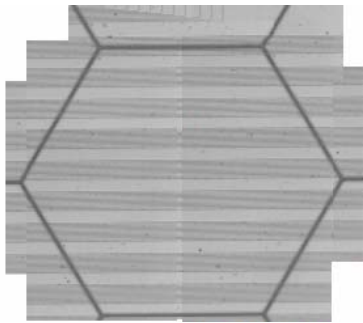
*Could lead to inefficiency late in the bunch train due to buffer overflow*

# Examples of capacitances

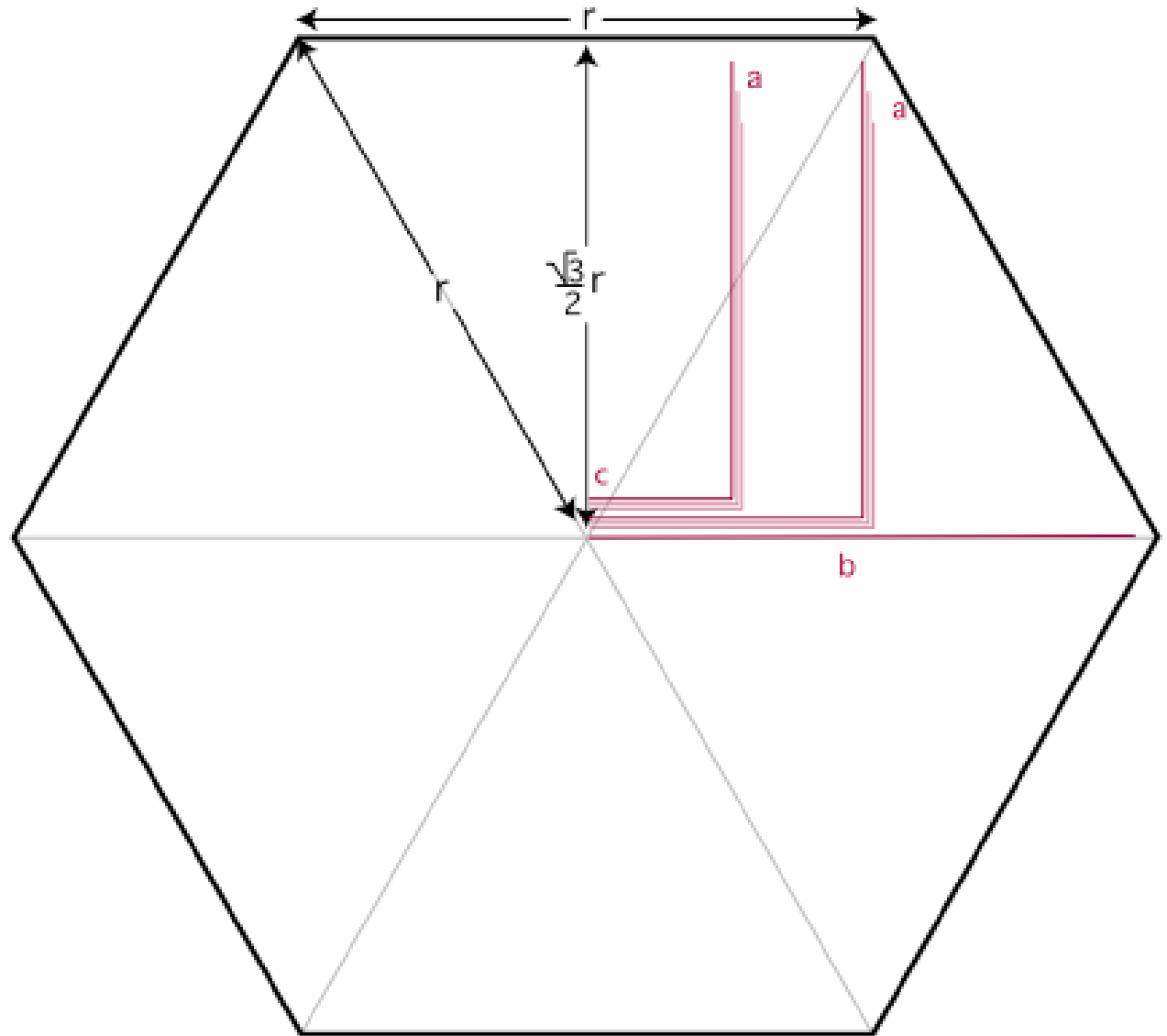
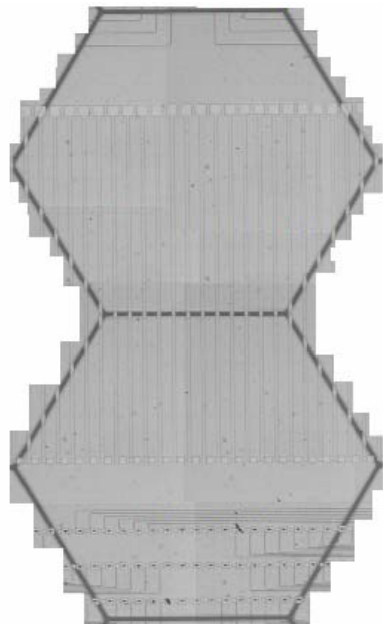
a)



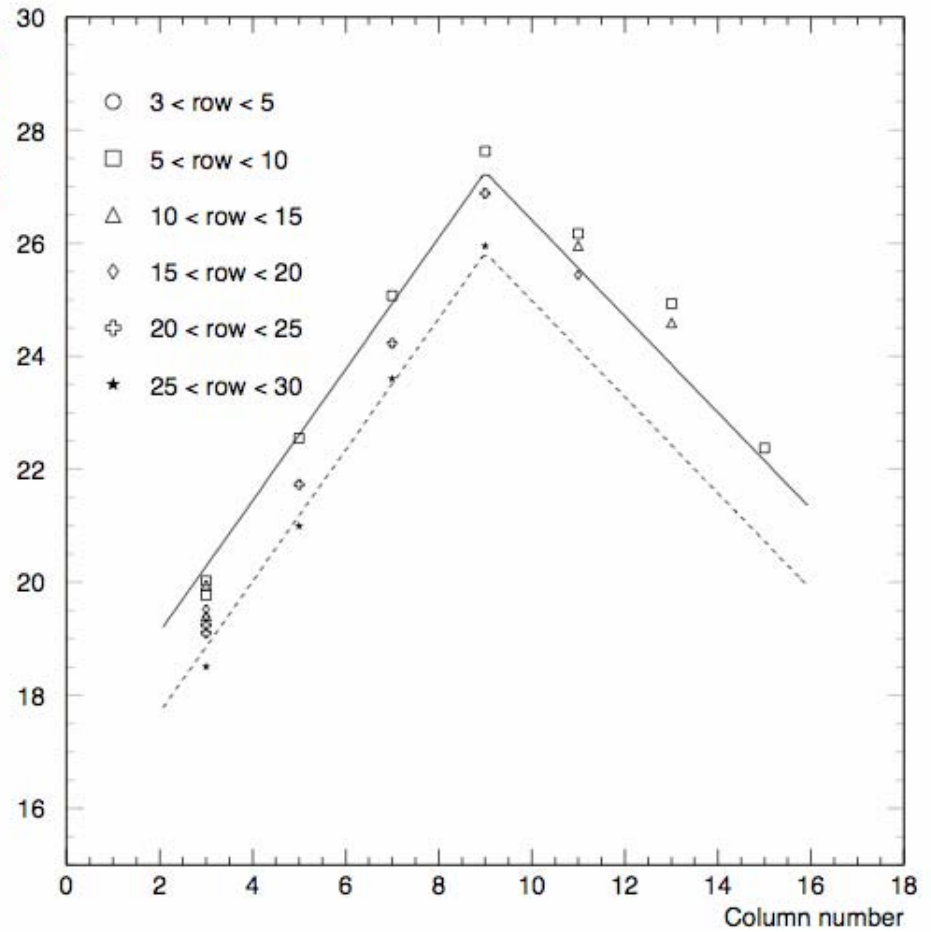
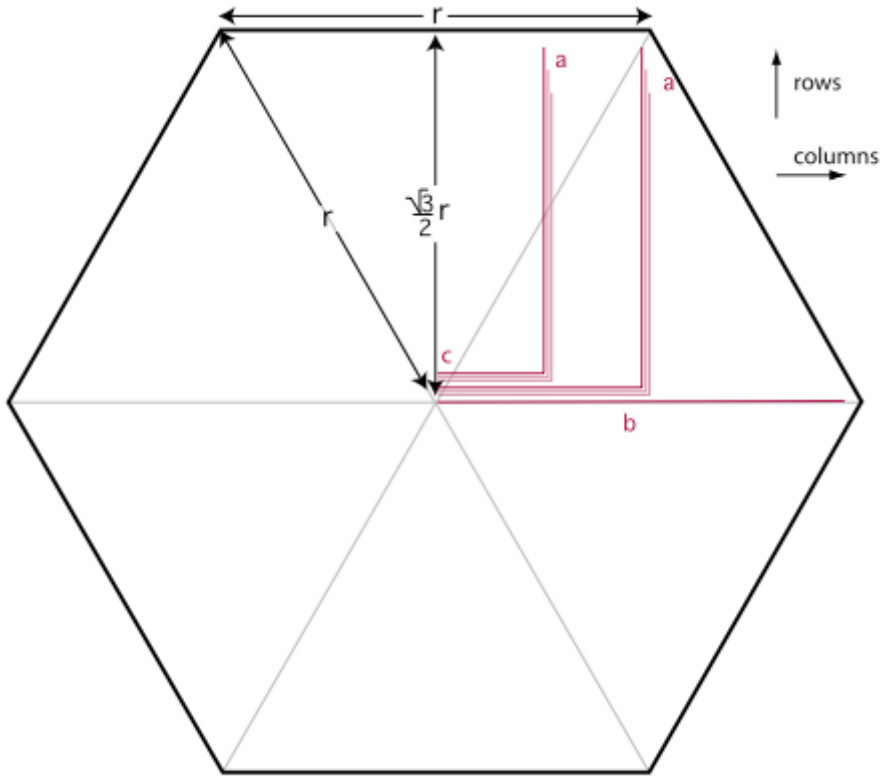
b)



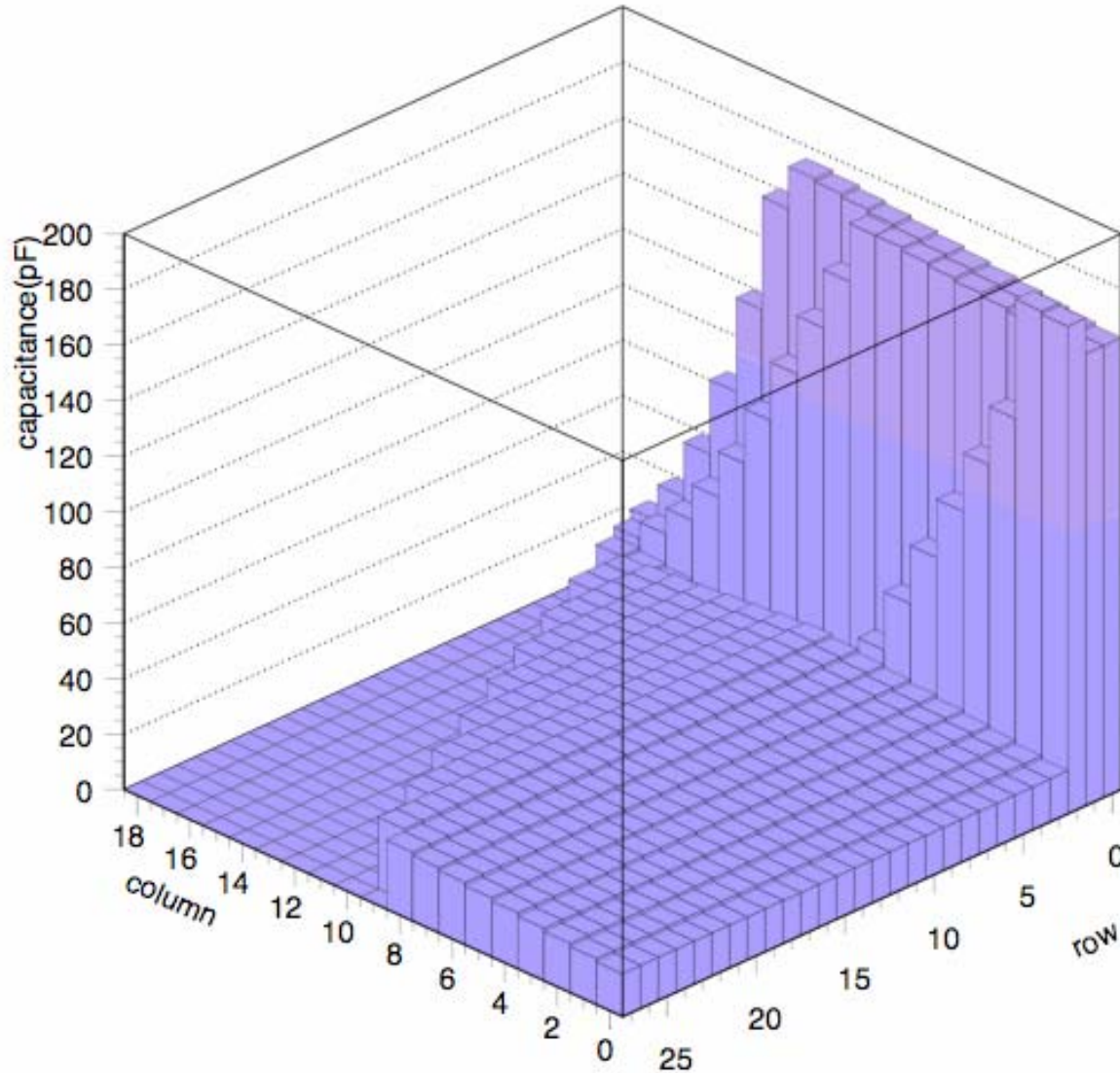
c)



Note that all pixels in a given row have nearly the same capacitance:



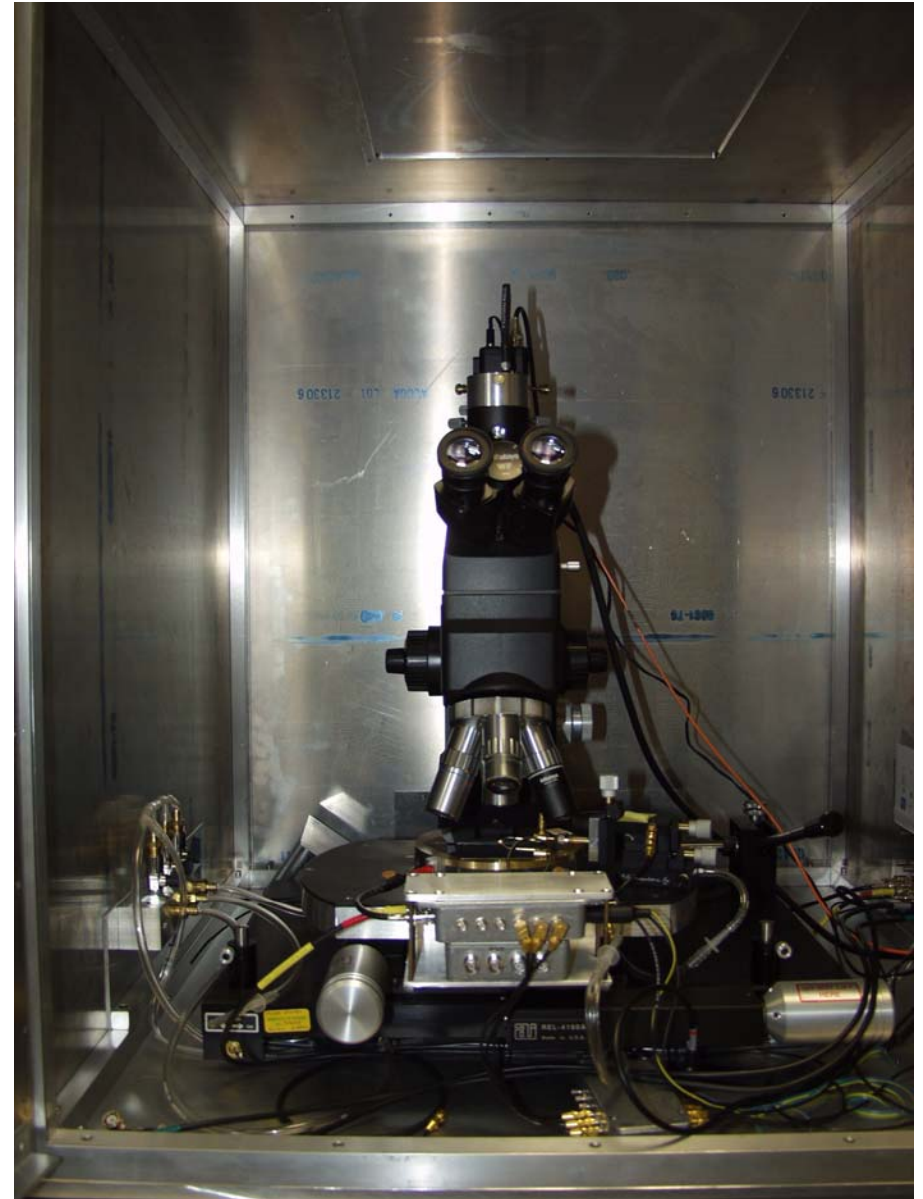
A simple model is under development for use in Monte Carlo simulations:



(Over estimates capacitance in region b because of unused channels in the 32 X 32 channel array)

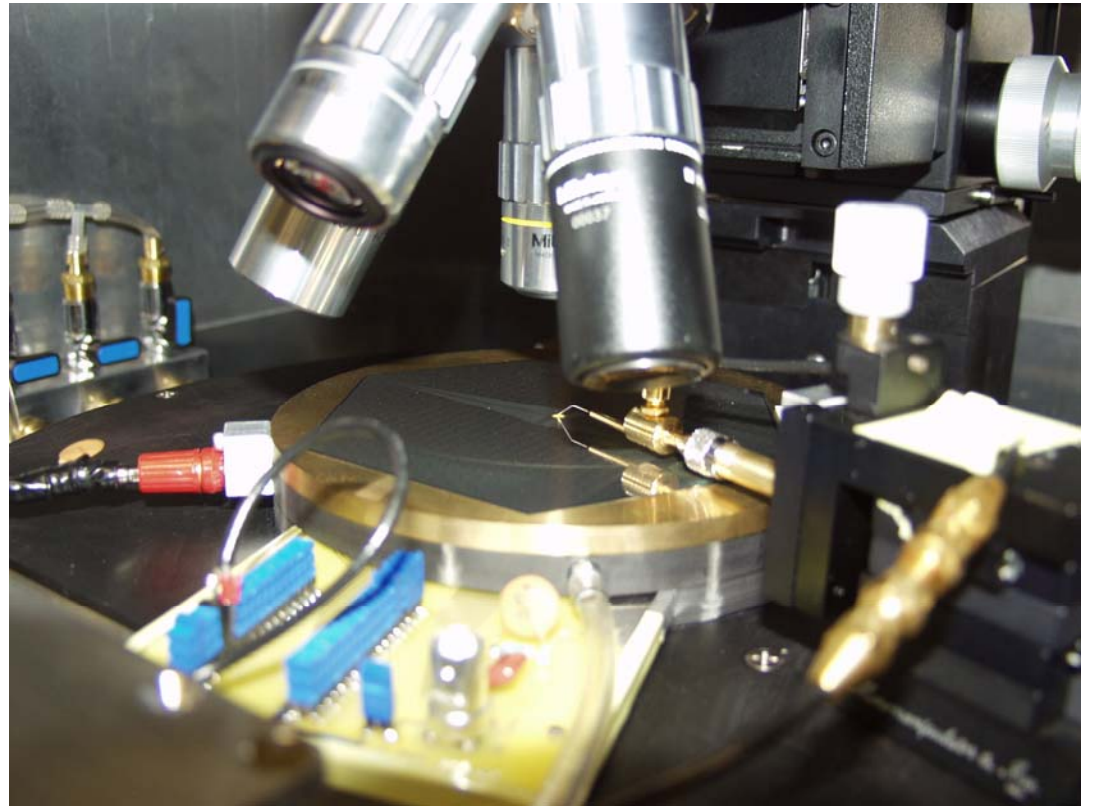
# Teststand for cosmics, laser and sources

- Modified probe station, allows laser to be target on entire detector
- IR microscope objective used to focus laser to  $\sim 10$ micron spot
- Bias applied to backside of detector using insulated chuck

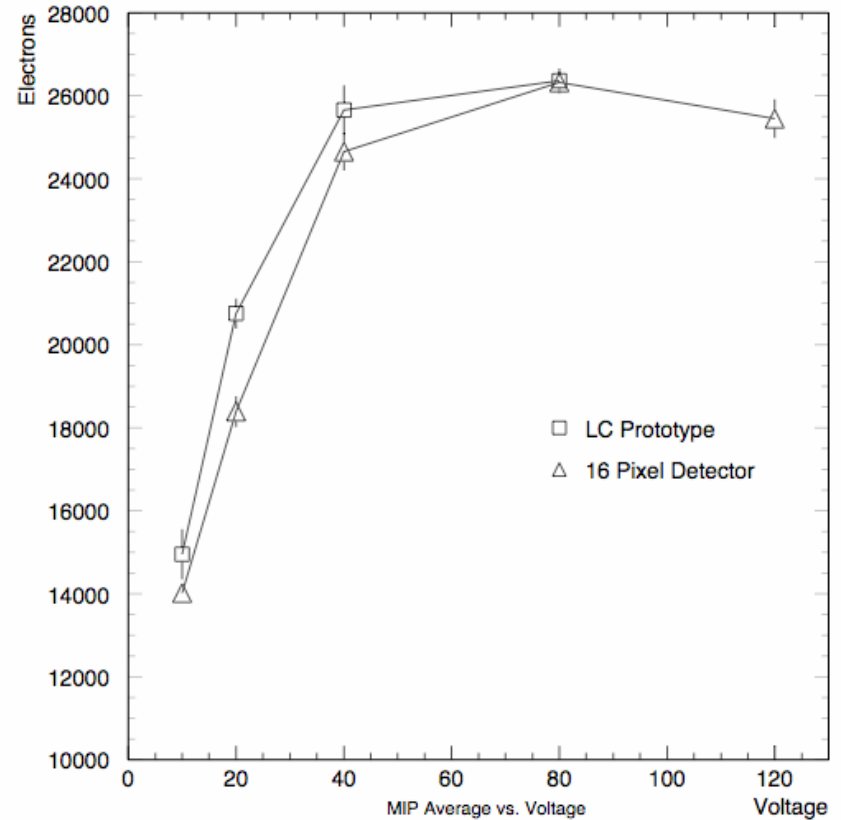
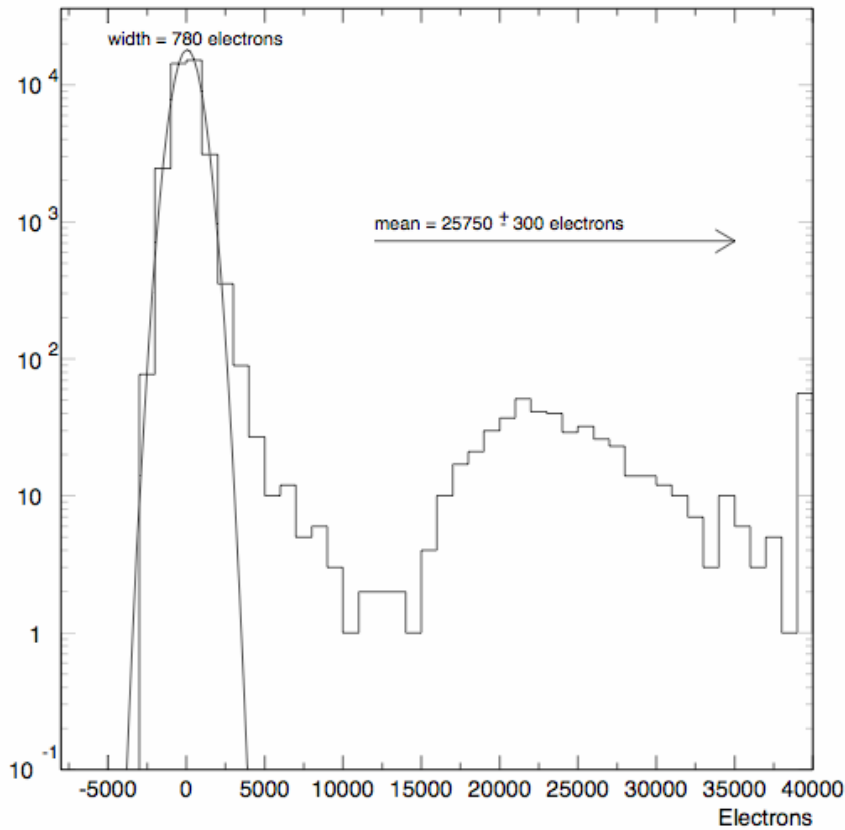
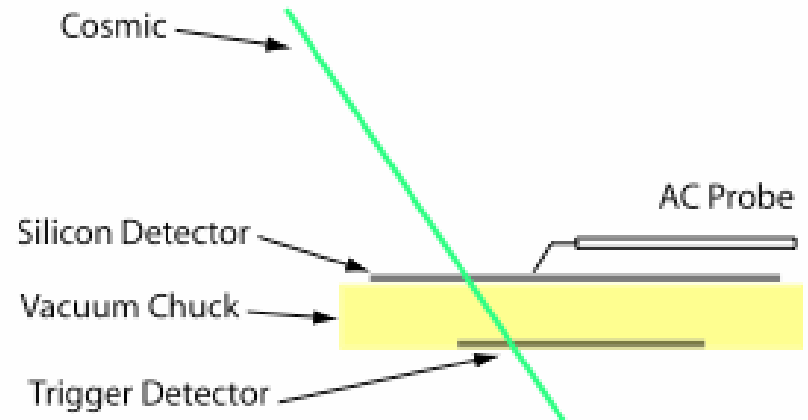


## Test Setup -- detector probing

- Contact made to test pads on bump bonding array using an AC probe
- Cables add  $\sim 20\text{pF}$  of additional capacitance, but noise performance is somewhat better than readout chip
- Use AMPTEK 250F preamp, shapers with  $\sim 1$  microsec shaping and a digitizing oscilloscope to mockup expected electronics
- PC board with  $1\text{cm} \times 1\text{cm}$  silicon pad detector used for cosmic trigger visible under chuck



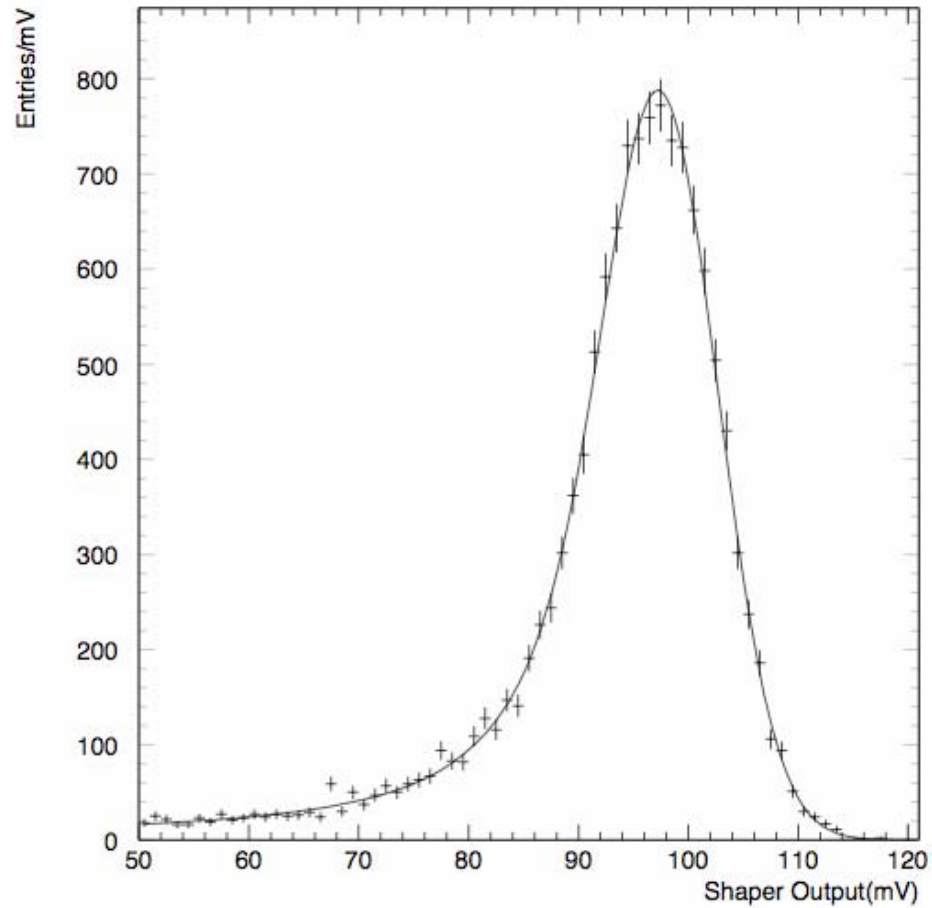
Response of detectors to Cosmics  
 (Single 5mm pixel)  
 Simulate LC electronics  
 (noise somewhat better)



Errors do not include 10% calibration uncertainty

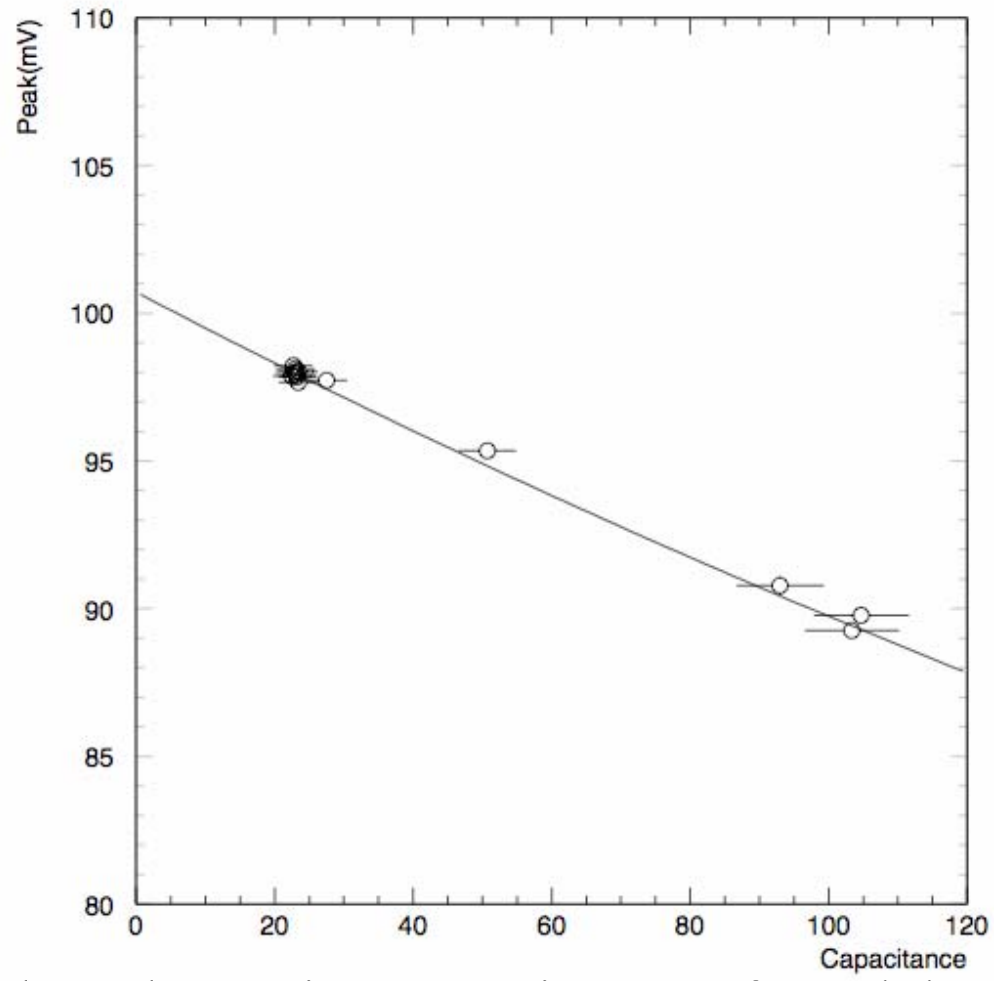


# Response of Detectors to 60KeV Gamma's from Am<sup>241</sup>

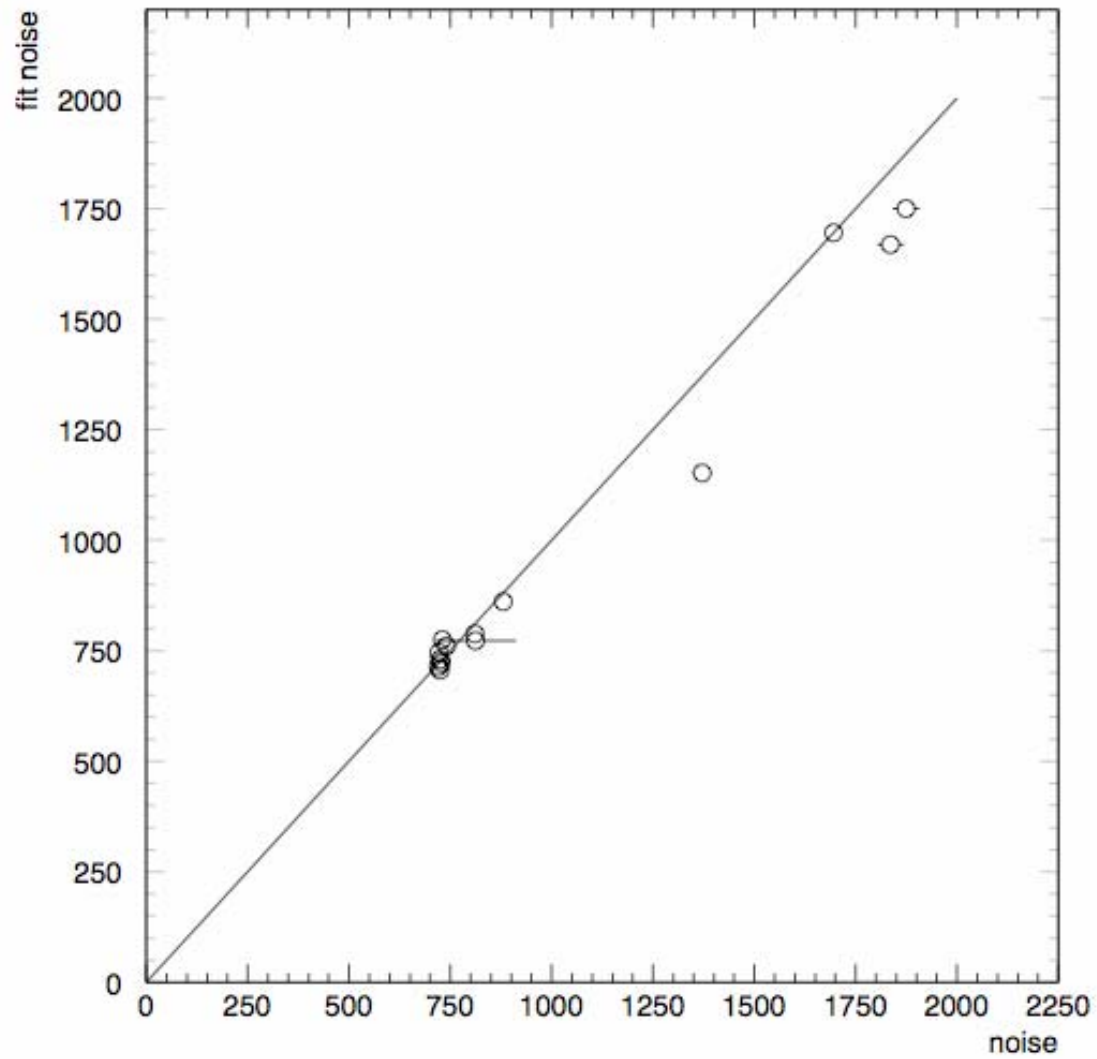


Possible ~1% wafer-wafer calibration?

# Mean calibration value versus capacitance



Slope is determined by “dynamic” capacitance of our laboratory electronics  $C_{\text{dyn}} \sim 790\text{pF}$

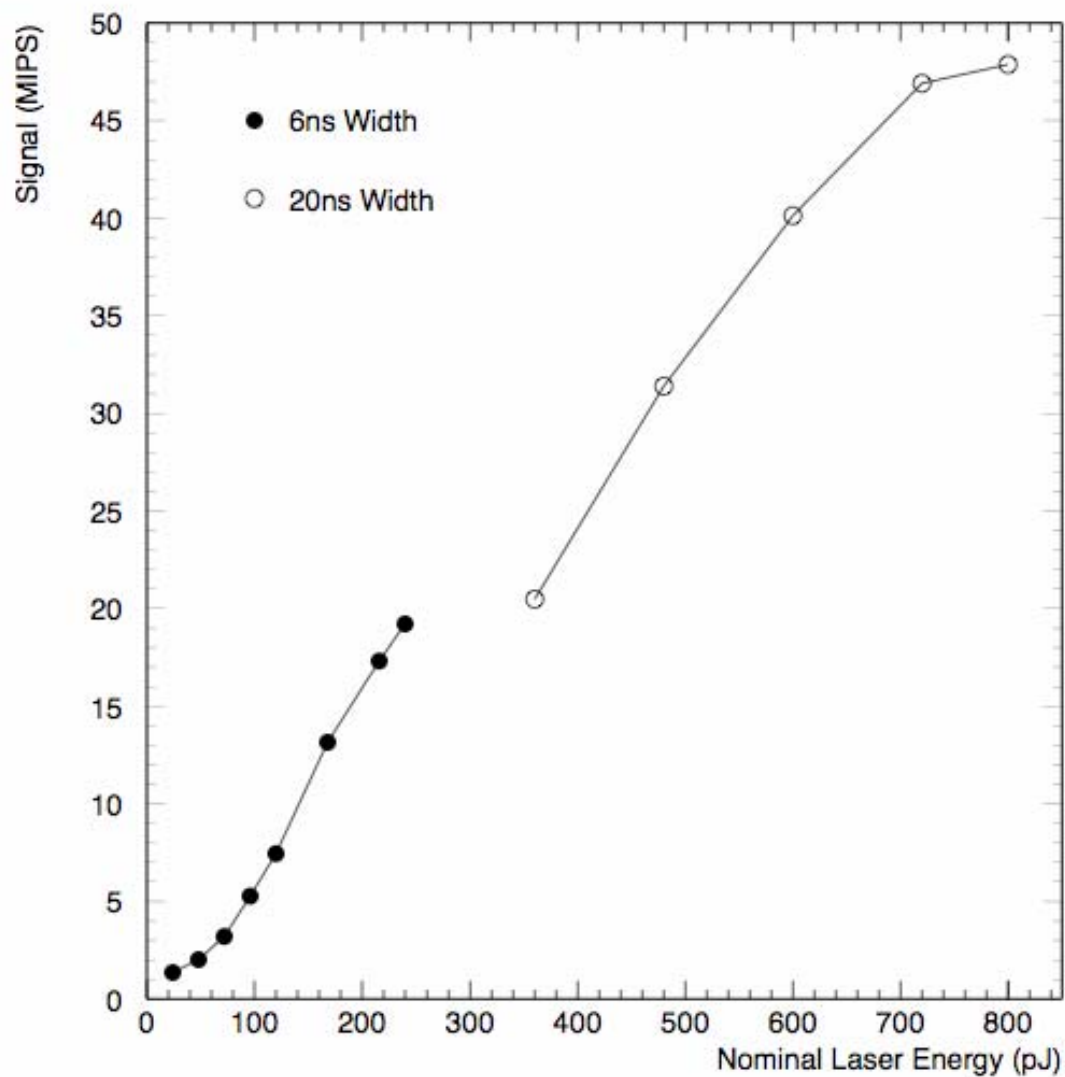


Noise is consistent with expectation from capacitance and series resistance

## Laser studies

Use 1024nm laser that penetrates the entire silicon wafer

The nonlinearities are probably due entirely to the difference between nominal and true laser power



# Conclusion

- A narrow gap silicon--tungsten detector for LC physics is attractive
- First round of prototype silicon detectors perform as expected
- Detectors can be produced with workable values of stray capacitance and series resistance
- Some minor changes needed for cold design