Preliminary Thoughts on the Silicon Tracking DAQ

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From preliminary thinking/discussions with Jean François Genat and a few others…

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Starting Points:

- **The Front End and readout chip on detector**
- **The elementary module**
- **The LDC case is taken here as example, but it can be directly extrapolated for any of the other two detector concepts.**

Detector data

- Pulse height: Cluster centroid to improve position resolution to O(μm)

  Detector pulse sampling 5-10 samples 8-10 bit A/D (Wilkinson) stored in an analog buffer

- Time: Two scales:

  - Coarse 150-300ns BCO tagging

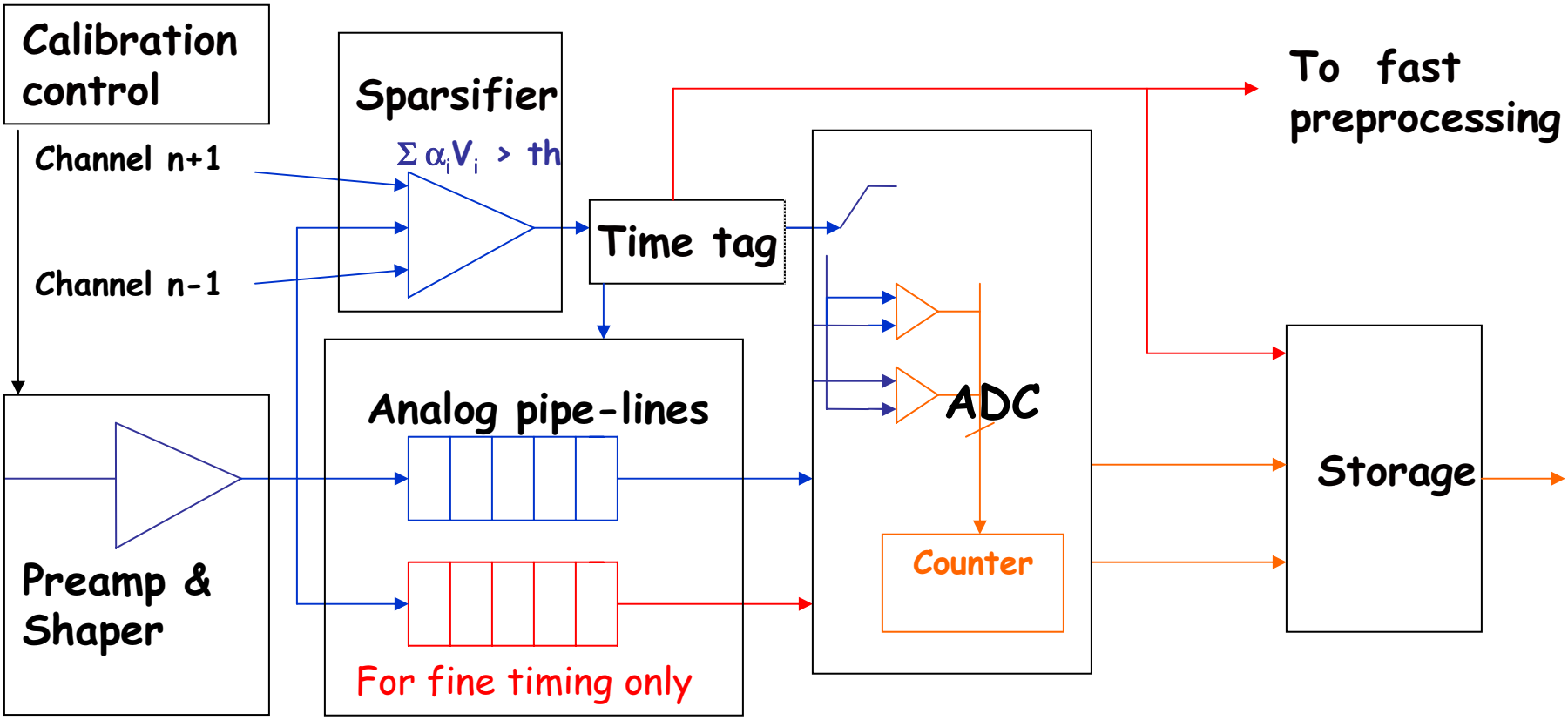
  - Fine nanosecond timing for coordinate along the strip and fine BCO tagging for some regions

Not to replace another detector layer or double sided detector, but give an estimation to a few cm

On-detector FE chip

- Pulse sampling: *5-10 samples over 2 shaping times*
- Buffering: *8-deep 2D analog buffer (8*5-10 samples cells) per channel*
- Analog-Digital conversion *Wilkinson optimum (SVX architecture)*
- Sparsification/calibration : *Integrated on detector FE chip*
- Digital processing: *Amplitude and time estimation + charge cluster algorithm*
- Power: 1/200 ILC duty cycle: *FE Power cycling*

Front-end architecture



Charge 1-40 MIP, S/N~ 15-20, Time resolutions: BC tagging, fine: ~ 2ns

Present technologies - Deep Sub-Micron CMOS
UMC 0.18 μm, 0.13 μm

Time-stamping on *all layers*
fine time resolution
on *some layers*

FE is expected to serve 1024 channels (high multiplexing at A/D level)

Charge measurements Expected

- Preamp + Shaper
  Gain: 20mV/MIP over 1-30 MIP
  Noise: CMOS 180 nm: 280e- + 10.5e-/pF @ 3 μs

- Analog buffer
  8-deep (cells of 5-10 100 fF caps)

- Sparsifier
  Threshold an analog sum of 3 adjacent channels after pulse shaping

- ADC
  10-12 bits
  Clocked at 96 MHz

- Signal-Noise ratio
  The larger, the best ! 15-20 ?

Time measurements Expected

- Time stamping

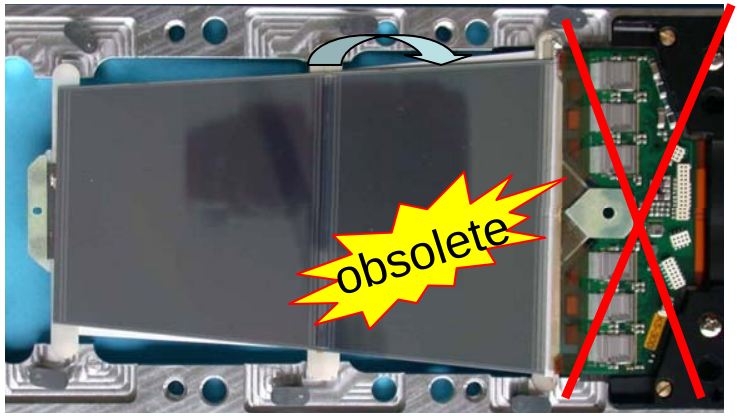
  Order of 30 to 50 ns
  Time-stamp the sparsifier output at 4 * BCO clock (12 MHz)

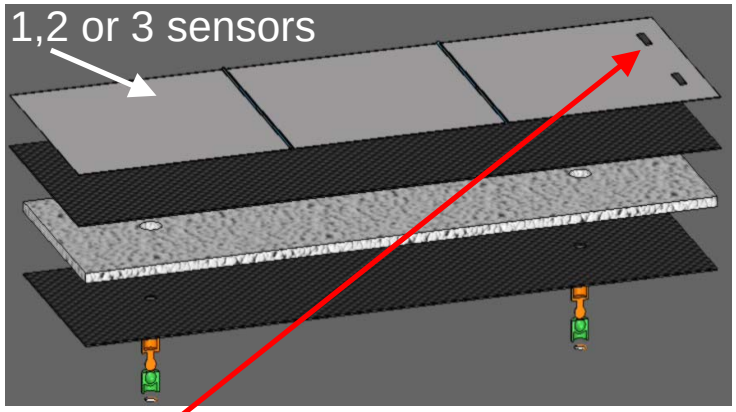
- Fine time measurement

  Order of 1 to 3 ns
  32 * BCO on chip interpolated clock sampling (PLL @96 MHz)
  Use digital processing over 5-10 digitized samples

Total data per hit channel: Address (32 bits)+time(BCO) + data (10 bits)

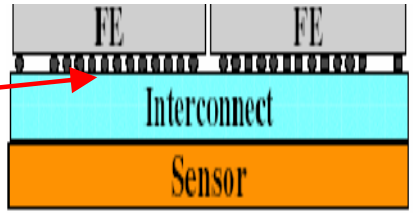
The elementary module





New wiring of FE chips onto the detector under investigation:

Conservative: Large chip 2.5x0.625cm^2 ≤ 0.13µm technology 1024 channels sitting on detector using flip chip bump bonding



Or 3D integration technology when available

Serial links used wherever possible to avoid multiple wire connexion improving transparency & reliability

The cabling

MITEQ
100 Davids Drive · Hauppauge · NY 11788
631-436-7400 · Fax: 631-436-7430

6 GHz SCM FIBER OPTIC LINK

On the detector, use of micro-coax, 2.54 mm diameter, 300 mW at 1 GHz, 900 a 3 GHz, and can be power cycled

Or Kapton cables

FEATURES

- **Small size**
- **Bandwidth to 6 GHz**
- **No external control circuits required**
- **Transimpedance amplifier in both transmitter and receiver**

TYPICAL APPLICATIONS

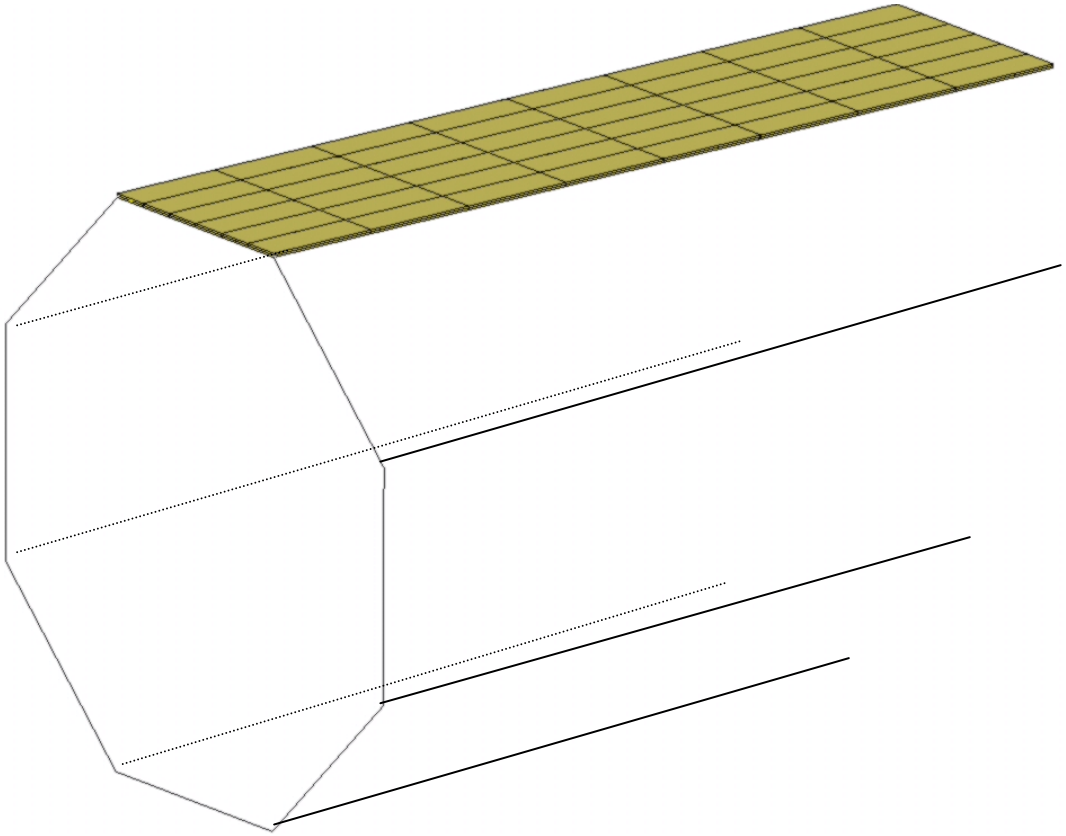
- **Antenna remoting**
- **Local oscillator remoting**
- **Interfacility communication links**

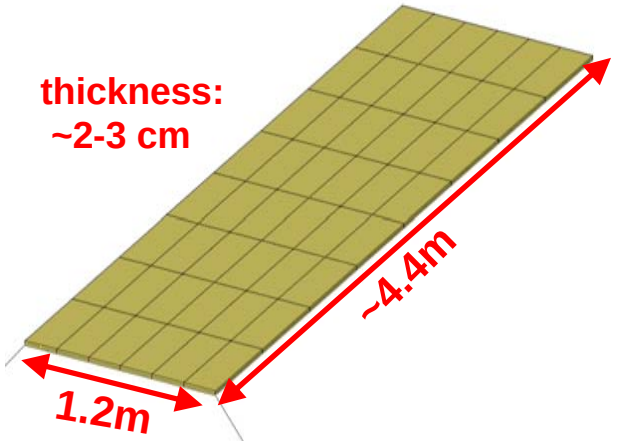
Chip driver + driver opto
Relatively high dissipation cannot be power cycled.

→ Under investigation

SET: Silicon External Tracker

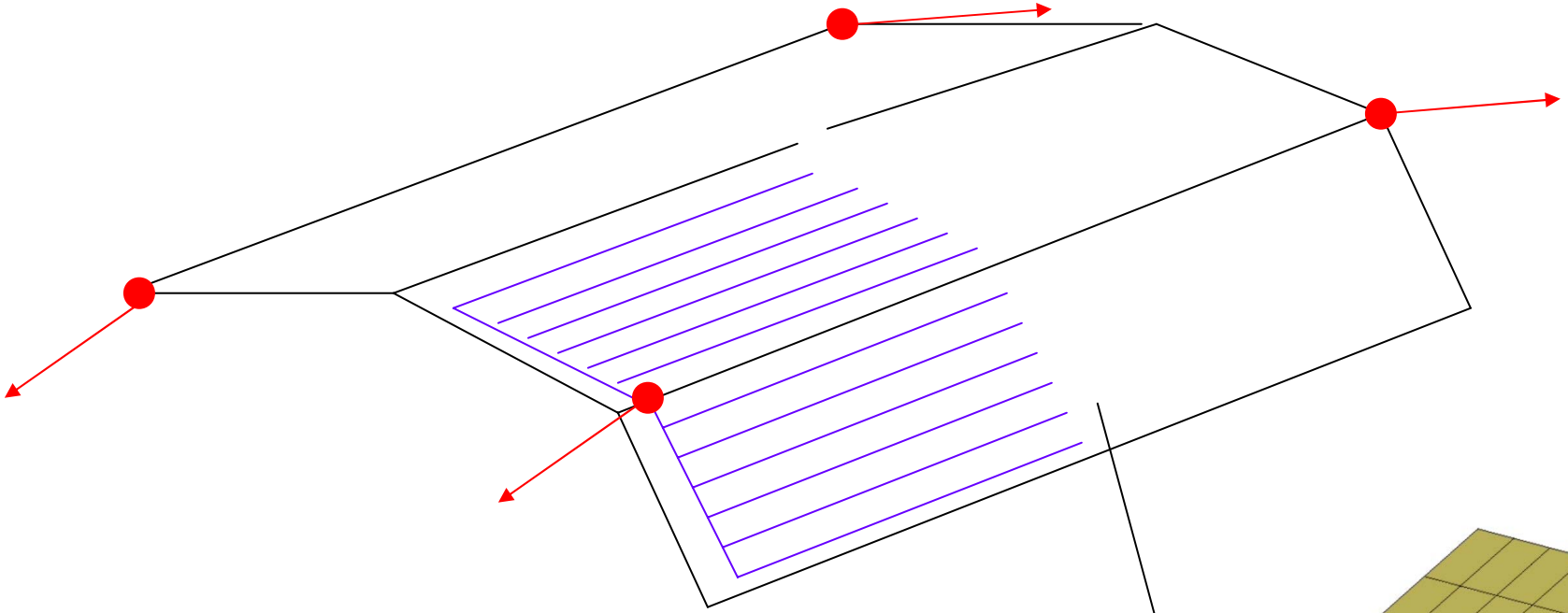
False double sided layer
60 cm long µstrips
20x20 cm^2 sensors

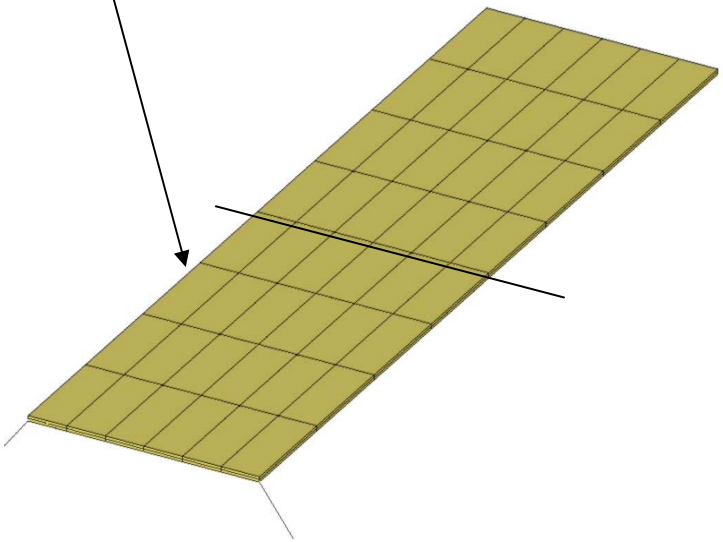




# ladders/octagone	96
# sensors/octagone	288
# channels/octagone	196608
# µchips/octagone	192
# µcoax/octagone	192
# fibres/octagone	2
# µchips/fibre	96
# voies/fibre	98304

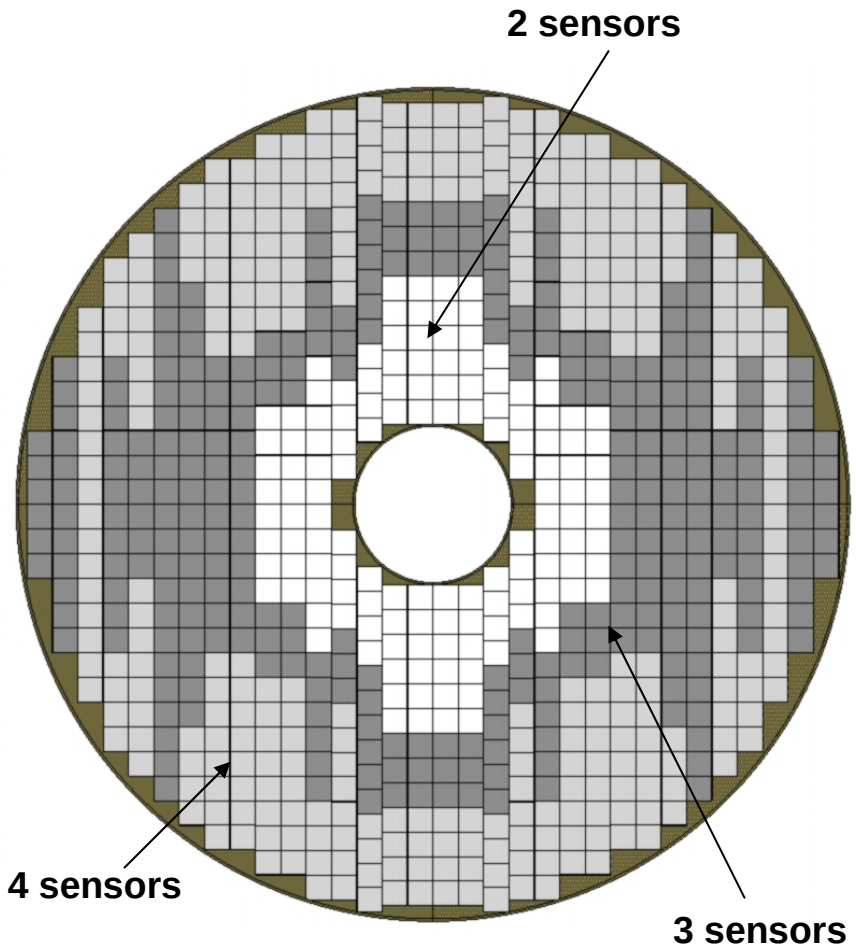
Total surface: ~86 m^2
Nb channels: 1,572864
Nb of fibres: 8 per side





Daisy chaining the FE chips of 4 adjacent ladders,
on the 2 planes of the same
octagonal plane, with a micro coax;
Thus 6 micro-coax/octogonal plane on each side,
all read out in parallel by fibres.
One fiber serves 2 semi-octogonal planes.
Per bunch and per Fiber:
1% x 3246 x 98304 = 3.2 Mwords
Thus 19.2 Mbyte or resp 32Mbyte depending the processing on detector
Duration of the readout procedure: 19.2M or 32M/6Gb/s = 3.2 or 5.3 ms

End Cap Tracker



Total area per XUV: ~15 m2

Nb modules x 2, 3 or 4 (10x10 cm^2)/plane: 68, 88, 92

Total modules/plan: 248 (248 µchips)

Total µchips/plan: 248 (1 per module)

Total Nb of channels/plan: 253952

Total Nb of channels/XUV: 761856

All these numbers X 2 because 2 sides!

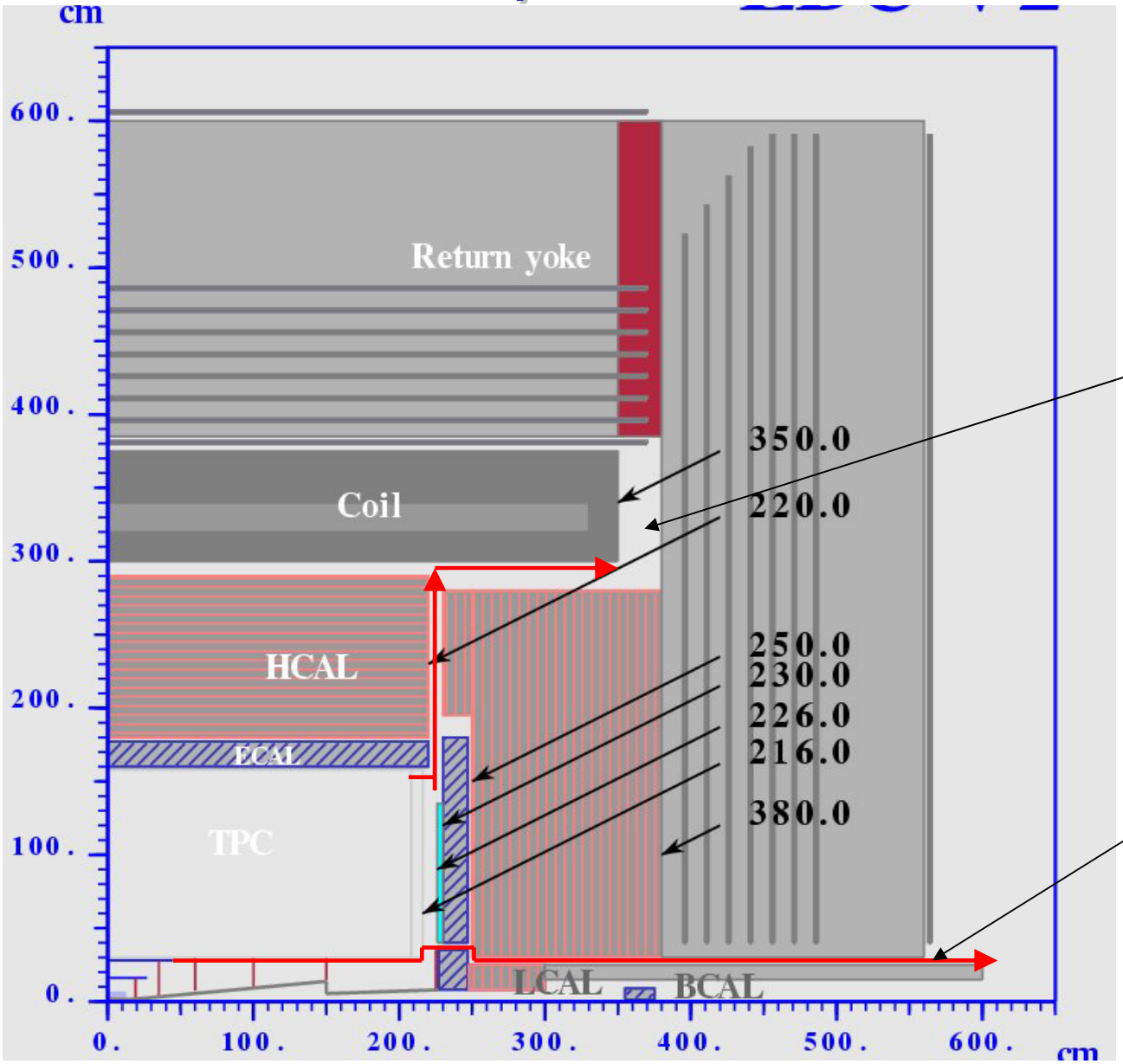
Total number of chips: 1488

Total number of channels: 1,523712

XUV gives similar scenario than SET. Thus also relatively few fibres on each side.

For this design:
modules are made of 10x10 cm^2 sensors (6'').
(Working on a design with 20x20 cm^2 10'' sensors)

Silicon detectors cabling paths out of the detector; ex: LDC case



SET & ECT fibres path: from the Top

SIT & FTD fibres path: along the beampipe

Conclusions

- The digitized and preprocessed information from the Si tracking will be provided at the detector stage
- Of the order of 8 to 16 fibers for the external layers per side
- Exact number of channels and cables for

Inner parts to be evaluated; will depend on the technologies

Starting to have an idea of the way to go to DAQ

Followed in the SiLC collab meetings

http://lpnhe-lc.in2p3.fr/silc2