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Status on the development of Front-end and readout electronics for large Silicon Trackers

J. David, M. Dhellot, J.F. Genat, F. Kapusta, H. Lebbolo,
T-H. Pham, F. Rossel, A. Savoy-Navarro
CNRS/IN2P3/LPNHE Universités Paris 6 and 7

E. Deumens, P. Malisse
IMEC, Belgium

D. Fougeron, R. Hermel, Y. Karyotakis, S. Vilalte
CNRS/IN2P3/LAPP, Annecy le Vieux

LPNHE, 4 Place Jussieu, 75252 Paris CEDEX 05 France
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
LAPP, 9 Chemin de Bellevue, BP110 F-74941, Annecy le Vieux, France

Abstract. Final results on a CMOS 0.18 μm Front-End chip for Silicon strips readout are summarized and preliminary results on time measurement are discussed. The status of the next version in 0.13 μm is briefly presented.

Keywords. Silicon, readout, front-end, deep sub-micron

1. Introduction

In any detector concept foreseen at the ILC, a front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimised keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the best integrated technologies available that allow to avoid as much as possible material added to the detector, such as connexions in terms of connectors, hybrid circuits, kaptons, and lead as well to a manageable amount of dissipated power. These technologies allow also to implement efficient data extraction and signal processing techniques such as analog sampling and on-chip digitization. For detectors that covers of the order of 100 square meters and millions of channels, the multiplexing of several tasks such as analog to digital conversion and zero suppression is mandatory.

2. Silicon strips detector numbers and detector data

At the ILC, the Silicon trackers will have up to ten millions of 10 - 60 cm long strips [1]. Readout pitch is foreseen to be 50 to 100 μm, DC or AC coupled. The occupancy defined as the percentage of channels hit per bunch crossing will be less than 1% in the outer barrel and end caps layers, less than 5% in the inner barrel and end caps.
The ILC machine is foreseen to run bunches spaced by 150-300 ns for a data taking period of 1 ms followed by a 200 ms idle stage available for readout.
Pulse height will be used to improve the position resolution to a few μm, 5 to 10 samples of the detector pulse will be digitized with an 8-10 bits Wilkinson AD converter after storage in an analog pipe-line.
Time will be recorded on two scales:
- Coarse for 150-300 ns beam crossing tagging.
- Fine nanosecond timing, in order to estimate the coordinate along the strip. This is not intended to replace another detector layer, but will provide an estimation of the longitudinal position to a few centimeters.

3. On detector electronics

The front-end chip will integrate the following functions:
- Low noise amplification and pulse shaping.
- Pulse sampling: 5-10 samples over two shaping times.
- Buffering: 8-deep 2D analog buffer (5-10 samples, and 8 events).
- Analog to Digital conversion: Wilkinson is optimum in terms of room and power.
- Sparsification/calibration: both implemented on-chip.
- Digital processing: amplitude/time estimation, and charge cluster algorithm.
- Power cycling: take benefit of the 1/200 duty cycle of the ILC engine.

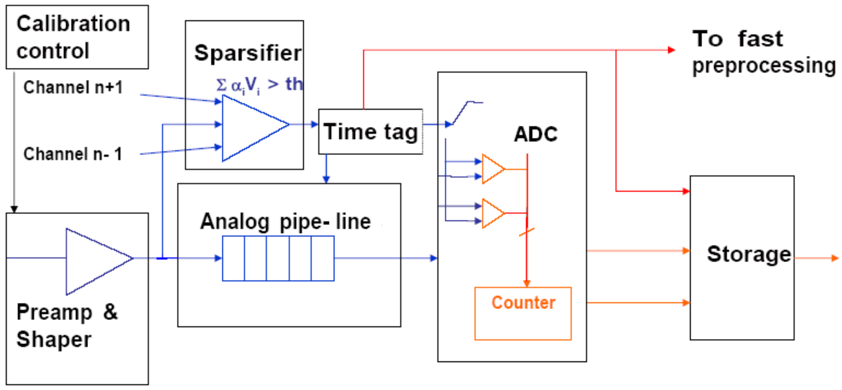

Figure 1. Front-End architecture

3.1 Expected charge measurements

- Gain: 20mV/MIP over 1-30 MIP,
- Noise: 280e- + 10.5e-/pF (as simulated in CMOS 0.18 μm)
- Analog buffer: 8-deep (cells of 5-10 100 fF capacitors)
- Sparsifier: Threshold an analog sum of three adjacent channels after pulse shaping
- ADC: 10-12 bits Wilkinson clocked at 96 MHz

3.2 Expected Time measurements

- Time stamping: 30-50ns Time stamp the sparsifier output a 4*BCO frequency clock.
- Fine time measurement: 1-3ns 32*BCO frequency clock multiplied on-chip.

Use digital signal processing over 5-10 digitized samples.
Expected fine time resolution: simulation under Matlab using a model of the full electronics chain from the preamplifier up to the ADC using a least squares fit algorithm from Cleland and Stern [3].
At S/N = 25, 8 samples and 50ns shaping time, 1.8 ns time resolution is foreseen.

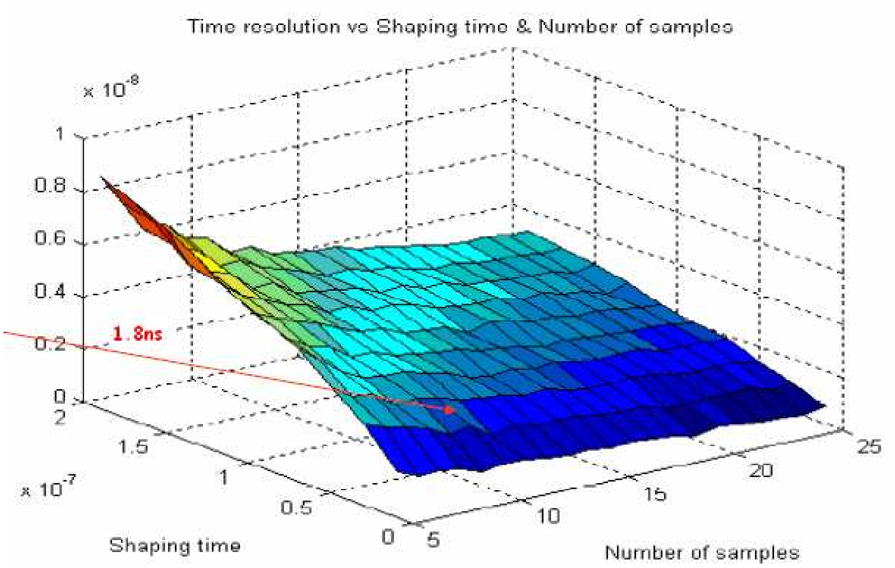

Figure 2. Expected fine time resolution

4. Overall noise contributions

Using CMOS 0.18 μm a signal to noise ratio of 25 is foreseen, according to Table 1. CMOS 0.13 μm is under investigations.

Table 1. Overall noise contributions at 30 pF detector capacitance and 3 μs shaping time

Source	Value	Noise 0.18 μm CMOS
Input stage (measured)	gm = 0.7 mA/V	615 e- (measured)
m Detector leak	10 nA	588 e- (from literature)
Biasing resistor	10 MΩ	423 (thermal noise)
Total		950 e-

5. Front-end test chip in CMOS 0.18 μm

The following structure has been submitted to Europractice and measured [2]. The chain comprises a low noise preamplifier, an RC-CR shaper, a Sample and Hold, a voltage follower and a comparator.

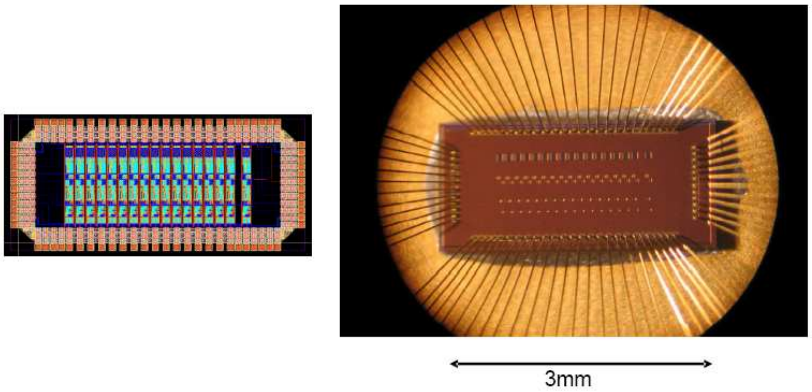

Figure 3. CMOS 0.18 μm UMC Silicon. 16 + 1 channel CMOS (layout and picture)

5.1 Preamp test results

Twelve chips have been tested. One single failure was found in a comparator, and the following numbers were obtained:
- Gain: 8 mV/MIP as expected.
- Linearity: +/- 1.5% against +/- 0.5 % expected.
due to large resistive transistor poorly modeled.
- Dynamic range: 50 MIP against 90 MIP expected, but within specs.
- Noise @ 70 μW power, 3 μs-20μs rise-fall times:
498 + 16.5 e-/pF against 490 + 16.5 e-/pF expected

5.2 Shaper test results

The noise at the output of the shaper is shown below, as measured on a chip on board (wire-bonded) test card, to 375 e- against 280 simulated, due to a small bump in the frequency

response, leading to small oscillations. The following results are obtained:
- Peaking time: 2-6 μs tunable against 1-10 targeted
- 6 MHz bump (650 e- added noise) show up in the soldered PCB test card, mostly removed using wired on board version, due to smaller parasitic capacitance (2 pF against 10 pF).
- Noise @ 70 μW power, 3 μs peaking time

375 + 10.4 e-/pF against 274 + 8.9 e-/pF expected.

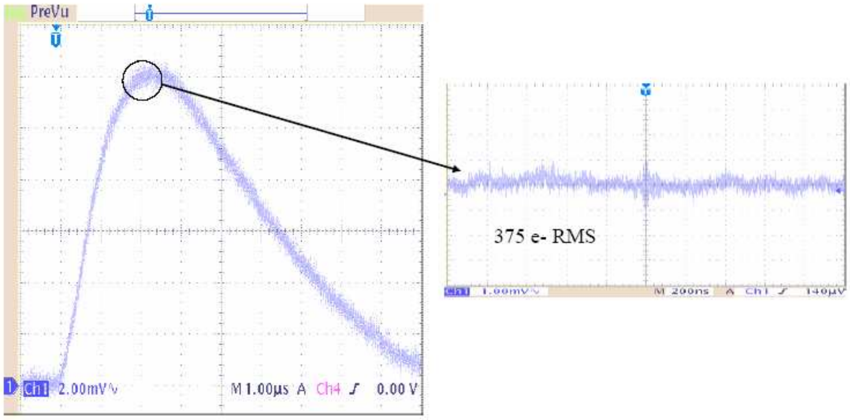

Figure 4. Preamp + Shaper noise (wire-bonded on card)

5.3 Sample and Hold and comparator

Sample and hold works as expected. On the comparator, the threshold voltages spread of the inputs transistors, of the order of 5 mV, is due to transistors sized too small. Size has been increased from 10/0.5 to 200/10 in the 0.13 μm version.

5.4 Tests conclusions

The UMC 0.18 μm CMOS process from UMC looks quite mature and reliable. Models are accurate, only one transistor failure on untested chips (Multiproject run), process spreads are of a few per cent only. The preamplifier is almost according to specs, the shaper is somewhat more noisy than expected, but matches simulations, the threshold voltages spreads problem is understood. First prototype run delivered functional chips in a relatively new (in our field) Deep Sub-Micron CMOS technology. These results are considered as very encouraging.

6. Next designs

0.13 μm CMOS is now available from Europractice. A cooperation between LPNHE and LAPP (Annecy le Vieux) has already started. A strong support was provided by IMEC (Leuven, Belgium) to run the UMC design kit and provide technology information. Access

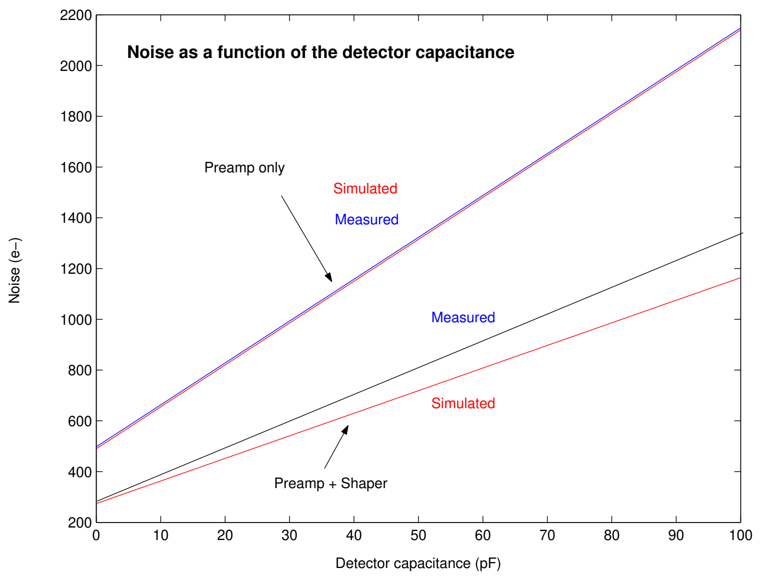

Figure 5. Noise summary

to other technologies is envisaged as well with CERN (A. Marchioro and co-workers), in the mainframe of the EUDET European FP6 project. The motivations for 0.13 μm are the following:
- This VLSI technology will be dominant in the industry in a few years.
- It is basically faster and lower power consuming (in particular for the digital)
- Some drawbacks that can be overcome for the analog.

After sending a 4-channel version in 0.13 μm including preamplifier and shaper, sampler and analog pipe-line and ADC, depending on tests results, a 128-channel is foreseen to be sent fall 2006 including digital: chip control (state machine), buffer memory (FIFO), calibrations LSQ estimations, centroids and power switching.

7. Conclusions

A CMOS 0.18 μm chip has been tested, the results are very encouraging. A test chip in CMOS 0.13 μm has been submitted end April 2006 including a full chain up to the AD converter. In addition, 0.18 μm and 0.13 μm chips beam tests are scheduled at DESY and CERN. Design for 128 channels is scheduled for the end of 2006.

References

[1] A. Savoy-Navarro. New Developments of the R&D SiLC Silicon Trackers. These Proceedings.
[2] J-F. Genat, A 16-channel Silicon Strips readout Chip in 180nm CMOS technology. 2005 ALCPG & ILC Workshops, Snowmass, CO USA, 14th-17th Aug 2005, To appear in the Proceedings.
[3] W-E. Cleland and E-G. Stern. Signal processing considerations for Liquid Ionisation Calorimeter in a high rate environment. Nuclear Instruments and Methods A, Vol 338, 1994, pp 467-497.