Status on the Development of FE & Readout Electronics for Large Silicon Trackers

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Forthcoming collaboration with CERN (Alessandro Marchioro et al, EUDET)

LCWS06, March 9-13th, Bangalore, India

Outline

- Silicon strips detector context
- On-detector Electronics
- 180nm CMOS readout chip
- Tests results
- Design in 130 nm
- Next ...

Silicon strips detector context

Silicon strips detector numbers

- 4-10 10^6 Silicon strips 10 - 60 cm long
- Readout Pitch 50-100 μm DC or AC coupled
- Occupancy defined as % channels hit per BC:
  Outer barrel and end caps layers: < 1 %
  Inner barrel and end caps layers: < 5 %
- ILC timing: 1 ms: bunch: 150-300ns / BC
  200ms in between

Detector data

- Pulse height: Cluster centroid to improve position resolution to O(μm)

  Detector pulse sampling 5-10 samples 8-10 bit A/D (Wilkinson)
  stored in an analog buffer

- Time: Two scales:

  - Coarse 150-300ns BCO tagging

  - Fine nanosecond timing for coordinate along the strip
    and fine BCO tagging for some regions

  Not to replace another detector layer or double sided detector,
  but give an estimation to a few cm

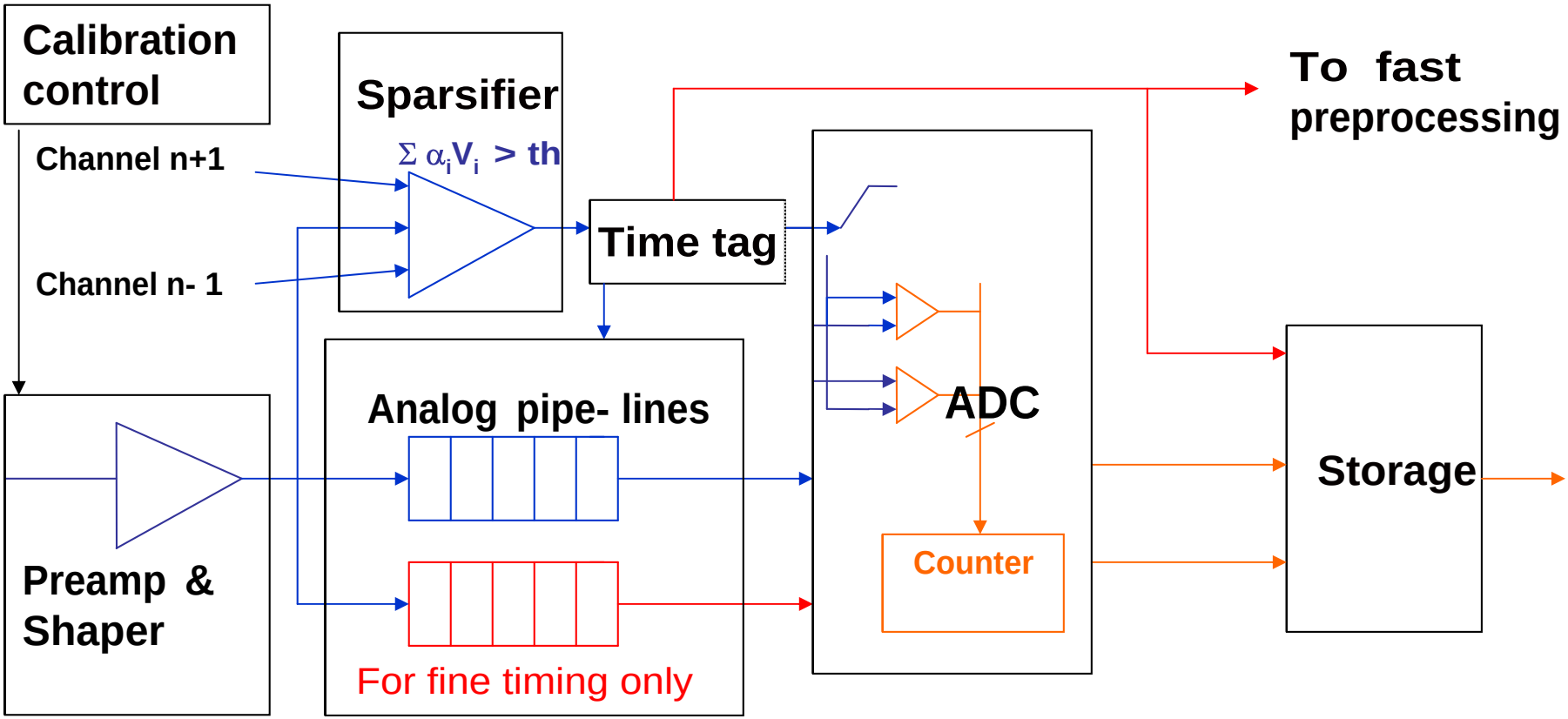
On-detector Electronics

Jean- Francois Genat, LCWS06, March 9- 13th, Bangalore, India

On-detector FE chip

- Pulse sampling: 5-10 samples over 2 shaping times
- Buffering: 8-deep 2D analog buffer (8*5-10 samples cells) per channel
- Analog-Digital conversion: Wilkinson optimum (SVX architecture)
- Sparsification/calibration : Integrated on detector FE chip
- Digital processing: Amplitude and time estimation + charge cluster algorithm
- Power: 1/200 ILC duty cycle: FE Power cycling

Front-end architecture



Charge 1- 40 MIP, S/N~ 15- 20, Time resolutions: BC tagging, fine: ~ 2ns

Present technologies - Deep Sub-Micron CMOS
UMC 0.18 μm, 0.13 μm

Time-stamping on all layers
fine time resolution
on some layers

Charge measurements Expected

- Preamp + Shaper
  Gain: 20mV/MIP over 1-30 MIP
  Noise: CMOS 180 nm: 280e- + 10.5e-/pF @ 3 μs
- Analog buffer
  8-deep (cells of 5-10 100 fF caps)
- Sparsifier
  Threshold an analog sum of 3 adjacent channels after pulse shaping
- ADC
  10-12 bits
  Clocked at 96 MHz
- Signal-Noise ratio
  The larger, the best ! 15-20 ?

Time measurements Expected

- Time stamping

  Order of 30 to 50 ns
  Time-stamp the sparsifier output at 4 * BCO clock (12 MHz)

- Fine time measurement

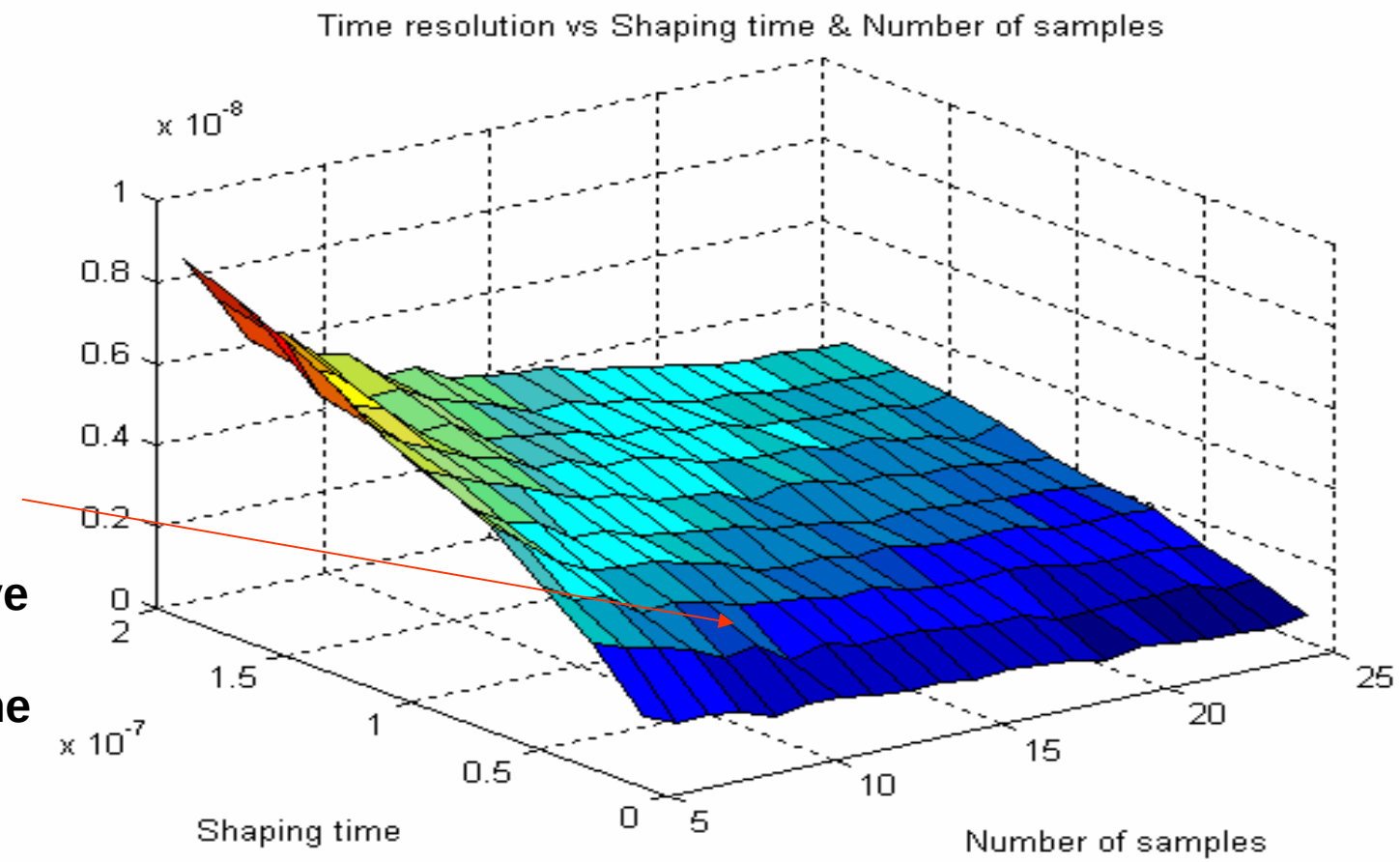
  Order of 1 to 3 ns
  32 * BCO on chip interpolated clock sampling (PLL @96 MHz)
  Use digital processing over 5-10 digitized samples

Expected fine time resolution

Simulated (JFG) time resolution using a model of the whole electronics readout chain from preamplifier to the analog sampler (ideal A/D) using least square fit algorithm (William Cleland)

- **S/N =25**
- **8 samples**
- **50 ns shaping**

→ **1.8 ns time resolution**
(will still improve with actual time distribution in the detector)



SiGe technology

Overall Noise Contributions

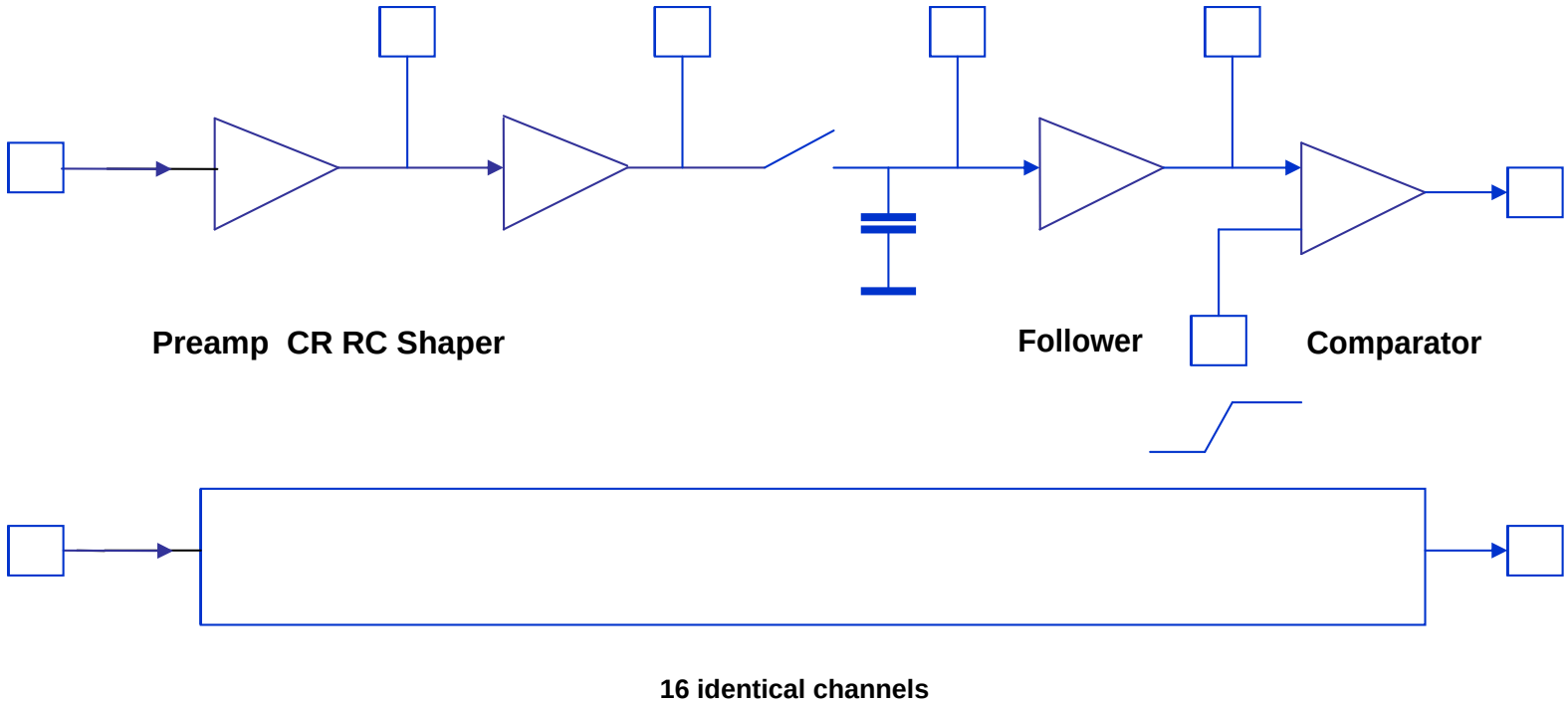
Source	**Value**	**Noise 180nm CMOS**
Input stage (measured)	g_m=0.7mA/V	615 e- (measured)
Detector leak	10 nA	588 e- (from literature)
Biasing resistor	10 MΩ	423 e- (thermal noise)
Total		950 e-

Foreseen overall ENC contributions at 30 pF detector capacitance and 3 μs shaping time:

- CMOS 180 nm: S/N ~ 20
- CMOS 130 under investigations

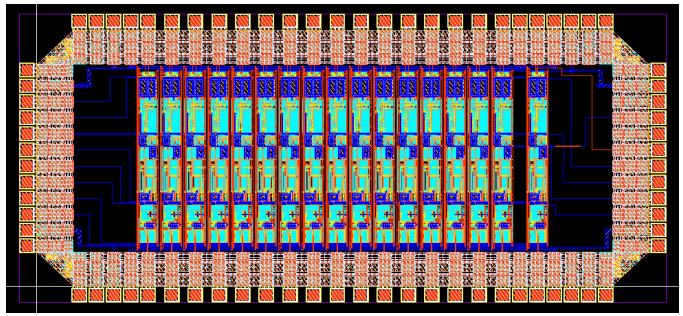
CMOS 180nm Chip

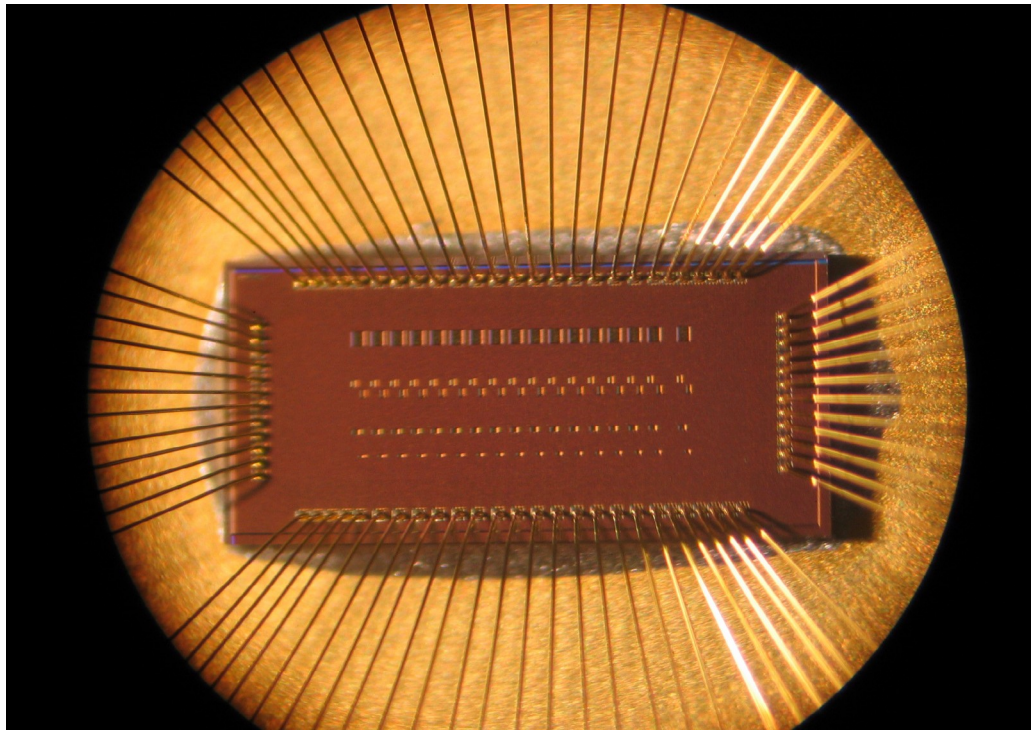
Front-end test chip in CMOS 180nm



- Low noise amplification + pulse shaping
- Sample & hold
- Comparator

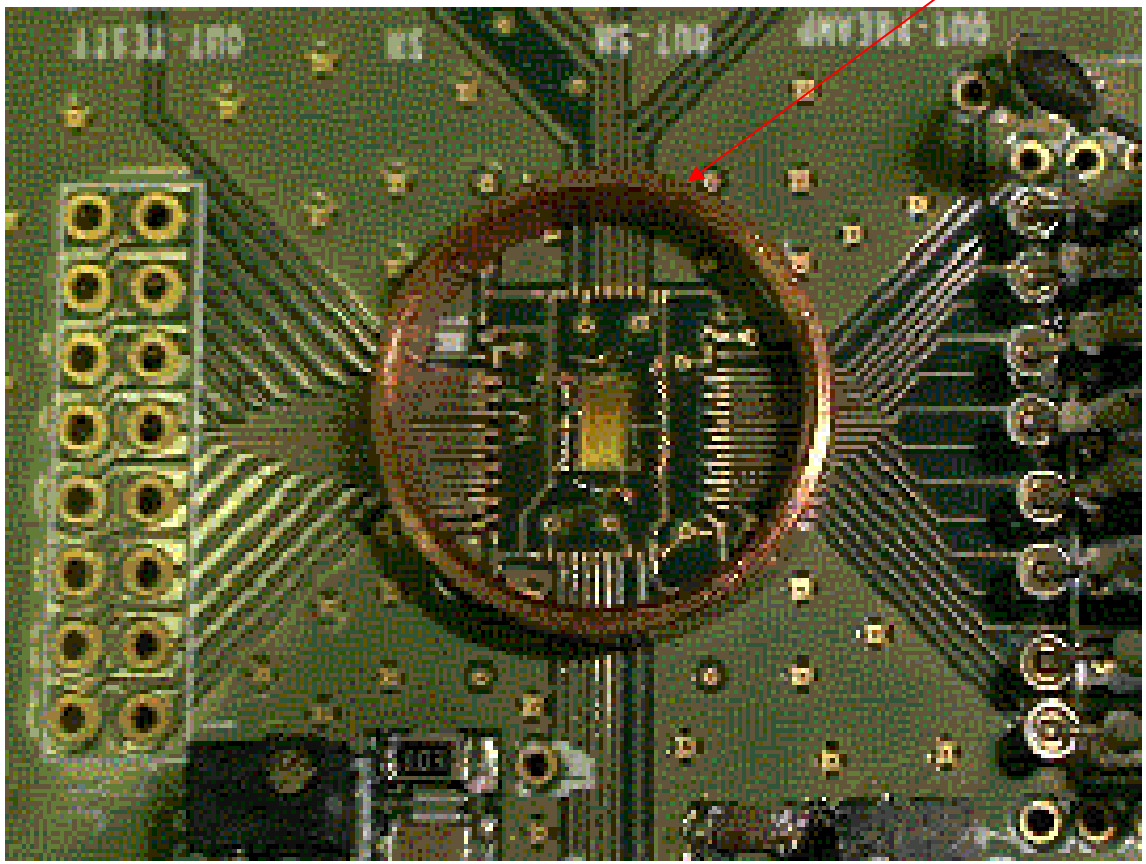
Silicon





16 + 1 channel UMC 0.18 um chip (layout and picture)

Tests Results



Chip wired-bonded on board

Preamp tests results

12 chips tested.

One failure: On chip # 8, comparator does not work.

Preamp:

- Gain: 8 mV/MIP OK
- Linearity: +/-1.5% +/-0.5% expected

  Transistor used as a resistor

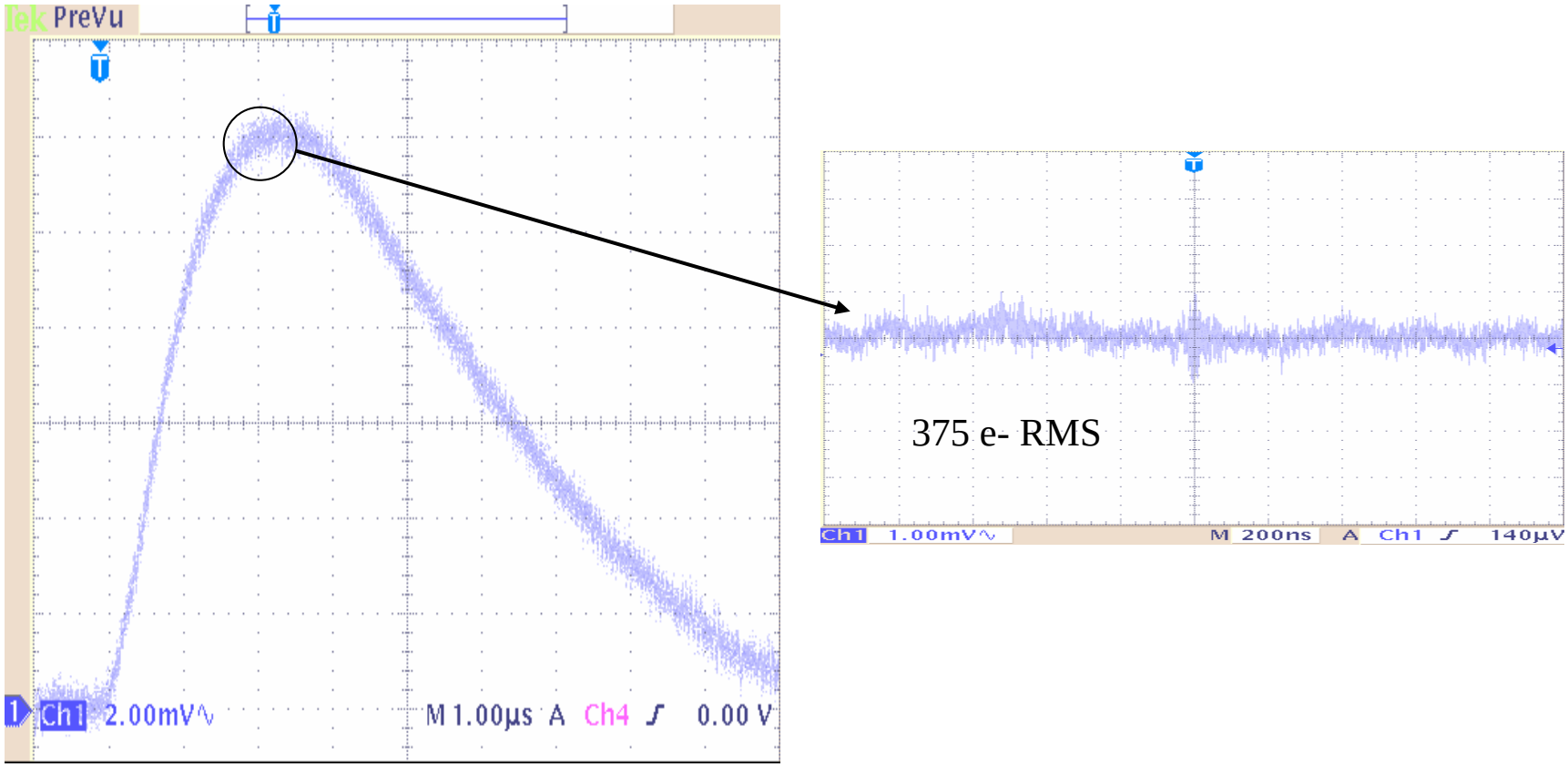
  non linear with voltage

- Dynamic range: 50 MIP 90 expected, but within specs
- Noise @ 70 μW power, 3μs-20μs rise-fall times:

  498 + 16.5 e-/pF 490 + 16.5 e-/pF expected

  OK

Shaper Noise (wired-bonded on board)



375 e- input noise with chip-on-board wire-bonding (against 280 simulated)

Shaper tests summary

Shaper: - Peaking time:

2 - 6 μs tunable peaking time 1-10 targeted

- 6 MHz bump (~ 650 e- added noise)

Not in simulations

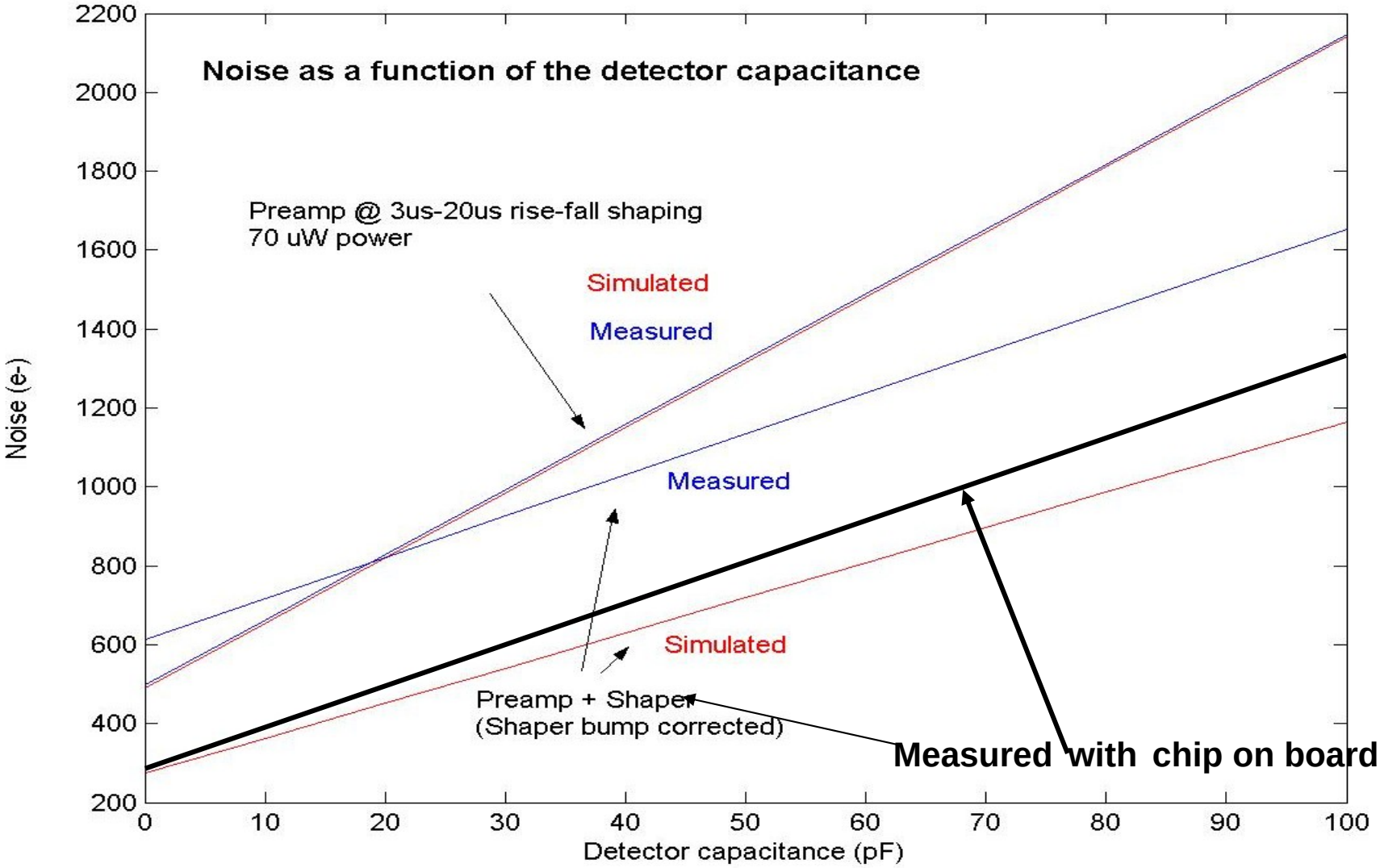
Shows up in simulations at 10 pF load (actual is 1 pF)

- Noise @ 3 us shaping time and 70μW power:

375 + 10.4 e-/pF 274 + 8.9 e-/pF expected

Noise summary

good agreement with expected values



Sample & Hold Comparator

- Sample and hold: OK
- Comparator:

Vt spreads of the order of 5 mV due to transistors sized too small

- Increase input transistors size from 10/0.5 to 200/10
- Increase Preamp + Shaper voltage gain from 8 to 25 mV/MIP

Tests Conclusions

12 chips tested

The UMC CMOS 180nm process looks quite mature and reliable:

- Models OK
- Only one transistor failure
- Process spreads of a few %

Preamplifier: almost according to specs

Shaper: a bit more noise than expected but OK with simulations

Comparator: V_t spreads understood

First proto delivered functional chips in a relatively new (in our field) DSM technology.

Encouraging results regarding CMOS DSM

Next designs

Front-end in CMOS 130nm

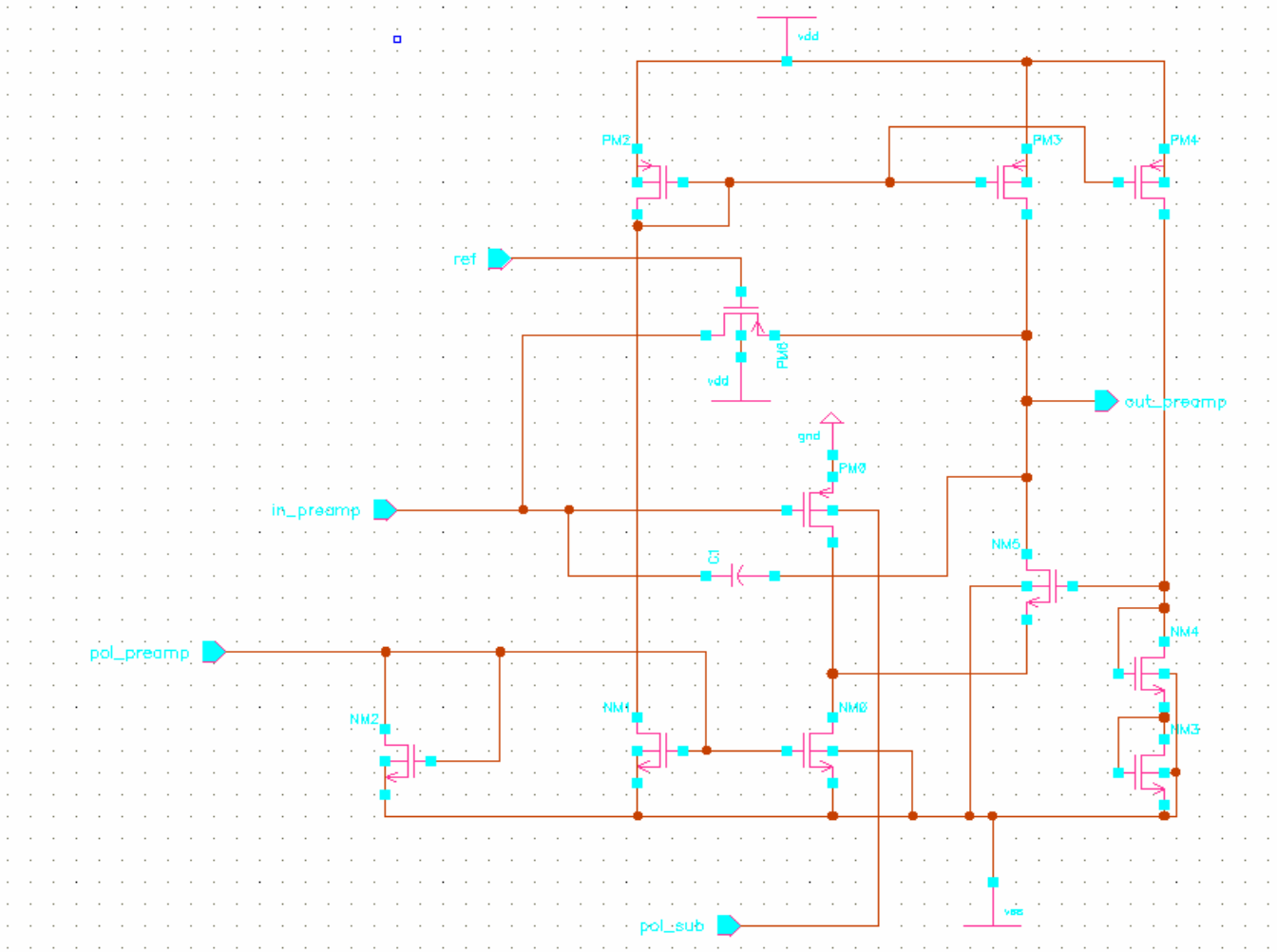
Cooperation between LPNHE and LAPP Annecy and soon with CERN (A. Marchioro et al., EUDET)

Why 130nm ?

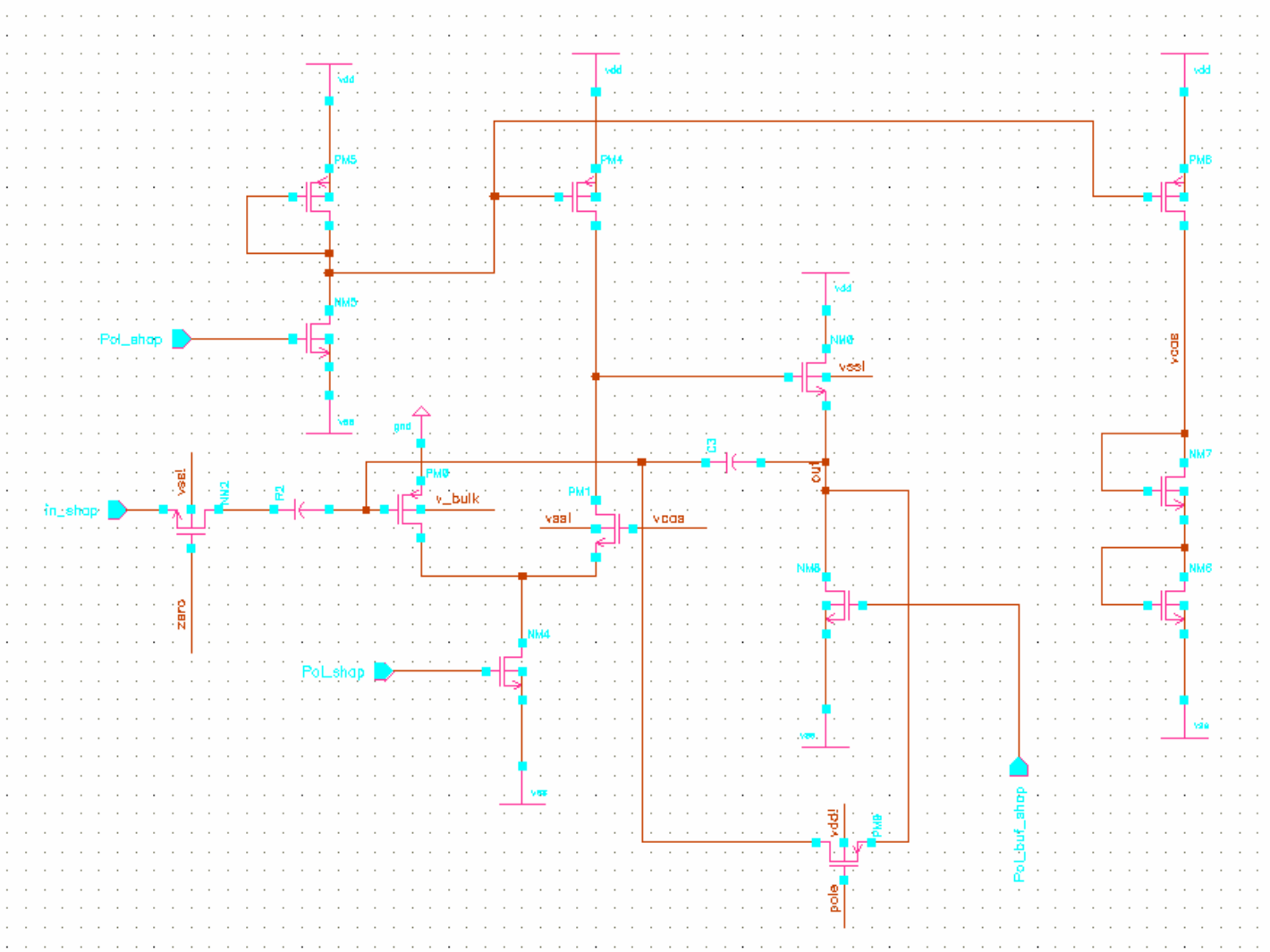
- VLSI
- Will be dominant in industry in the next few years
- Faster
- Lower power

Drawbacks for low noise analog design

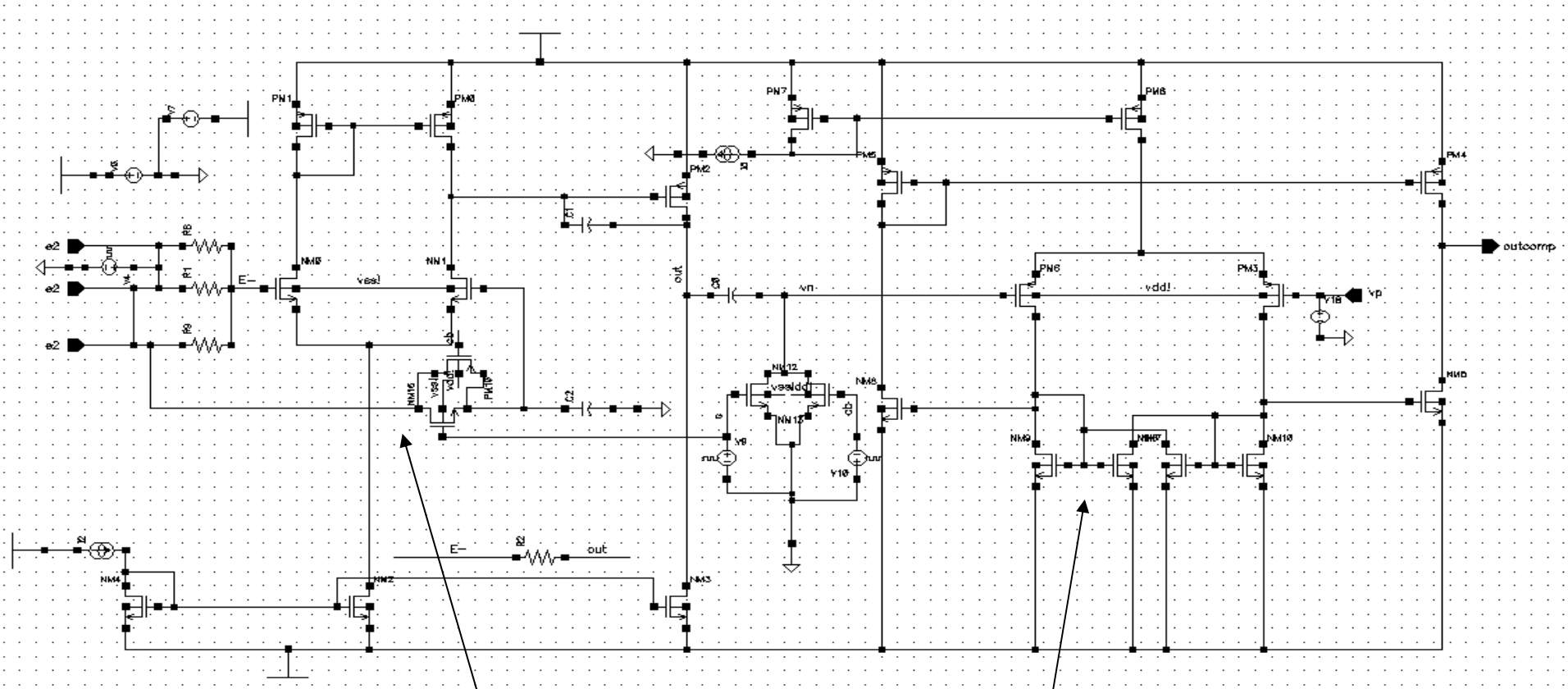
Preamp in 130nm



Shaper in 130nm



130nm Sparsifier



- Sum of adjacent channels
- Offset cancelled Threshold detection

130nm plans

130 nm technology available end 2005 from Europractice

- Submit a 4 channel version end April 2006 including:

  - Preamp + Shaper
  - Sampling and analog pipe-line
  - ADC
  - Power cycling

Then, depending on tests

- Submit a 128 channel version end 2006 including digital

Front-End Digital in 130nm

- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
- Tools
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/ Verilog
  - SRAM memory
  - PLLs

Conclusions

- CMOS 180nm chip tested, very encouraging results
- CMOS 130nm underway, include:

  Preamps + Shapers
  Analog pipe-lines
  Sparsifiers
  ADC
  Power cycling

  Submission end April 2006

- 180 and 130nm chips beam tests scheduled (DESY, CERN)
- Plans for 128 channels