# R&D towards a TPC at ILC
## (TPC readout for Heavy Ion collisions)

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Family of ASICs originally designed for Heavy Ion collisions and ALICE TPC

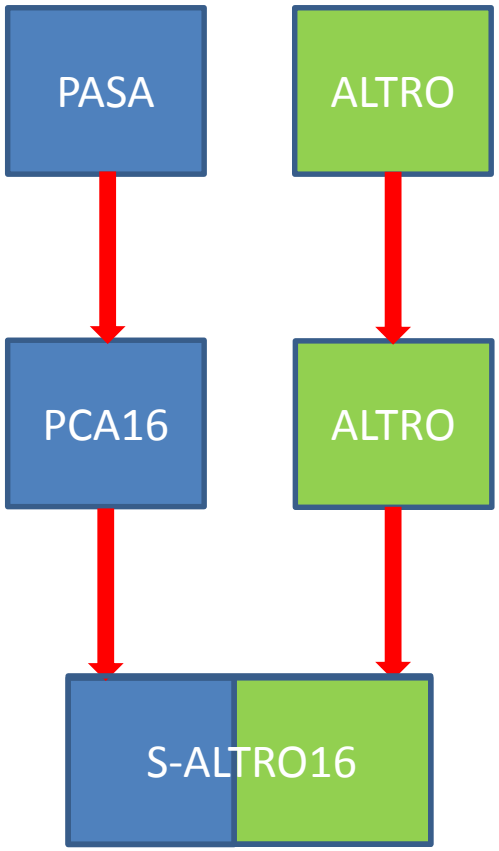
Special considerations
High multiplicity
- high filling factor >10% of samples are non-zero
- many tracks close by
- many tracks crossing

# Development history (>10 years)

ALICE:
+ polarity
12mV/fC
190ns

EUDET:
+/- polarity
12,16,20,27mV/fC
30,60,90,120ns

AIDA:
+/- polarity
12,16,20,27mV/fC
30,60,90,120ns




ALTRObus
40 bit wide parallel bus
@40MHz

Many tests on real chamber

Only tested on the bench

# Driving forces for LCTPC

High PT physics

High demands on momentum resolution

- Long tracks Large TPC
- High B-field (4-6T)
- low diffusion – narrow pads
- 300-400 coordinates along track

Nearby track resolution important (as for ALICE but other reason)

End up with 2-5Mchannels

Readout:

Linear colliders have poor duty factor (ILC, 5 spills of 1ms per second)

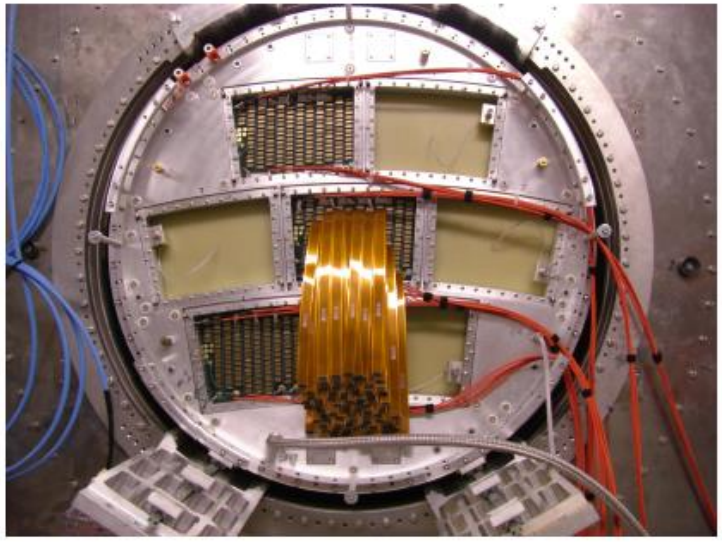
- contiuous untriggered readout but
- storage of full spill (10 times event memory depth)
- readout between spills.
- **Power pulsing**

# The EUDET system:

General purpose readout electronics for ”proof of principle” tests.
Test different TPC-readout concepts.

GEM, Micromegas.....

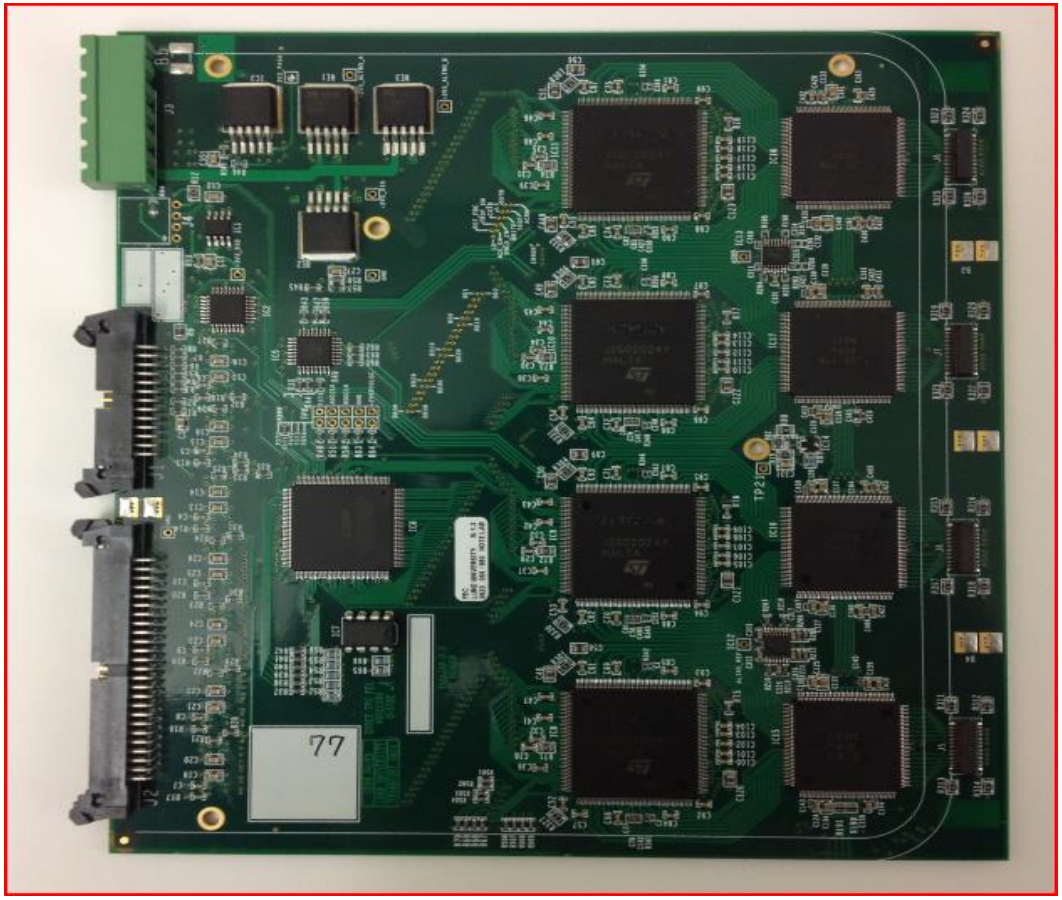
10000 channels procuced  PCA16 + ALTRO



End plate of large prototype TPC

35cm long Kapton cables
1*5.2mm$^2$ pads

# 128 ch FEC, PCA16 + ALTRO



EUDET front end electronics, 128ch FEC

20MHz sampling rate

# SALTRO16

## CHIP dev:

**Luciano Musa … S-Altro Specifications and Architecture**
**Hugo França-Santos … ADC (PhD Thesis, Lisboa)**
**Eduardo Garcia… Digital Signal Processing & Control (PhD Thesis, Valencia)**
**Massimiliano De Gaspari … Front-end, Integration, Tests (PhD Thesis, Heidelberg)**

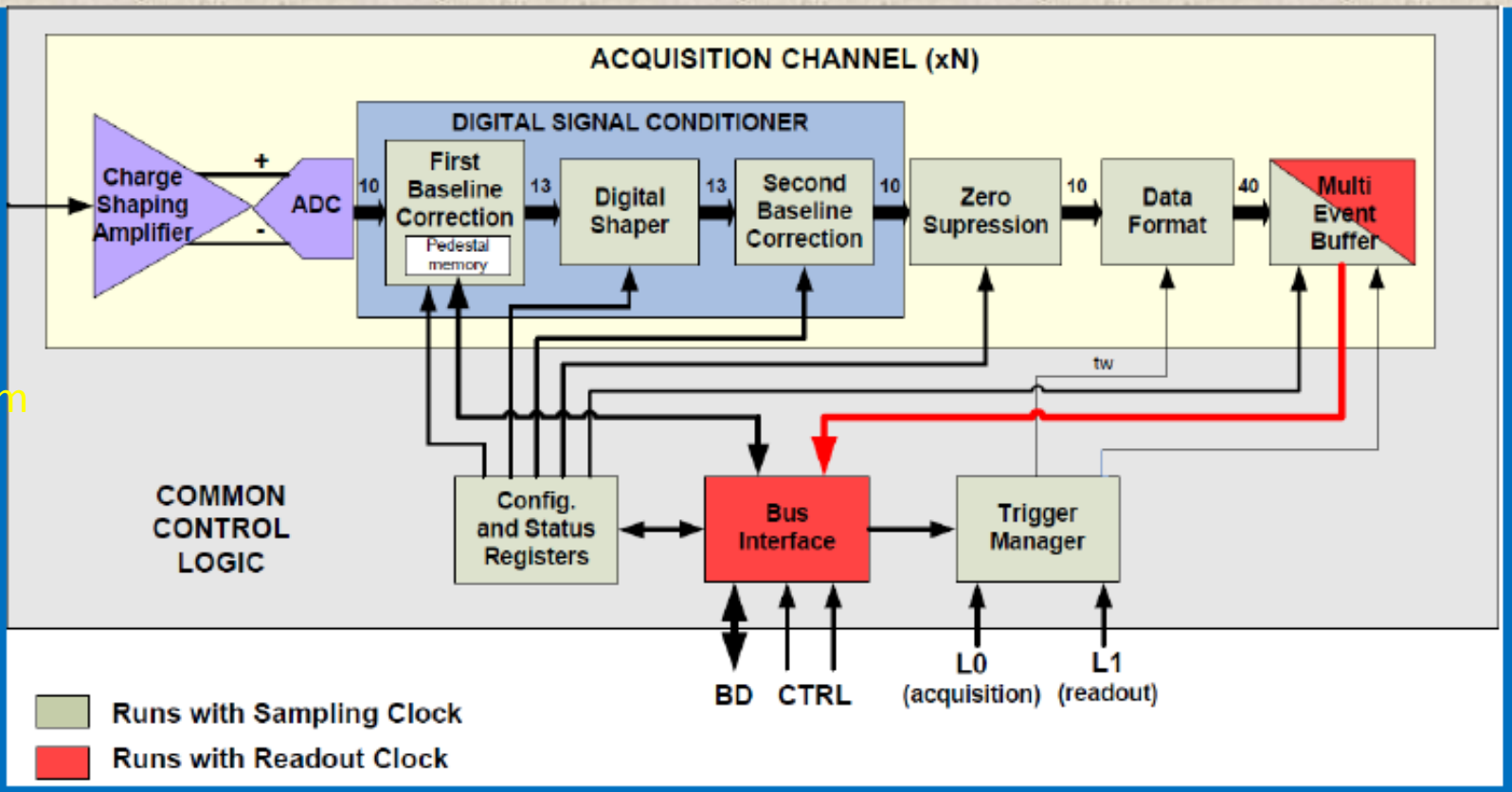
## Main use, LCTPC R&D:

**Readout system based on S-ALTRO16 for TPC protoytping for ILD**

**Financing from EUDET – AIDA2020 brings it all together**

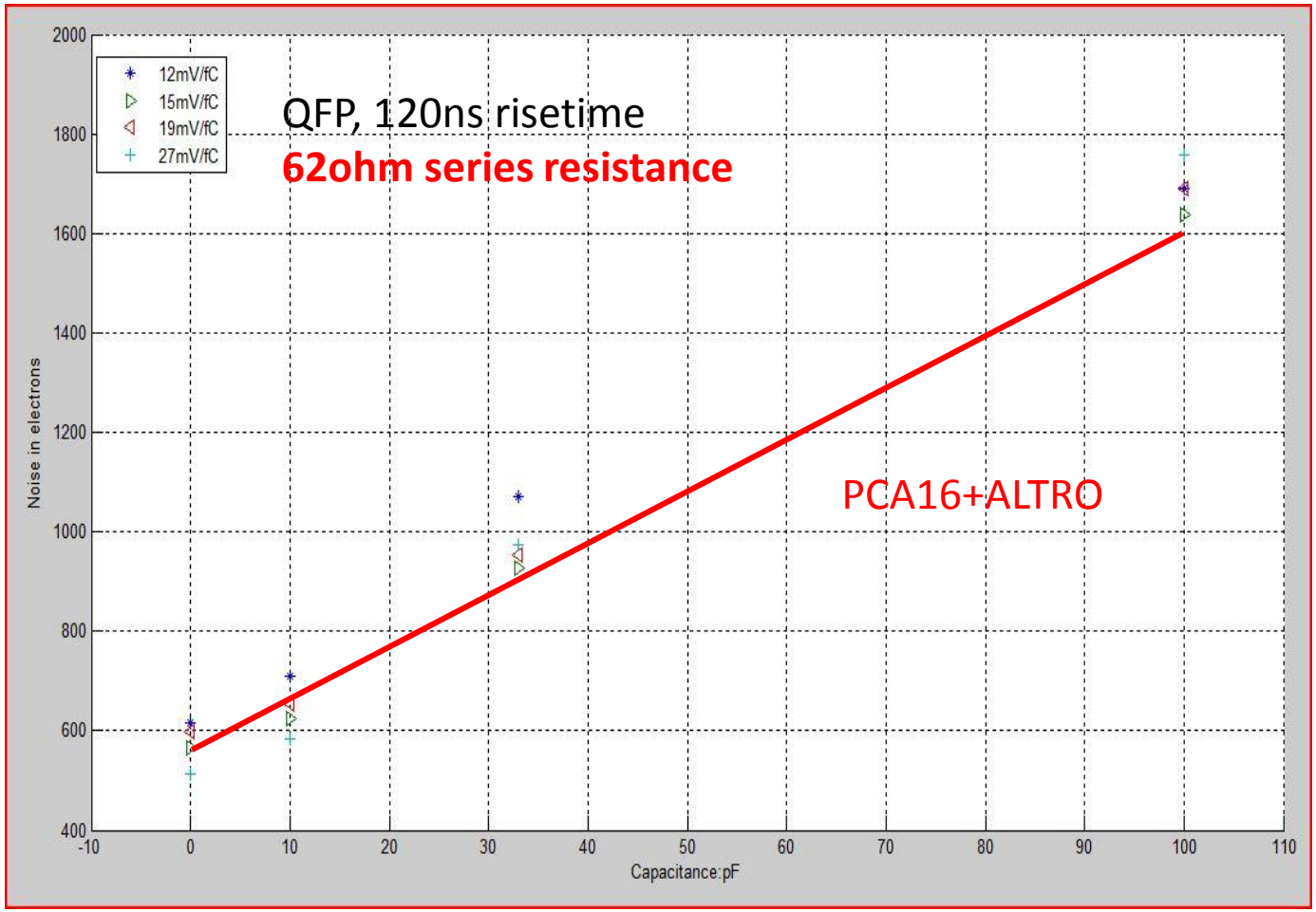
# System architecture

0.13µm
CMOS
IBM




**Level 1: Starts the data acquisition.**
**Level 2: Validates data from previous L1.**
**BD : 40 bit bidirectional bus; 20 bits address + 20 bit data.**
**CTRL : 6 bits.**
**Sampling clock : max 40MHz. Readout clock : max 80MHz.**

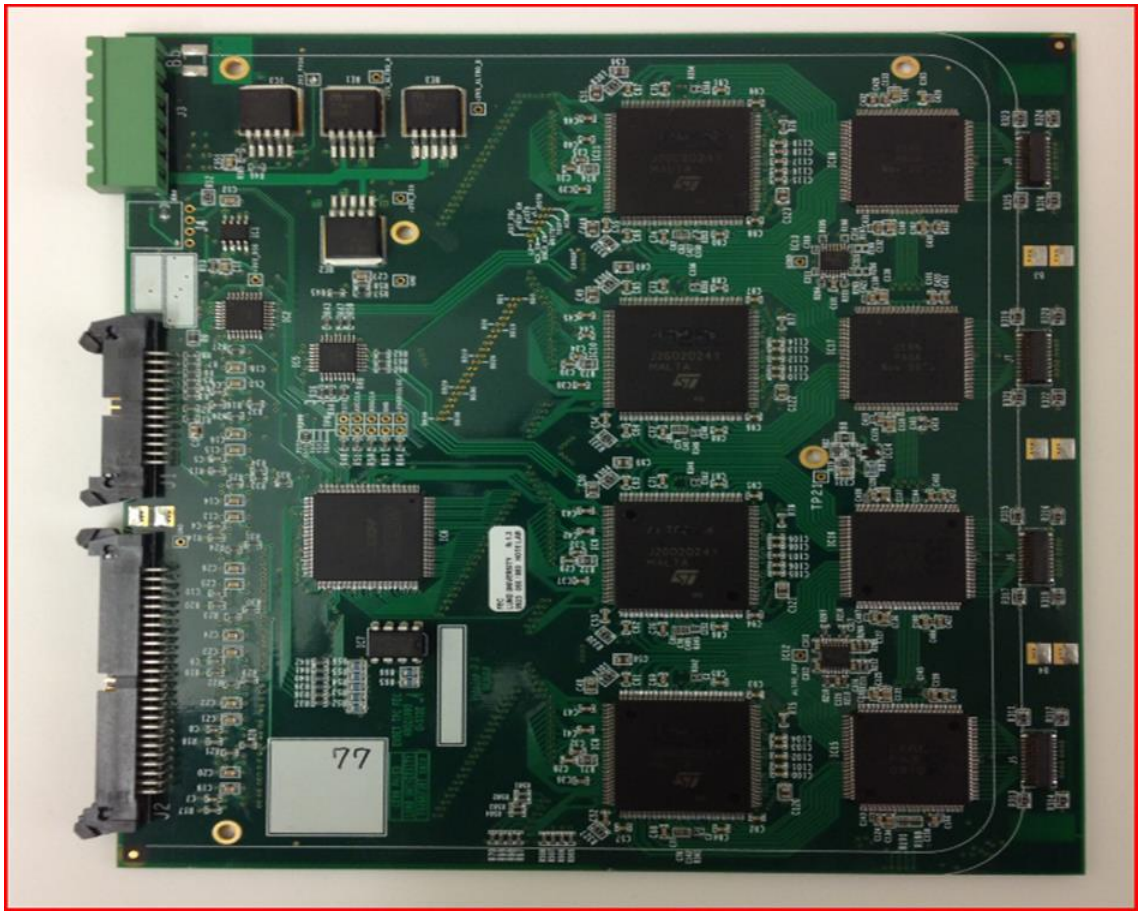
# SALTRO16 noise in electrons




Additional capacitance

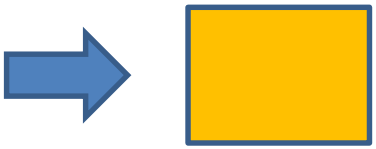
Integration digital/analog succesful

# Massive Miniaturisation needed



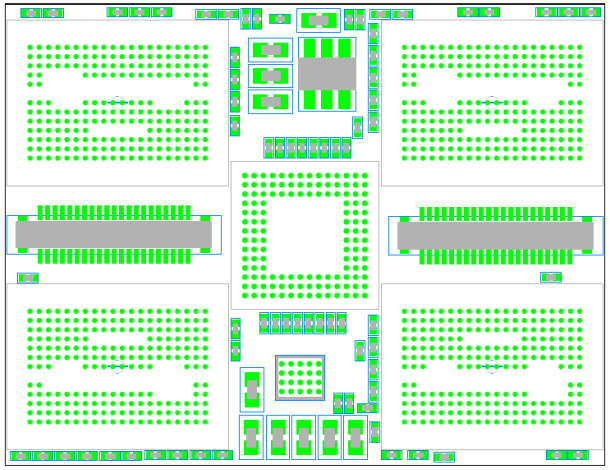
With present chip-set

Only R&D funding

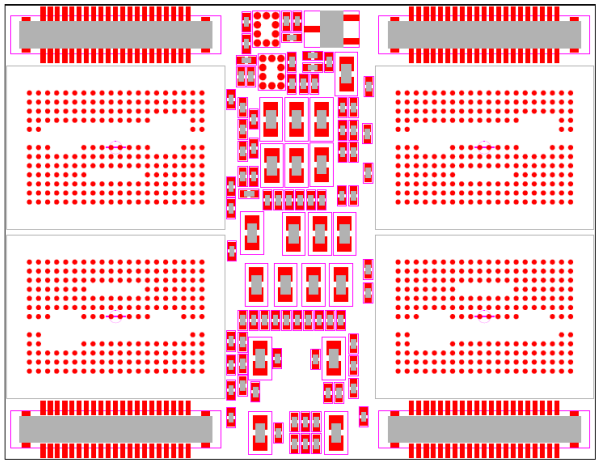


# Assemble MCM with 8 SALTRO16 in BGA

Top side



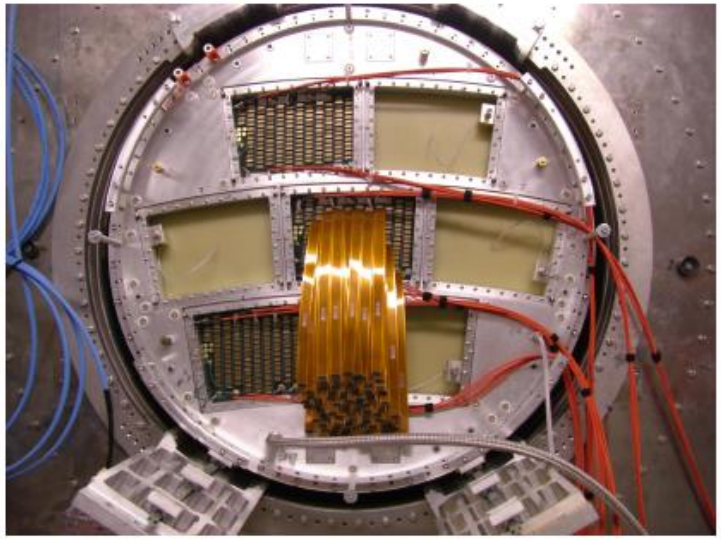
Below side



Can not use ALTRObus for readout. Do  parallel-serial-parallel by CPLD on MCM

# How small it has to be

4 MCM on a VISA card



# SALTRO16 system for R&D

SALTRO16 is very versatile and ideal for R&D

- selectable polarity
- Gain 12-27mV/fC, shaping 30-120ns
- Sampling up to 40MHz
- compact with new MCM-allows 7mm$^2$ pads

but

- Old design
- 40 bit parallel bus
- only 16 ch per chip

So unlikely to be manufactured in larger quantities.
Not the final soluiton for ILD

# The SAMPA chip for ALICE TPC GEM upgrade

Development - Sao Paolo
Same functionality as SALTRO 16
32ch per chip (can hardly be increased)
Selectable:
- 4mV/fC, 20mV/fC, 30mV/fC selectable gain
- polarity
- shaping 160ns or 300ns

serial links out – 11 links at 320Mbit/s
Triggered mode (as before)
Continuous readout of 10MS/s sampling rate (the upgraded TPC way)

First full chip prototype available  this summer

# Conclusions

- The SALTRO16 is unlikely to be a solution for the future
- But it is great for R&D, when small pads are needed
- SAMPA gets ready timely

**Important Question!**

Are chips designed for very high occupancy in Heavy Ion collisions optimal for low rate -- Low multiplicity experiments

To digitize everything up front will give the worlds best measurement of zero at the cost of chip area (€€€€) and power.

A TPC at ILC has high demands of 2-track resolution. Digitization of everything up front may be worth the effort.

Neutrinos, NNBar at ESS and other low rate low track density exps, maybe a step back to analog multiplexing is more optimal

backup

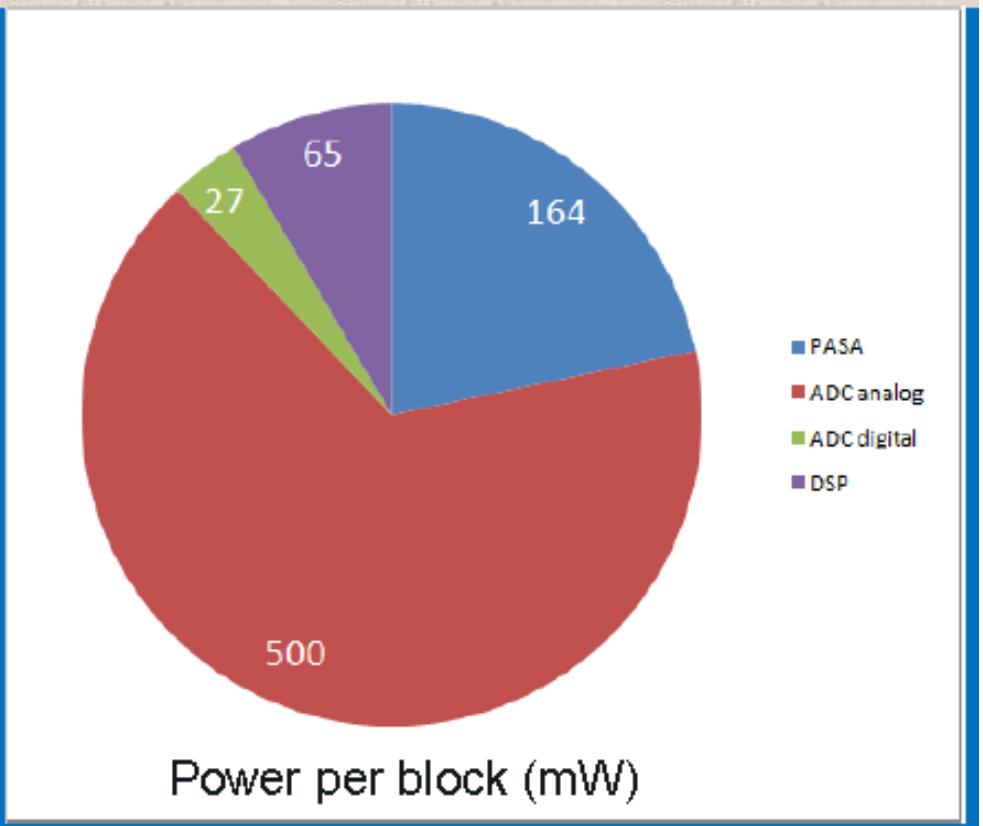
# Noise summary

| | Config | 120ns L 12 | 120ns L 27 | 30ns L 12 | 30ns L 27 | 120ns H 12 | 30ns H 12 |
|---|---|---|---|---|---|---|---|
| PGA3 Inp nc | Noise LSB | 0.480 | 0.655 | 0.526 | 0.683 | 0.498 | 0.504 |
| | Noise fC | 0.088 | 0.051 | 0.103 | 0.059 | 0.092 | 0.100 |
| | Noise e- | 547 | 316 | 641 | 370 | 574 | 625 |
| PGA4 | Noise LSB | 0.709 | 1.346 | 1.475 | 3.263 | 0.668 | 1.279 |
| | Noise fC | 0.129 | 0.104 | 0.287 | 0.283 | 0.123 | 0.254 |
| | Noise e- | 809 | 649 | 1796 | 1768 | 770 | 1587 |

Measured noise averaged over 16 channels

# Power consumption

| | 40MHz operation | Smart shutdown |
|---|---|---|
| PASA | 10.26mW/ch | 235uW/ch |
| ADC analog | 31.28mW/ch | 394uW/ch |
| ADC digital | 1.71mW/ch | ≈0 |
| DSP | 4.04mW/ch | 10.8uW/ch |




**Smart shutdown: shutdown control lines for PASA and ADC, clock removal for the DSP.**

**Total power consumption: 757mW.**

# Resolution in bend plane

## residuals

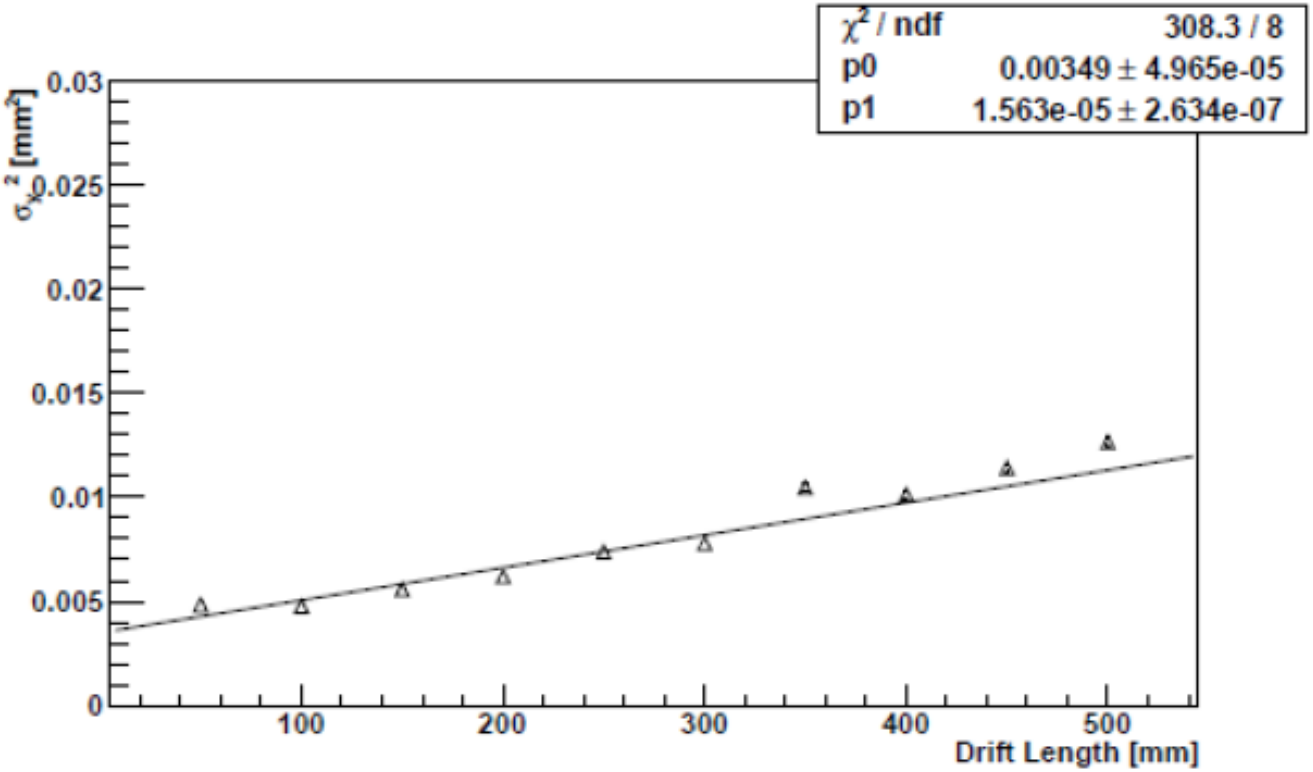
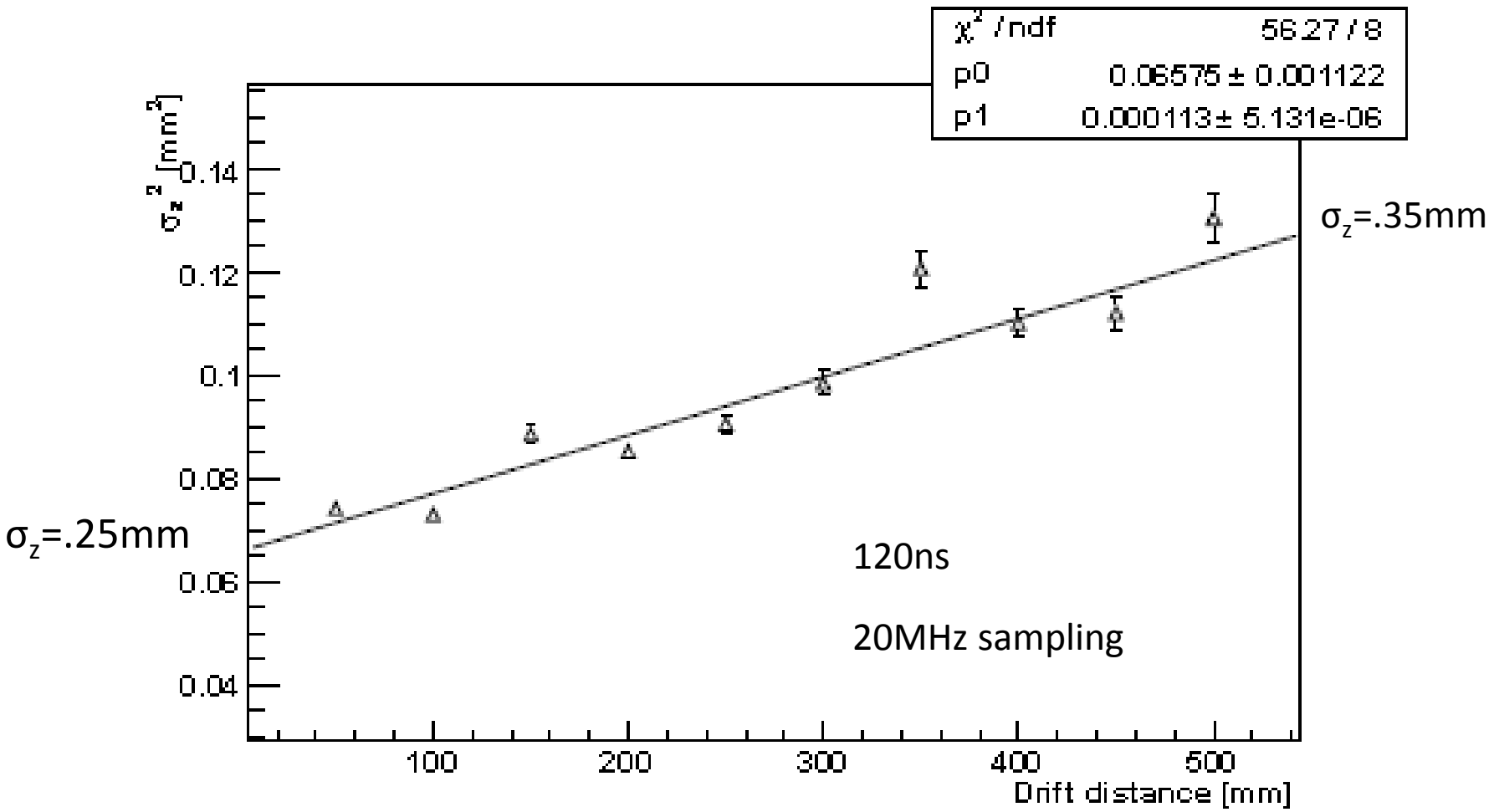



Figure: Measured resolution for different drift lengths. The line crosses the y-axis at 0.00349 mm$^2$ which corresponds to an intrinsic resolution of $\sigma_y(0) = 59.1 \pm 0.4\mu$m.

Slightly better now after field distortions fixed

# Residuals in drift direction



# Residuals in drift direction