

# Layout comparison of the SBDS5 vertical kicker

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# Overview

## 1. Introduction

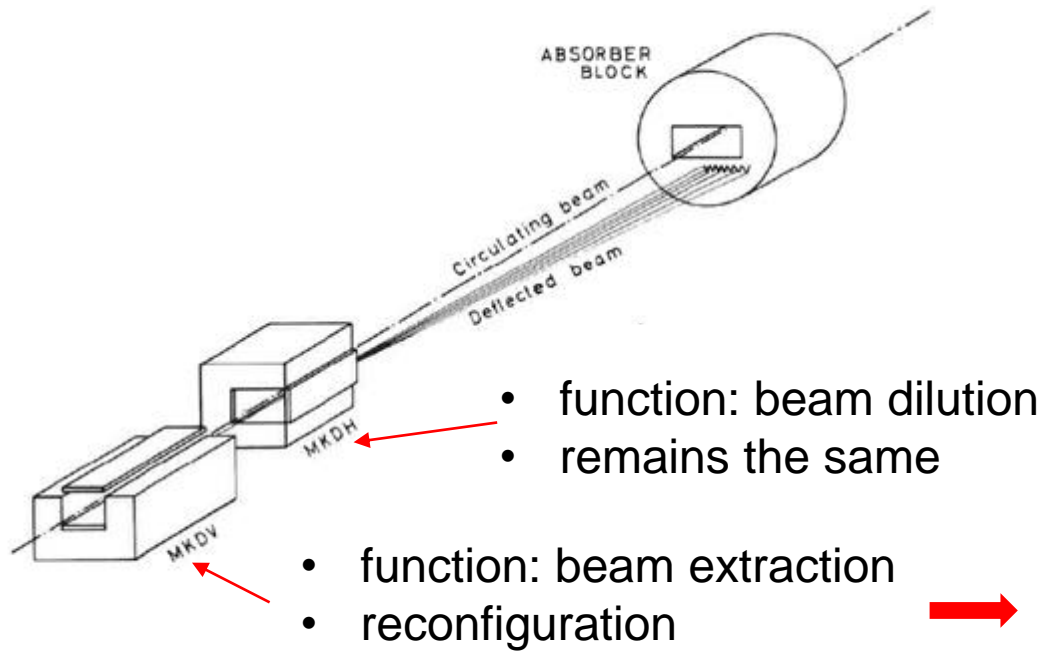
- Reason for layout comparison
- Introduction to the vertical kicker
- System failure modes

## 2. Fault Tree Analysis

- Different system failure modes
- Fault tolerant design
- Sensitivity of the results to the model parameters

# Upgrade vertical kicker

## Schematic drawing of the SBDS

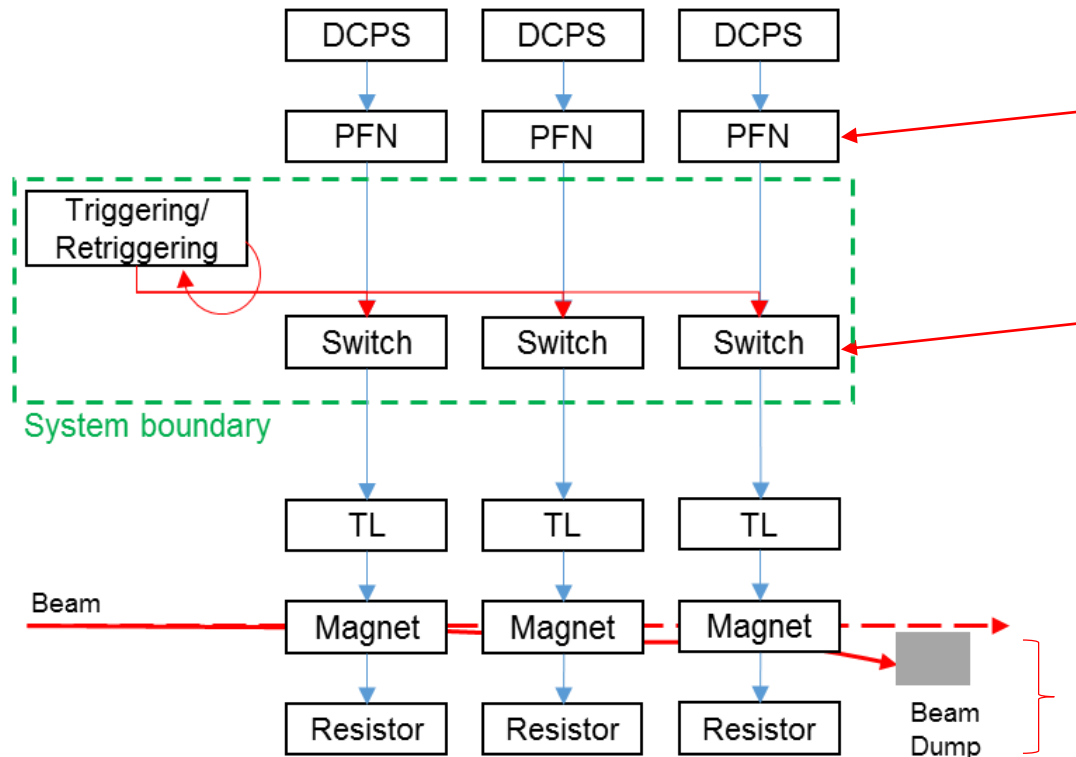


**→** focus of reliability study

## LHC Injectors upgrade

- SBDS movement from LSS1+ to LSS5
- Reconfiguration of the vertical kicker

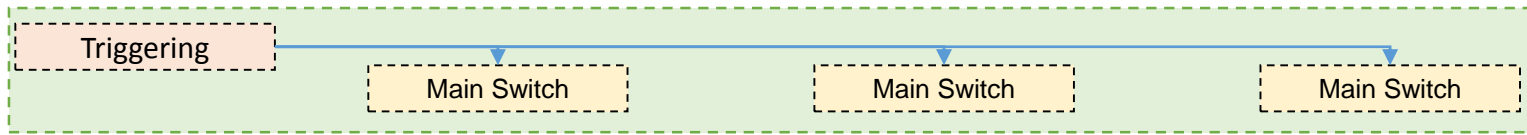
# Block diagram future vertical kicker



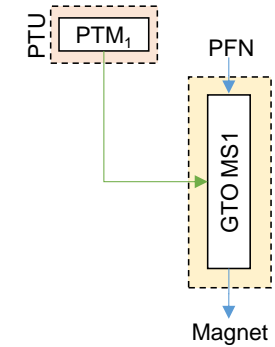
## Consolidation works

- Convert existing PFN from 3W to 2W
- Passive components
- replacement of thyristron by solid state switches: new design
- same design of magnet and TMR
- passive components

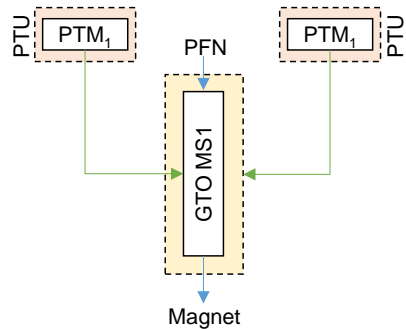
# Layout possibilities main switch and triggering



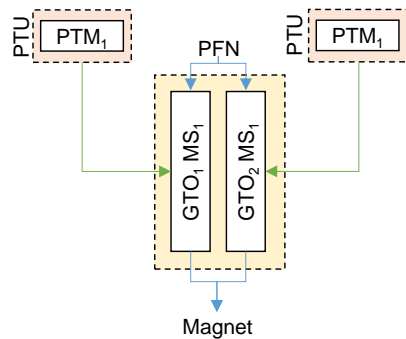
1 Stack per MS  
1 PTM per stack



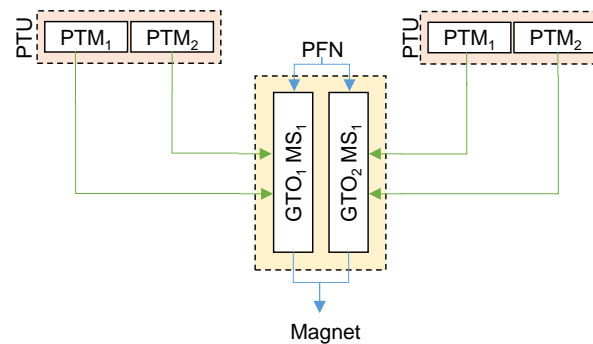
1 Stack per MS  
2 PTM per stack



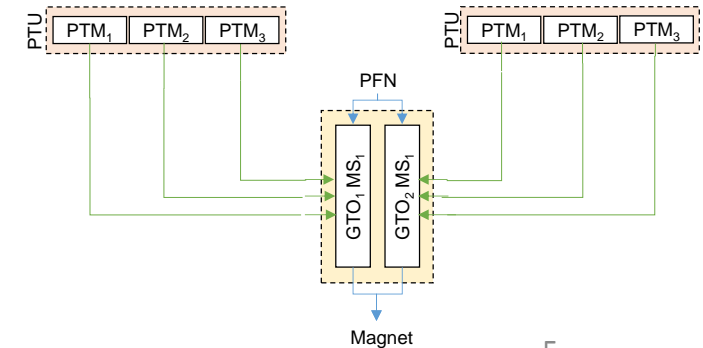
2 Stacks per MS  
1 PTM per stack



2 Stacks per MS  
2 PTM per stack

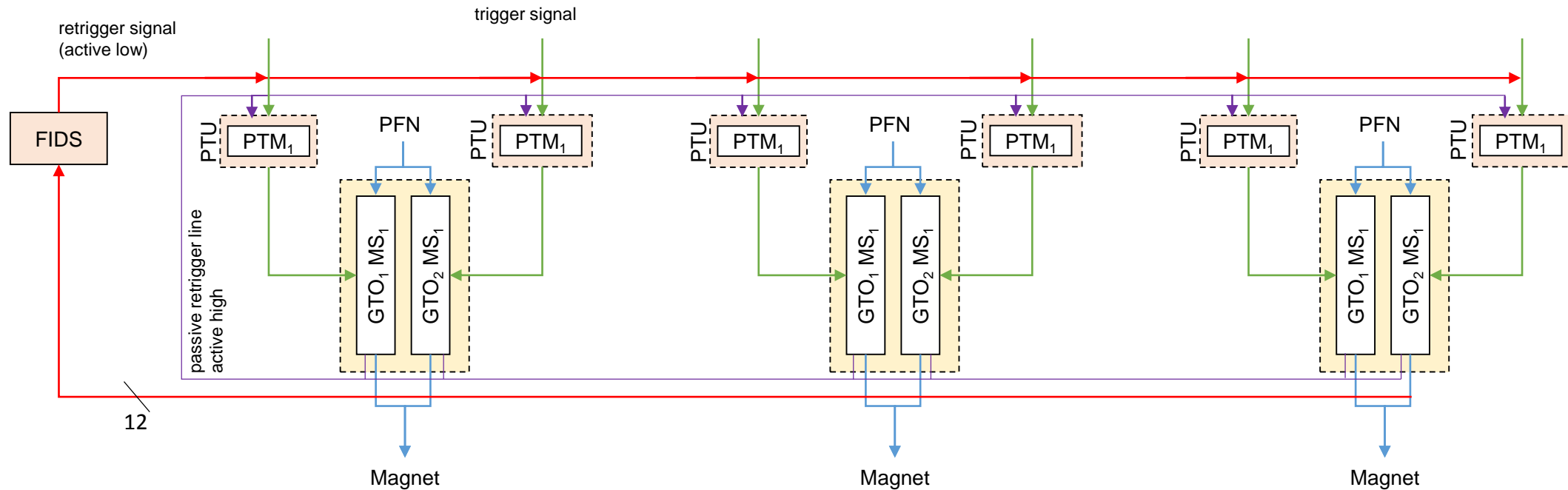


2 Stacks per MS  
3 PTM per stack



# Block diagram switches, triggering and retriggering

## FIDS and passive retrigger line: example layout 2 GTO; 2 PTM

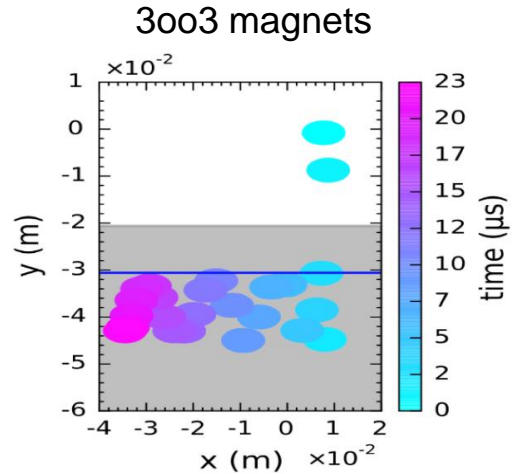


- trigger signal
- retrigger signal (active low)
- passive retrigger line (active high)

# System failure modes of the vertical kicker

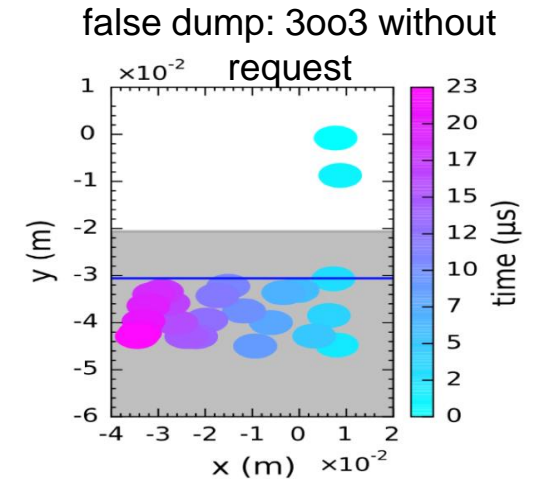
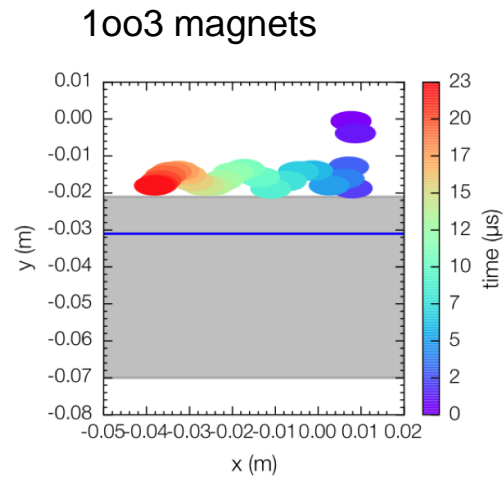
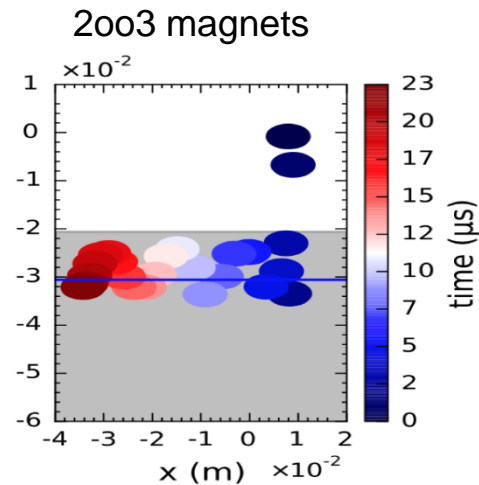
## Nominal:

- 3003 magnets after dump request



## Failure modes

- 2003
- 1003
- false dumps
- examined in Fault Tree



# FTA assumptions

## failure and repair scenario

- repairable system
- corrective maintenance:
  - failures are immediately revealed
  - repair or replacement begins immediately after failure, and when begun will require some time to complete
  - the repair restores the component to a state where it is essentially as good as new
- Exponential distribution for both the failure and repair processes

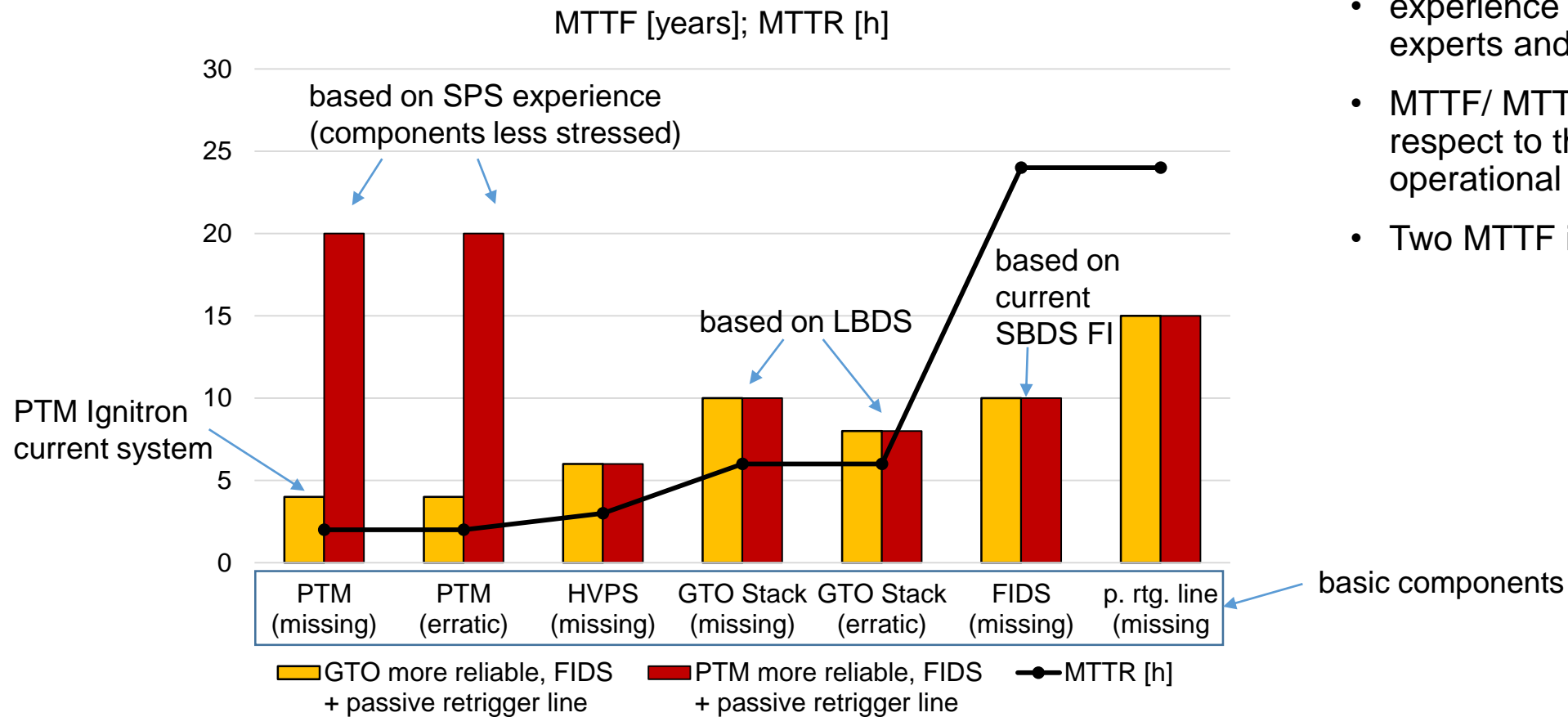
$$f(t) = \lambda * e^{-\lambda t} \quad \lambda(t) = \frac{1}{MTTF} = \text{const.} \quad \mu(t) = \frac{1}{MTTR} = \text{const.} \quad F(t) = 1 - e^{-\lambda t} \quad A_D^{(i)} = \frac{MTTF}{MTTF+MTTR}$$

## operational scenario

- operation from April – December, 24 hours a day
  - 6600 hours operation per year
  - 2 million pulses per year
  - 10 s cycle length

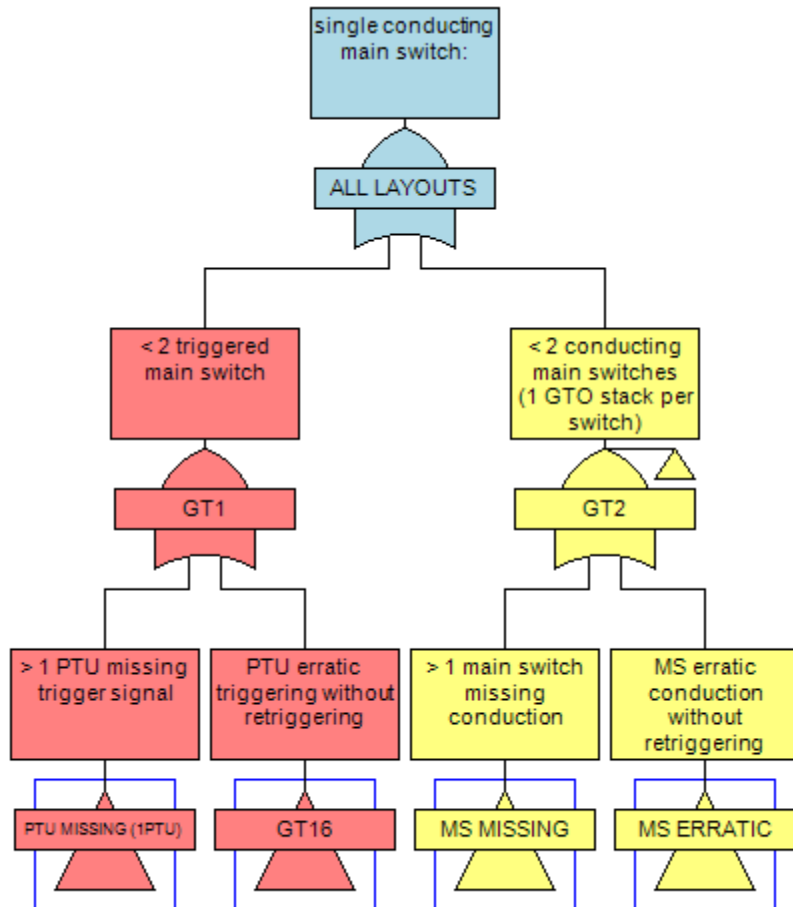


# FT: Input values



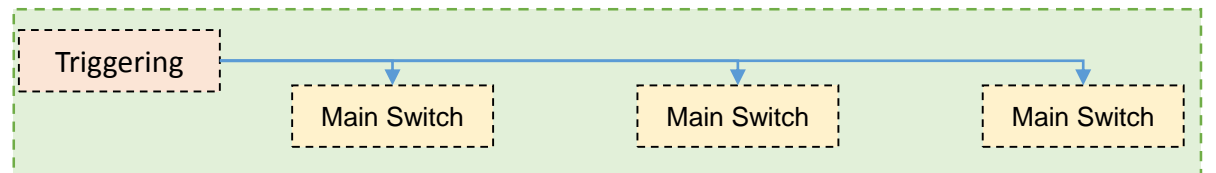
- experience based (system experts and logbook)
- MTTF/ MTTR are estimated with respect to the described operational scenario
- Two MTTF inputs for PTM

# FT: 1003 generators



## 1003 generators

- one erratic + no retriggering
- two missings



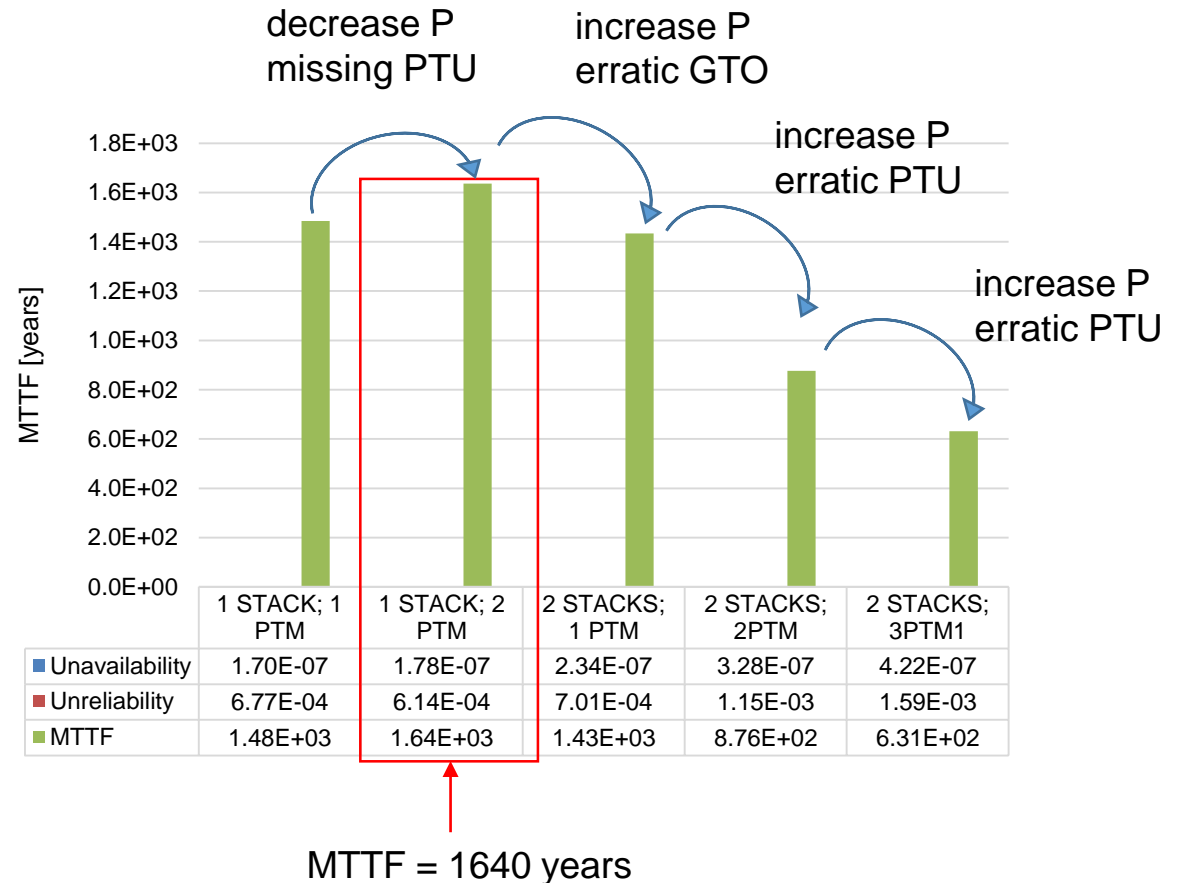
# FT: 1003 generators

## input values:

- GTO more reliable than PTM

Generic data		
basic components	MTTF [years]	MTTR [h]
PTM missing	4	2
PTM erratic	4	2
HVPS (missing)	6	3
GTO Stack missing	10	6
GTO Stack erratic	8	6
FI (missing)	10	24
p FI (missing)	-	-
t=1 year		

- without passive FI the minimal cut set consists for all layouts of 2 components

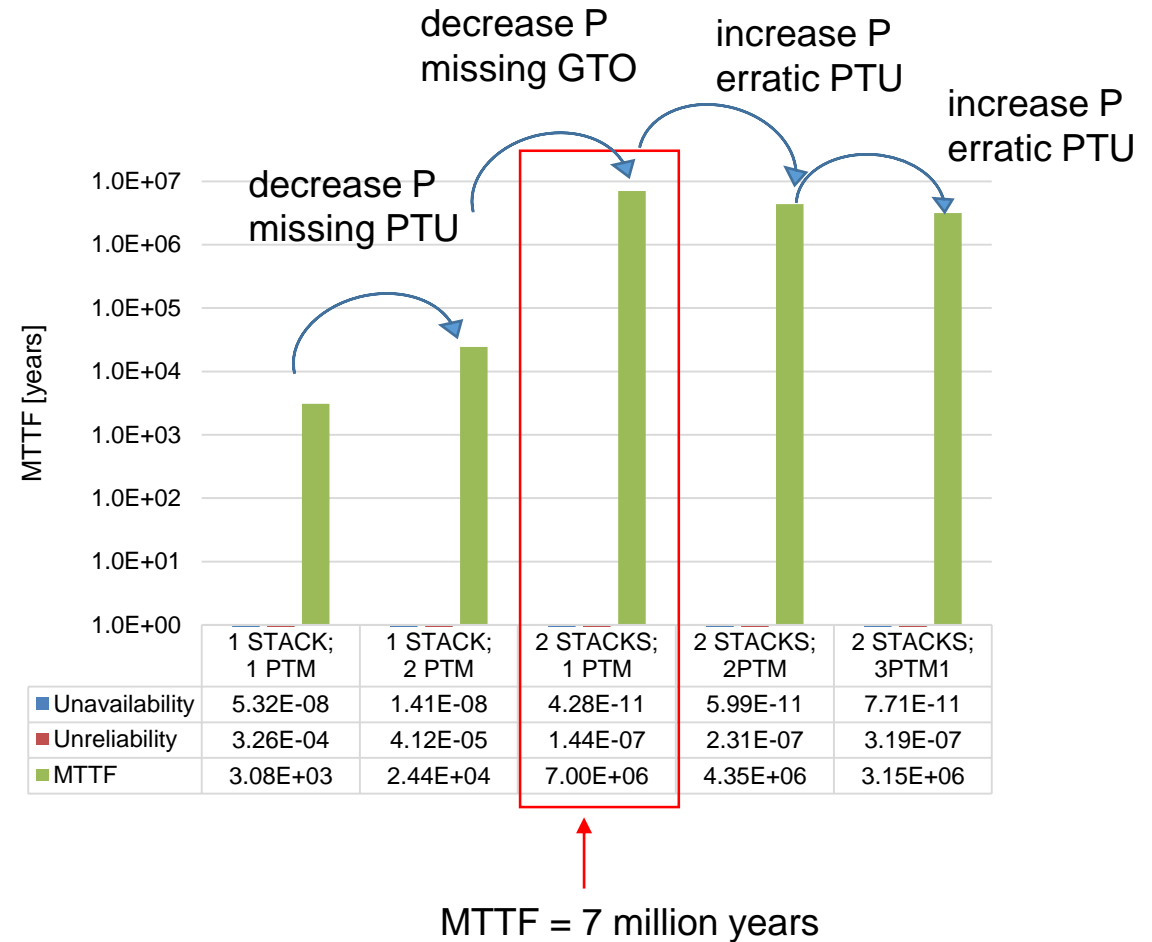
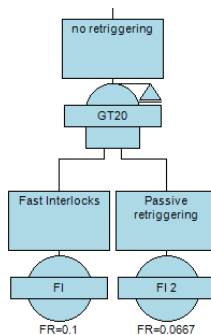


# FT: 1003 generators

## input values:

- GTO more reliable than PTM
- passive retriggering line

basic components	MTTF [years]	MTTR [h]
PTM missing	4	2
PTM erratic	4	2
HVPS (missing)	6	3
GTO Stack missing	10	6
GTO Stack erratic	8	6
FI (missing)	10	24
p FI (missing)	15	24
t=1 year		



# FT: 1003 generators

Sensitivity of the results to the model parameters

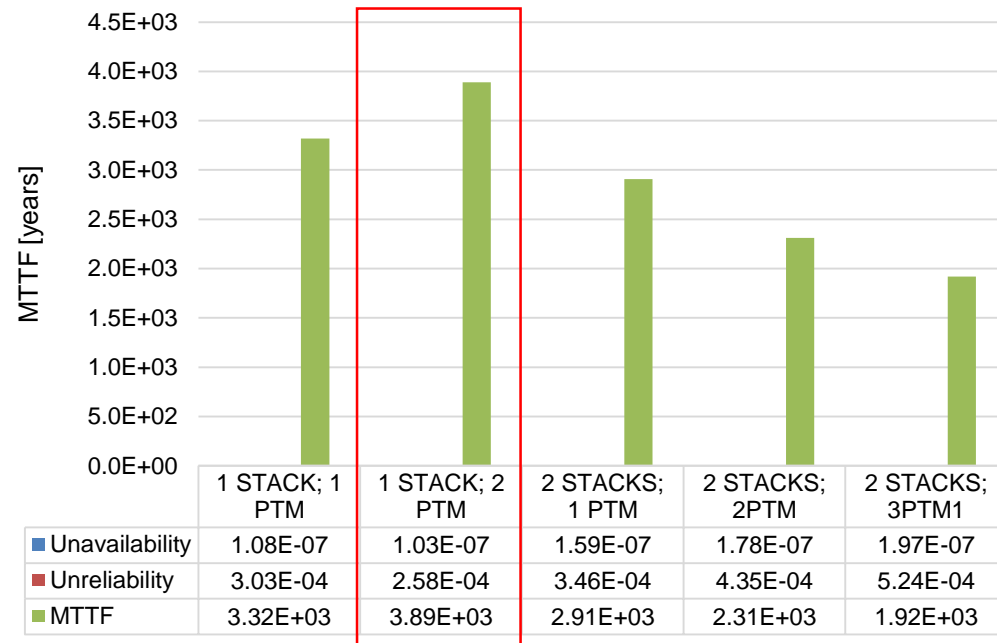
## Variation failure rate PTM

input values:

- PTM more reliable than GTO

basic components	MTTF [years]	MTTR [h]
PTM missing	20	2
PTM erratic	20	2
HVPS (missing)	6	3
GTO Stack missing	10	6
GTO Stack erratic	8	6
FI (missing)	10	24
p FI (missing)	-	-
t=1 year		

➤ Pattern remains the same



MTTF = 3890 years

# FT: 1003 generators

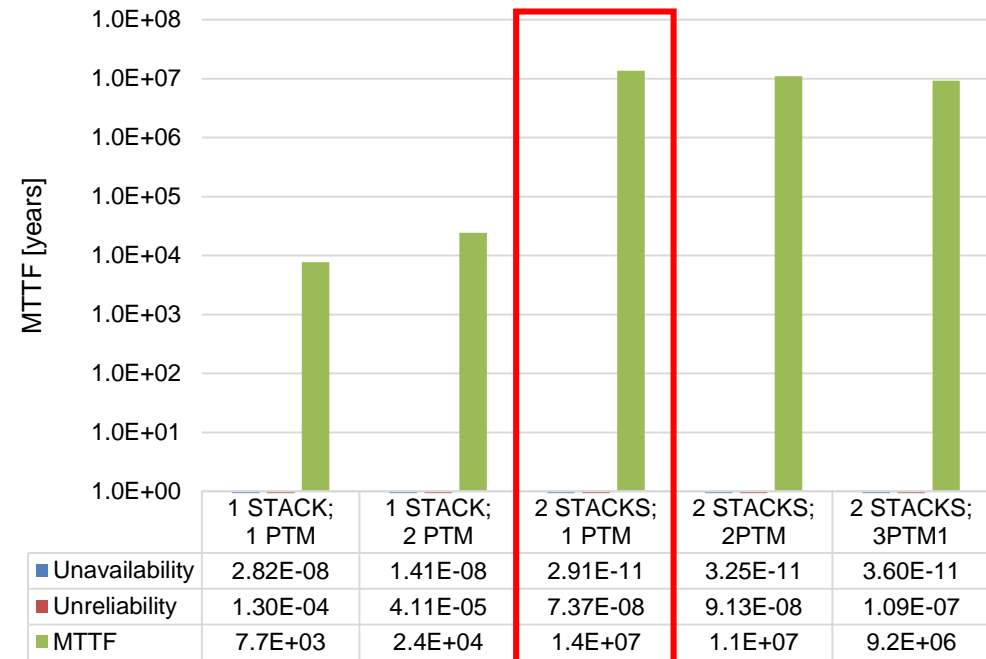
Sensitivity of the results to the model parameters

## Variation failure rate PTM

input values:

- PTM more reliable than GTO
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basic components	MTTF [years]	MTTR [h]
PTM missing	20	2
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t=1 year		



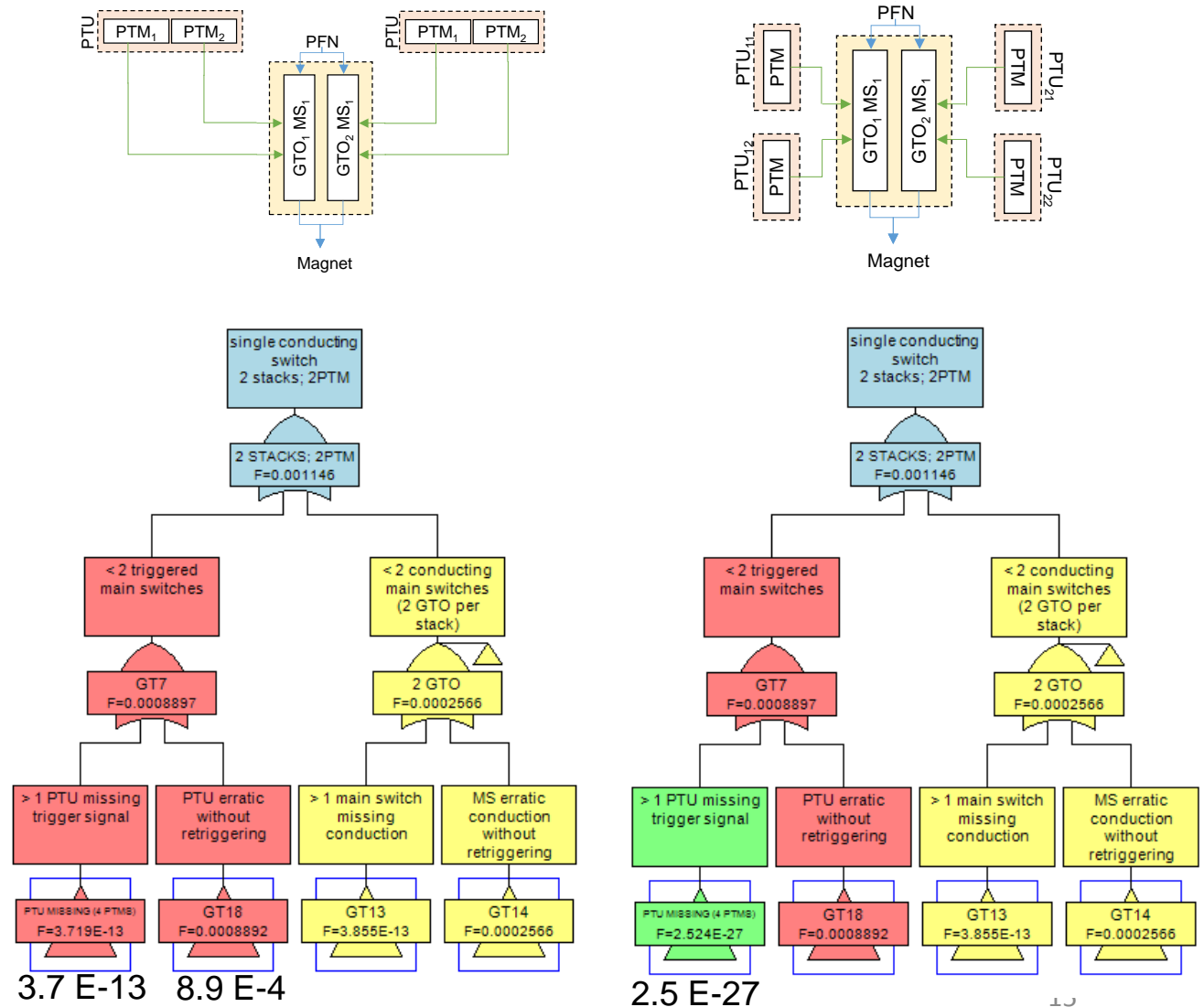
# FT: 1003 generators

## Independent PTUs

### input values:

Generic data		
basic components	MTTF [years]	MTTR [h]
PTM missing	4	2
PTM erratic	4	2
HVPS (missing)	6	3
GTO Stack missing	10	6
GTO Stack erratic	8	6
FI (missing)	10	24
p FI (missing)	-	-
t=1 year		

- two new layouts
  - 2Stacks; 2PTM
  - 2Stacks; 3PTM
- decreased “PTU missing” probability: improvement at the wrong place
- doesn't change “erratics” probability: FM “erratic” is not assumed for PS
- top event results remain the same



# FT: 1003 generators

Sensitivity of the results to the model parameters

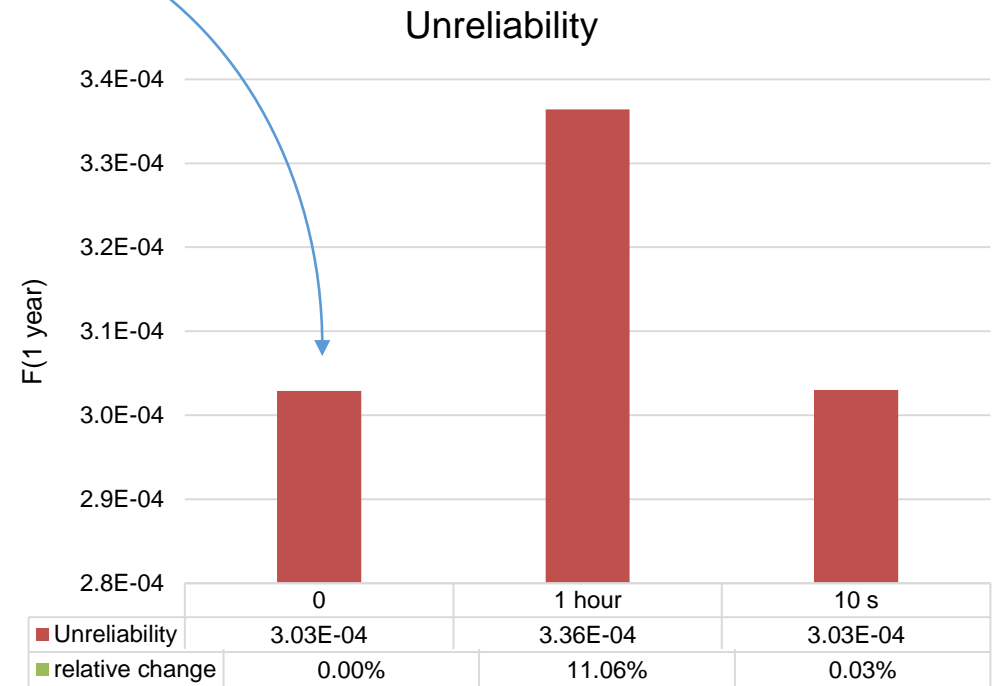
## Variation failure model

### so far: rate-MTTR failure model

- failures are immediately revealed

### dormant failure model

- failures are only revealed when an inspection or test is performed
- 1 cycle = test interval

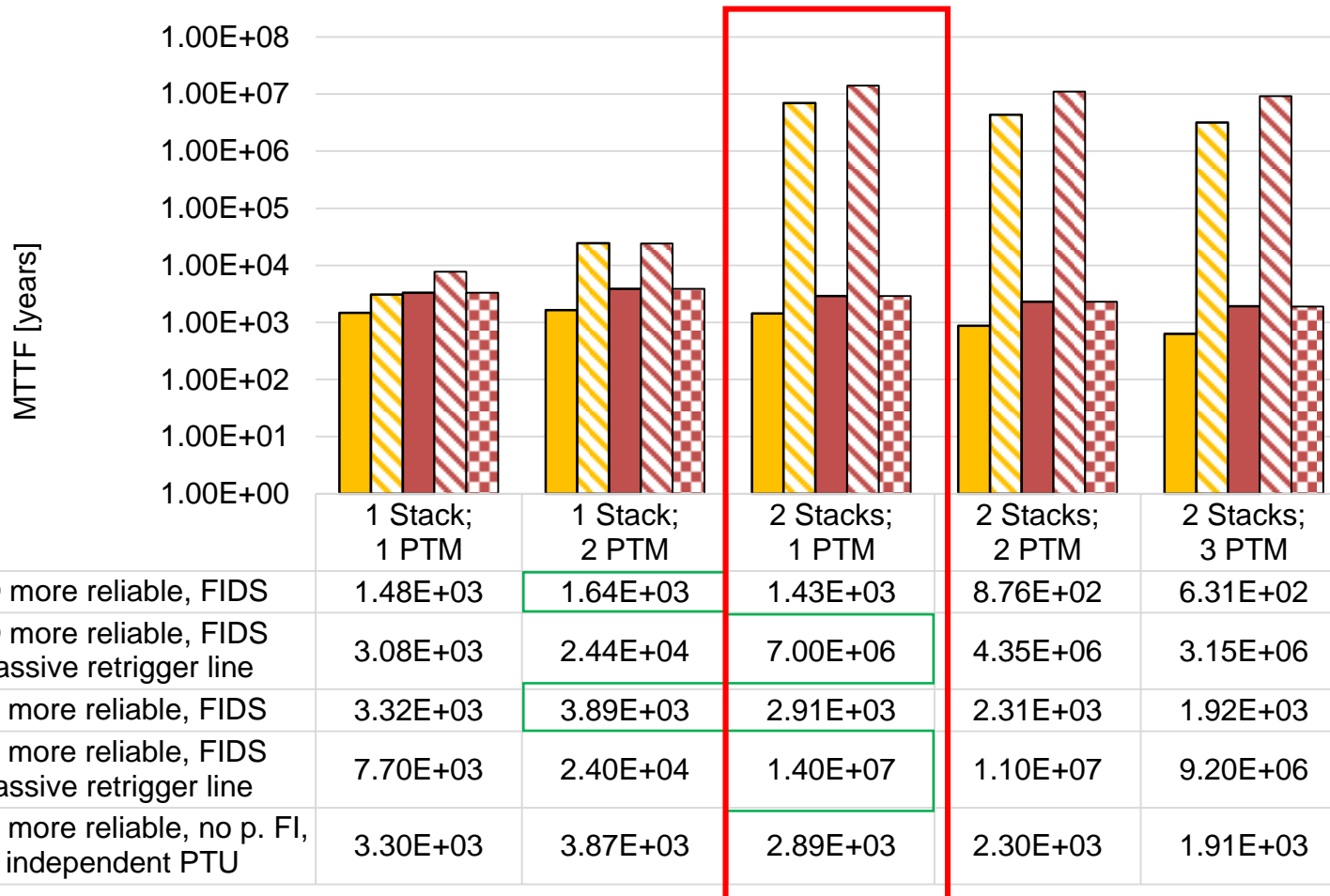


1 Stack; 1 PTM  
FIDS  
PTM more reliable



# Conclusion I

## System failure mode 1003

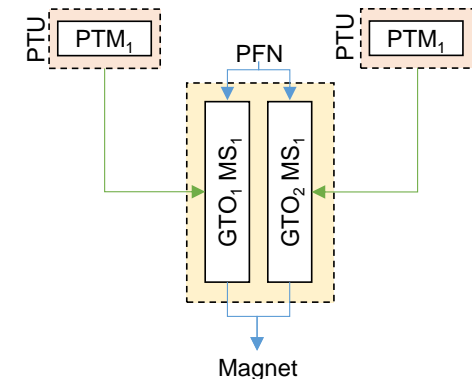


### Sensitivity to the model parameters

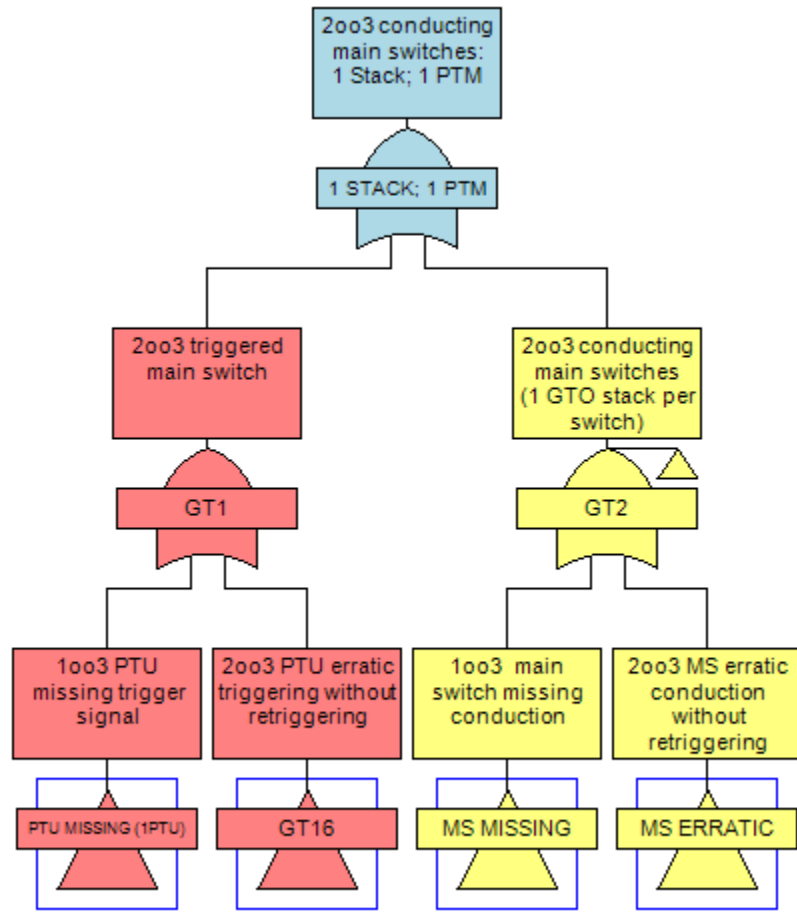
- PTM fr variation doesn't change the pattern
- failure model has minor influence if cycle length = 10 s

### Fault tolerant design

- independent PTU doesn't change the results
- for electrical performance 2 GTO stacks per main switch are needed
- passive retriggering line is recommended



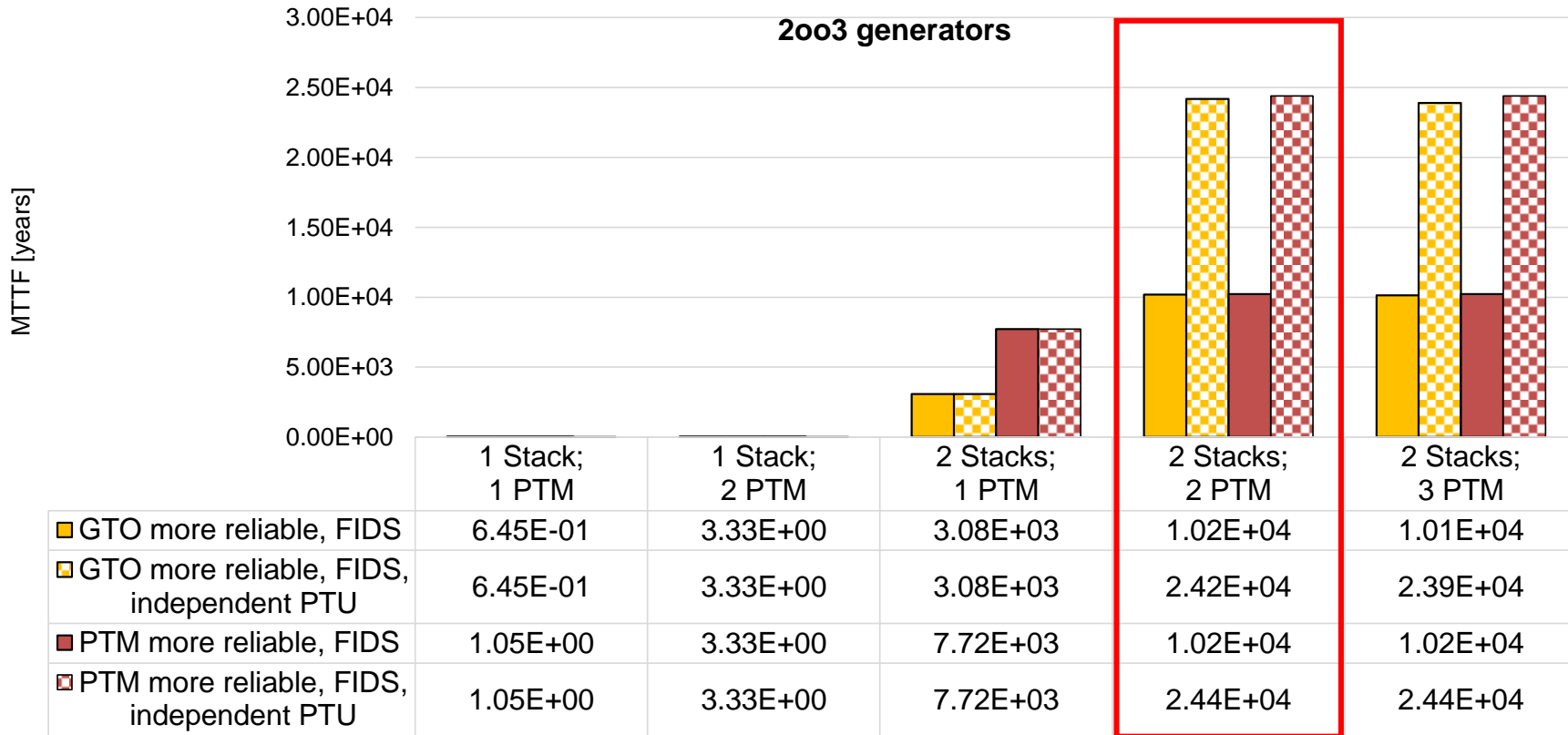
# FT: 2003 generators



- one missing
- two erratics + no retriggering

# Conclusion II

## System failure mode 2003

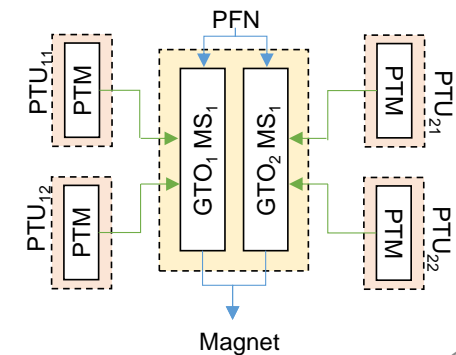


### Sensitivity to the model parameters

- PTM fr variation doesn't change the pattern

### Fault tolerant design

- independent PTU decreases "missing" probability
- passive retriggering line doesn't improve "missing" probability

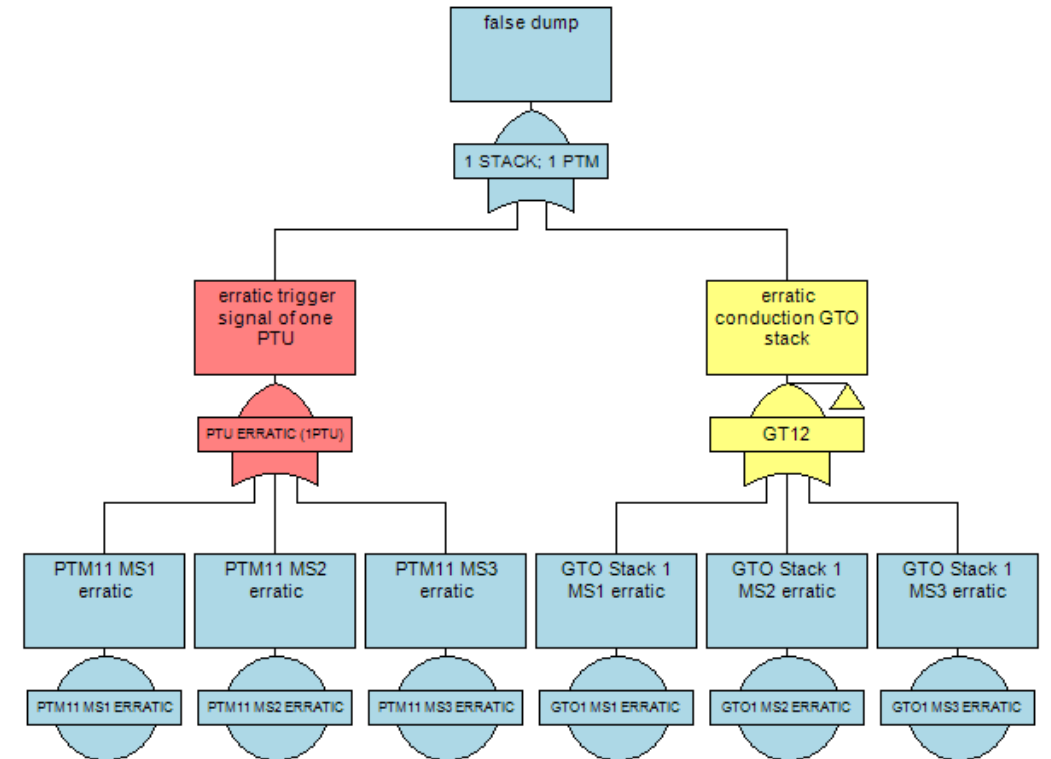


# FT: false dumps

- false dump: erratic + retriggering
- Assumption: all erratics are detected by FIDS
- shortest cut set for all layouts: 1 erratic

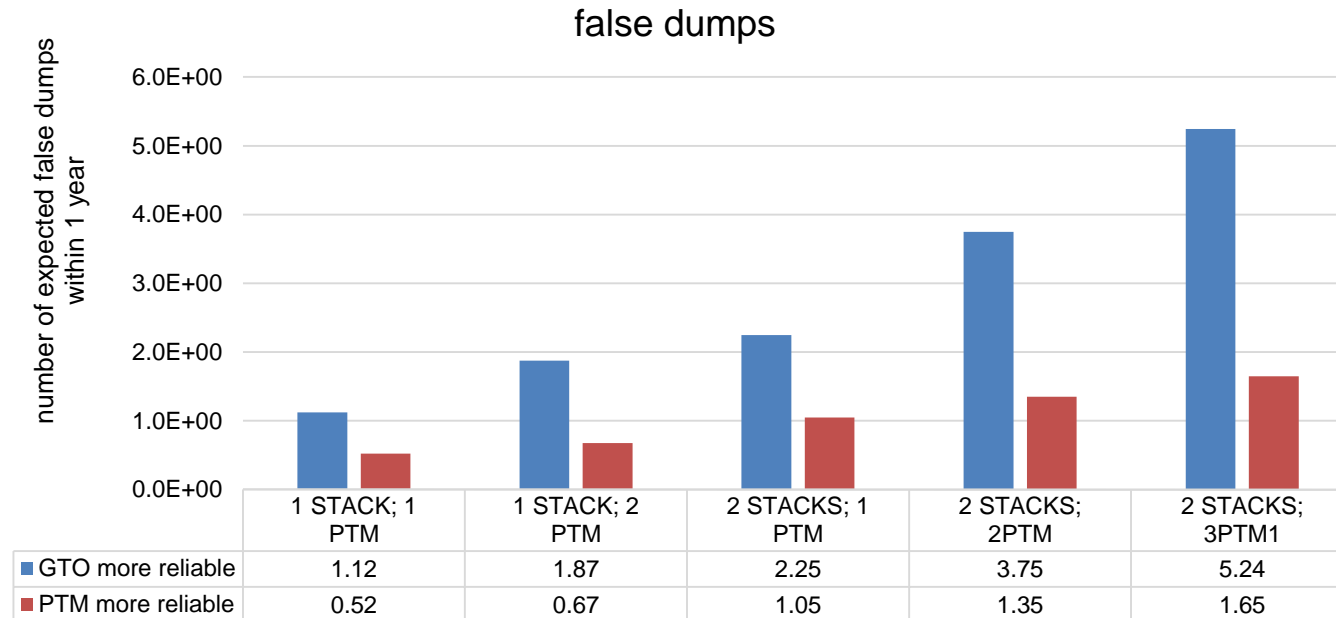
Generic data		
basic components	MTTF [years]	MTTR [h]
PTM erratic	4	2
GTO Stack erratic	8	6
t=1 year		

Generic data		
basic components	MTTF [years]	MTTR [h]
PTM erratic	20	2
GTO Stack erratic	8	6
t=1 year		



# Conclusion III

## System failure mode false dump



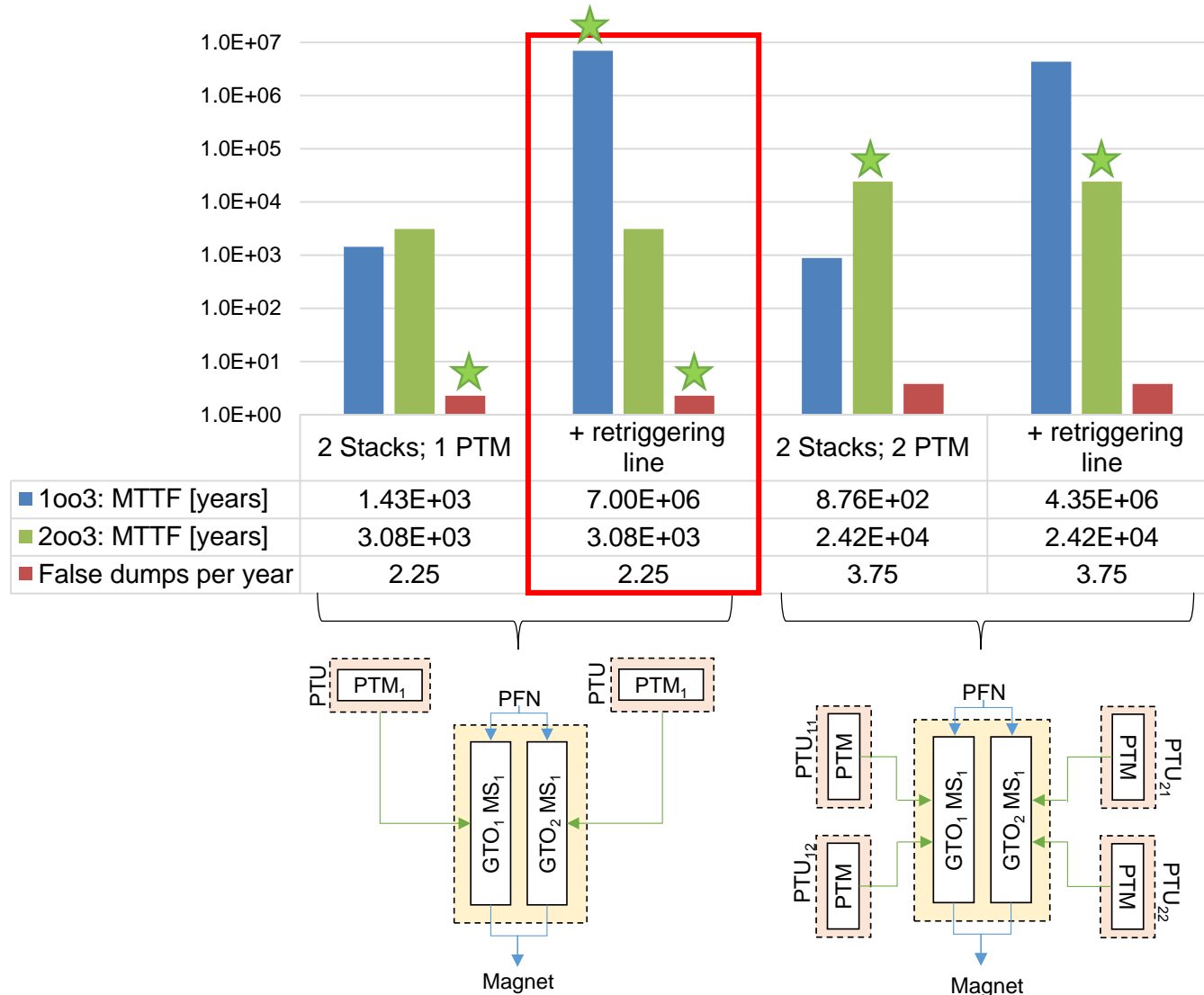
### Sensitivity to the model parameters

- PTM fr variation doesn't change the pattern

### Fault tolerant design

- the higher the number of potentially erratic components the higher the probability of false dumps

# Conclusion IV

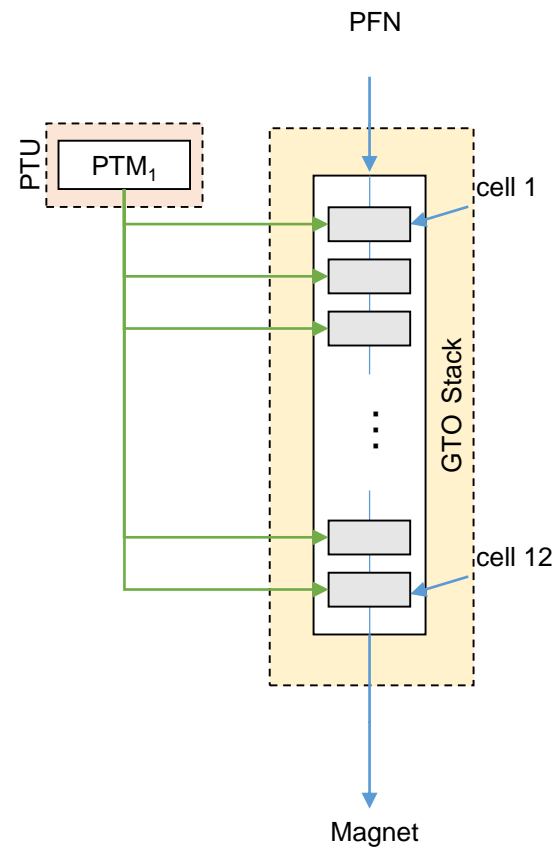
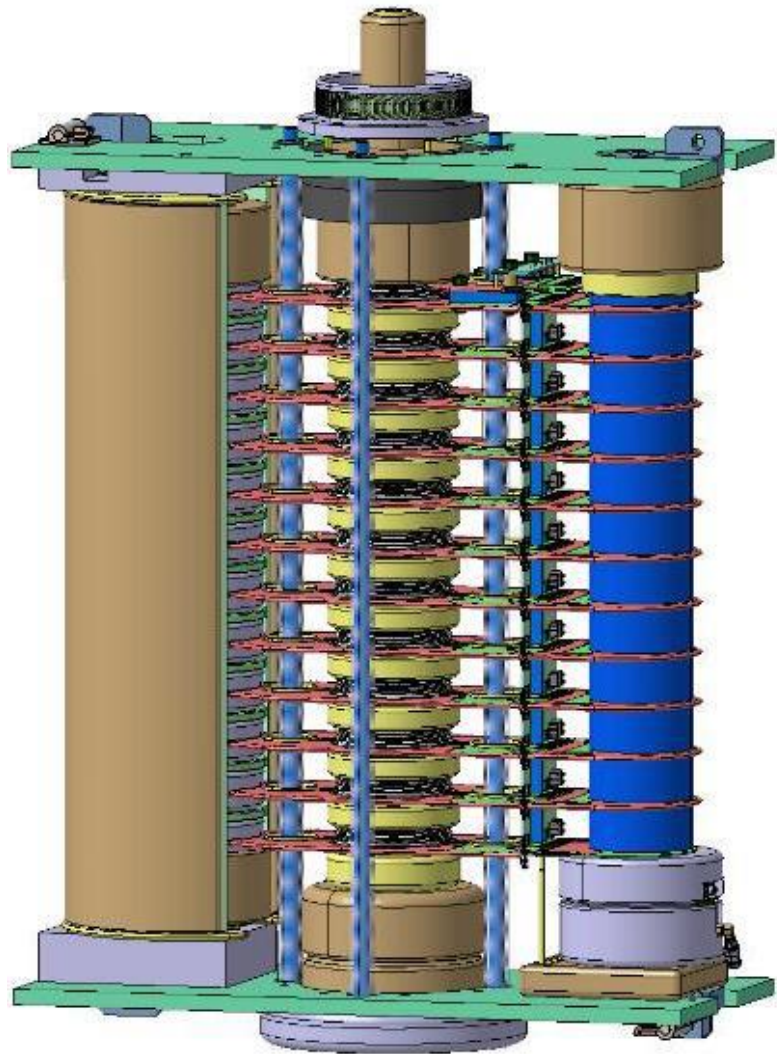


- first priority: FM 1003
- second priority: FM false dump
- third priority: FM 2003

basic components	MTTF [years]	MTTR [h]
PTM missing	4	2
PTM erratic	4	2
HVPS (missing)	6	3
GTO Stack missing	10	6
GTO Stack erratic	8	6
FI (missing)	10	24
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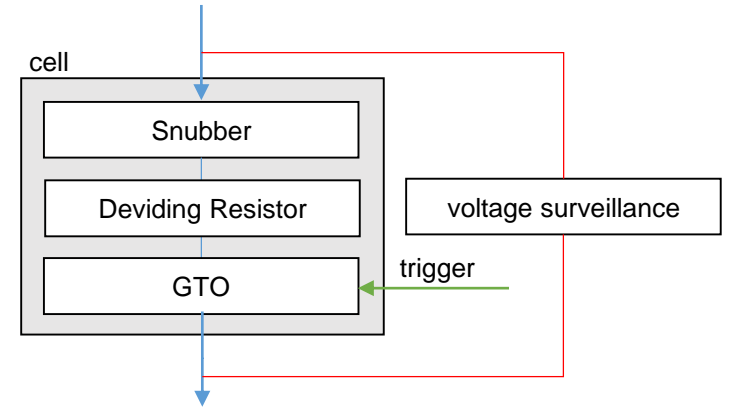


# 1. GTO stack



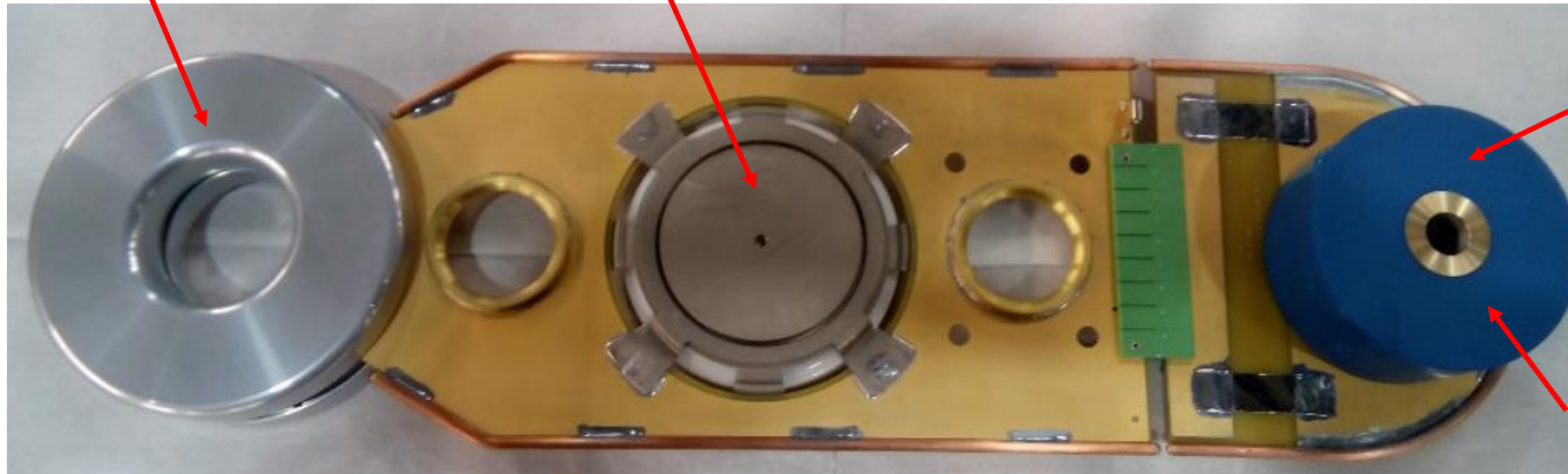


# Details cell



trigger transformer

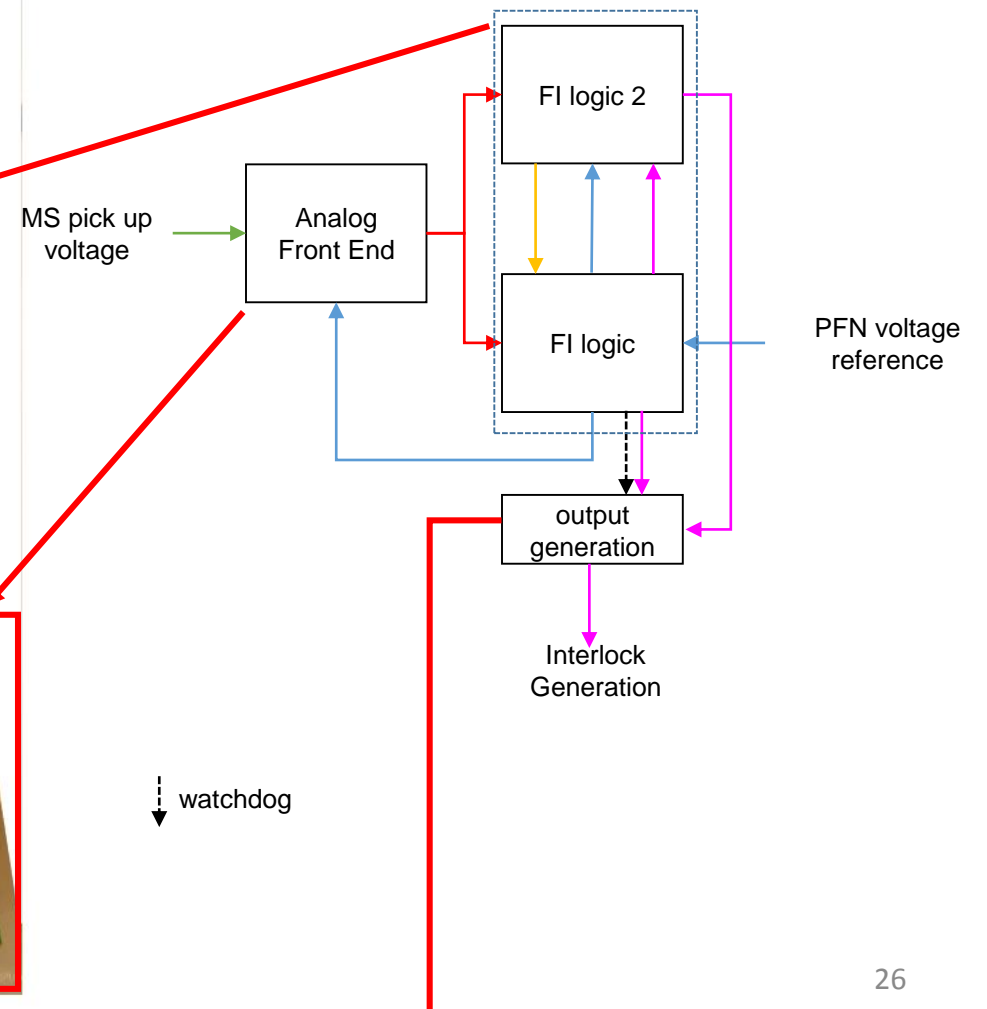
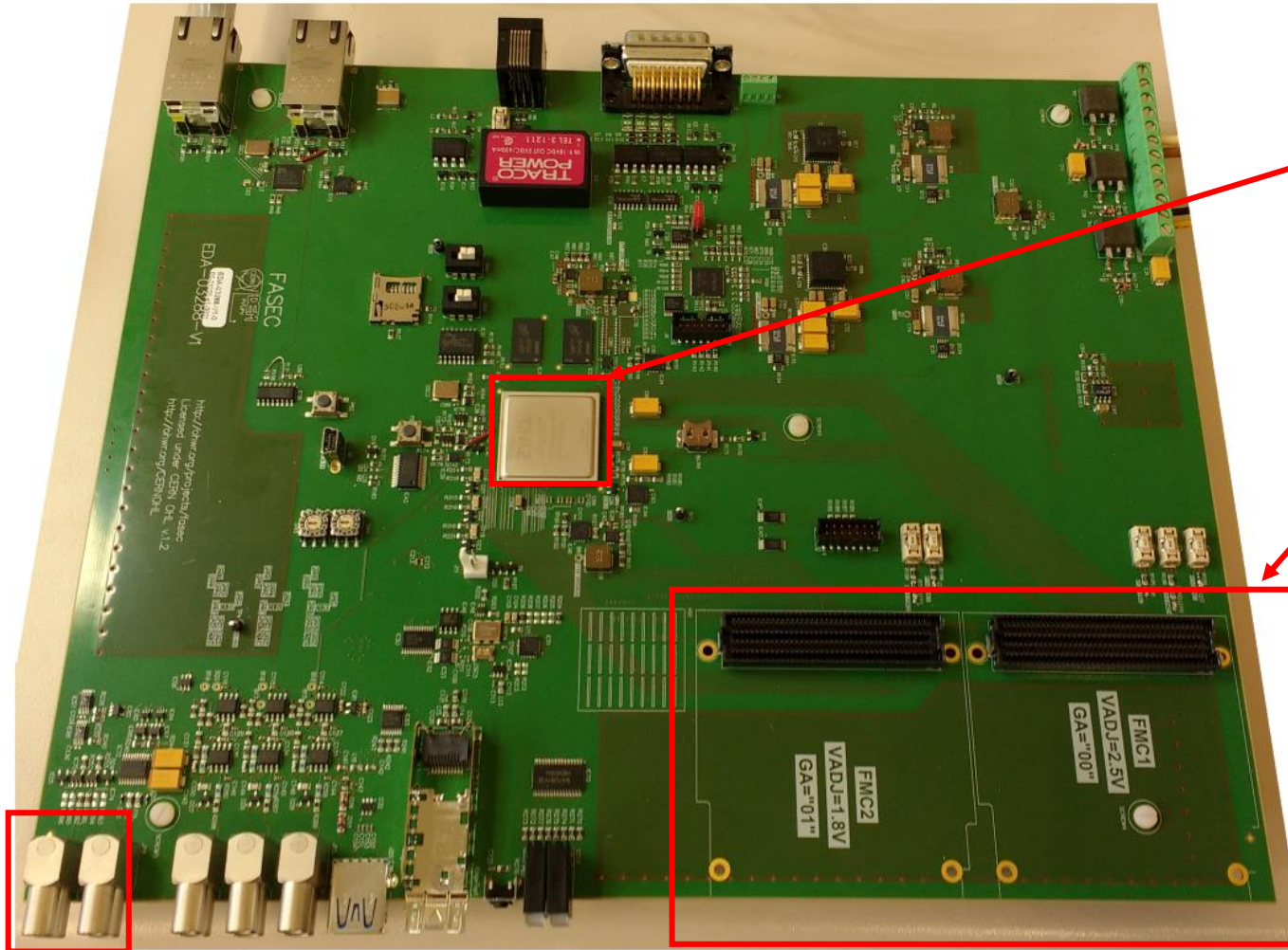
GTO



snubber capacitor

dividing resistor

# Details FIDS



Indenture level		0	1	2	3	4	
<b>0: MKDV</b>							
<b>1: Switch and Triggering</b>							
<b>1.1: Main Switch</b>							
<b>1.1.1: GTO Stack</b>							
<b>1.1.1.1 Cell</b>							
<b>1.1.1.1.1 C Snubber</b>						<ul style="list-style-type: none"> <li>• suppress voltage transients</li> </ul>	
<b>1.1.1.1.2 Deviding Resistor</b>						<ul style="list-style-type: none"> <li>• ensure voltage sharing</li> </ul>	
<b>1.1.1.1.3 GTO</b>						<ul style="list-style-type: none"> <li>• conduct current when triggered</li> <li>• block voltage when not triggered</li> </ul>	
<b>1.2: Power Trigger Unit</b>							
<b>1.2.1 HVPS</b>							<ul style="list-style-type: none"> <li>• supply electric energy</li> </ul>
<b>1.2.2 PTM</b>							<ul style="list-style-type: none"> <li>• receive and retransmit trigger signals</li> </ul>
<b>1.2.2.1 IBGT</b>						<ul style="list-style-type: none"> <li>• shape and amplify trigger signals</li> <li>• conduct current when triggered</li> <li>• block capacitor voltage when not triggered</li> </ul>	
<b>1.2.2.2 Triggering Capacitor</b>						<ul style="list-style-type: none"> <li>• stocking trigger pulse energy</li> </ul>	
<b>1.2.2.3 Diode</b>						<ul style="list-style-type: none"> <li>• suppress unwanted resonances</li> </ul>	
<b>1.3: Fast Interlock Detection System FIDS</b>							
<b>1.3.1 Analog Front End</b>							<ul style="list-style-type: none"> <li>• receive analog switch pick-up voltage and comparator reference</li> </ul>
<b>1.3.1.1 Analog comparator positive</b>						<ul style="list-style-type: none"> <li>• compare switch pick-up voltage (positive and negative amplitude) to reference</li> <li>• generate input signals for FPGA</li> </ul>	
<b>1.3.1.1 Analog comparator negative</b>							
<b>1.3.1.3 Reference DAC</b>							generates analog signal from calculated comparator reference
<b>1.3.2 FI logic digital (FPGA)</b>						<ul style="list-style-type: none"> <li>• calculate the comparator reference, lin. formular</li> <li>• receive comparator output and trigger signal</li> <li>• detect failures: missing, erratic, short circuits, magnet overvoltage</li> <li>• generate fast-interlock events</li> </ul>	
<b>1.3.2 FI logic digital 2 (FPGA)</b>							
<b>1.3.3 Output Generation</b>							<ul style="list-style-type: none"> <li>• verifies that the FPGA is still operative (fixed frequency)</li> <li>• generates output signals from FPGA logic outputs</li> </ul>
<b>1.3.3.1 watchdog</b>							
<b>1.3.3.2 output buffers</b>							
<b>1.4 Passive Retriggering</b>							<ul style="list-style-type: none"> <li>• retrigger all MS after each MS conduction</li> </ul>
<b>2: Pulse Forming Network</b>							<ul style="list-style-type: none"> <li>• energy storage</li> <li>• form quasi-rectangular current pulses</li> </ul>
<b>3. Vertical Magnet</b>							<ul style="list-style-type: none"> <li>• deflect beam vertically</li> <li>• dilute beam</li> </ul>

# FMEA

## Failure modes and effects of the safety systems

### effect on system level

### failure FIDS

1oo3 magnets	no erratic detection
2oo3; overheat dump	no missing detection
2oo3 magnets, no damage of GTO, damage magnet	no sparking detection

### consequence on system level

### failure passive retriggering

1oo3 magnets	no retriggering
	partly retriggering
2oo3 magnets	partly retriggering