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Book of Abstracts

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Parallel Session A1-Readout, commissioning and integration 1 / 0

The readout system for the LHCb Outer Tracker

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The LHCb Outer Tracker is composed of 55000 straw drift tubes.
The requirements for the OT electronics is the precise (1ns) drift time measurement at 6% occupancy and 1MHz readout.
Charge signals form the straw detector are amplified, shaped and discriminated by ATLAS ASDBLR chips.
Drift-times are determined and stored in the OTIS TDC and output to a GOL serializer at L0 accept.
Optical fibers carry the data 120m to the TELL1 acquisition board.
The full readout chain performed well in an e- test beam.

Summary:

The Outer Tracker of the LHCb detector is composed of 55000 straw drift tubes of 5mm diameter.
The requirements for the OT electronics is the precise (1ns) drift time measurement, permitting a track resolution of 200 um in the bending plane, at 6% occupancy and 1MHz readout.
The readout electronics is based on three ASIC chips, the ASDBLR amplifier from ATLAS, the OTIS TDC developed at the ASIC lab in Heidelberg and the GOL (gigabit optical link) serializer from CERN EP.
All on-detector electronics for one module end is housed in a shielded metal box.

The charge signal from the straw anode wires is amplified, shaped and discriminated by an 8 channel ASDBLR chip with 12ns shaping time.
Four ASDBLRs on 2 PCBs are connected to one OTIS TDC.
The relative time between the discriminated hit signal and the bunch clock is determined by the OTIS TDC with the help of a delay locked loop. The 64 inverters in the DLL lead to a time resolution of 25ns/64 = 390ps. Drift times are 6-bit encoded and written to a 240 bit wide L0-buffer. At L0-accept hits within a 75ns window are readout and a header containing OTIS location, L0-id, Bunch-Id plus status is prepended.

L0 accepted data from 4 TDCs runs to the GOL chip.
The GOL serializes 32 input bits to a 1.6 Gbit/s output, driving a VCSEL diode. Optical fibers carry the data 120m to the TELL1 acquisition board.
On the TELL1 daughter boards with 12 inputs each convert the optical serial data back to paralell electrical data. FPGAs on the TELL1 are programmed to synchronize, zero suppress and reformat the data.

At 1MHz events are transmitted through multiple Gigabit ports to a more than 1000 node computing farm.

The newly developed outer tracker electronics was used for data taking in an e- test beam. Reading out 512 channels the full chain proved excellent performance.

Parallel Session B7-DAQ session / 1

Low-power front-end for a Neutrino Underwater Telescope

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The work described here has been developed in the context of the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration ASIC. The solution has a multitude of advantages. The most important are low power consumption and the preanalysis and suitable reduction of data to be transferred to the shore station for acquisition. A detailed description of the chosen architecture and the design principles of the blocks, that carry out the specialized function required by this architecture, will be given.

Summary:

A proposal for a system to capture signals in the Optical Module of an Underwater Neutrino Telescope is described.
An underwater neutrino telescope detects the muons produced by the interaction of neutrinos with the nuclei of matter along the path through the Earth.
These, emerging from the bottom of the sea and passing through sea water, produce light due to the Cherenkov effect.
The detection of the tracks allows the direction and energy of the primary neutrinos to be reconstructed.
The detector sensors are large area (>8")photomultipliers (PMT) in pressure resistant borosilicate glass spheres called Optical Modules (OM).
These also contain the high voltage power supply device, the front-end electronics and the required data transfer and communication unit.
There is a large number of OMs, about 6000, and the power they require is a key element when considering the feasibility of such a detector.
In the experimantal conditions the power transfer is limited, the electronics power consumption must be limited to not more than a few kW in the whole detector, that is less than 200-300 mW in the OM.
Power is transferred to the whole telescope at a great distance from the shore by means of an electro-optic cable and is limited by cable capacity.
Anything which is commercially available and satisfies the technical and power consumption requirements will be

adopted in the OM.
Not included in this forecast are: the Switched Capacitor Array Analogue Memory to capture the signal (LIRA), the module which triggers and classifies the signals, the T&SPC, the synchronous frequency multiplier (PLL), the Control system, the DC/DC conversion system that supplies power starting from the single one that enters from the connector.
The front-end electronics, therefore, have to have low power consumption.
The aim of the Catania Microelectronics group is to design a full custom VLSI ASIC containing as many circuital blocks as possible in order to reduce the total cost of the electronics, utilizing commercial devices for the other blocks.
In the following the blocks which are present in the chip will be described in more detail.
In particular, a device to capture the electric signals of the PMT must perform suitably.
These signals have a very wide dynamic range and a lot of care has to be devoted to the design of the device with the aim of its being able to respond to the need to acquire all the PMT signals adequately.
An accurate analysis of the signal shapes and careful design of the front-end architecture must guarantee the efficiency and precision of the electronics in capturing the signals in very low power conditions.
The design of the Smart Autotriggering Sampler (SAS) chip is the final result.
It is introduced in this presentation together with the simulation results.
A proposal for a system to capture signals in the Optical Module of a Underwater Neutrino Telescope has been described.
It pays great attention to the problem of power consumption with relation to precision.
All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any Underwater Cherenkov Neutrino Telescope.

Parallel Session B5-Power systems / **2**

The CMS Tracker Power Supply System: the Quality Assurance test work results over 2000 power units.

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The CMS tracker Power Supply System is made out of 2000 power supply modules where LV and HV channels are grouped together.
A dedicated quality assurance plan, using a complex, remoted controlled Test Fixture, has been developped in collaboration between INFN-Torino and CAEN spa to test each single channel during and after production.

Details on the test procedure and results that have been obtained are given with emphasis on the expected performances during CMS operation.

Parallel Session B2-Trigger session 2 / 4

LHCb Calorimeter Trigger : Validation Board

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The Validation board participates in the electronic for triggering system of LHCb calorimeter detector.
The board, designed in Annecy-le-vieux Laboratory (LAPP-France), has logic radiation tolerant components: programmable logic, LVDS deserializer, 1.6Gbits optic transmitter.
The inputs come from Front-end board of 4 different detectors (Electromagnetic, Hadronic, PreShower, Scintillator-Pad) by backplane board or shielded twisted pair long cable.
All inputs transmit serial data in LVDS level at 280MHz. The treatment is implemented in 2 large Actel FPGAs cadenced at 40MHz.
The outputs go through an optic mezzanine driven a 12 Channels fibber ribbon.

Summary:

The first prototype of the validation board was finished in October 2005. It works without fault. The methology of the design will be exposed: schematic, layout, EMC rule. The board process 440 input bits and create 256 output bits at 40Mhz. Speed, environment,
material and component choice will be described.
This board will be in the Cavern of LHCb detector. The PCB is with free halogen dielectric, all components must be protected in case of latch-up and redundancy is implemented in Actel ProAsicPlus FPGA.
We choice 676 BGA Package, the PCB is high density with 16 layers, 250µm via and 2.4mm thickness. All CEM rules are used: Clock routing, adapted net, plane, Shielded belt around board, connector. Presentation will show one detail of each rule in the Layout of Trigger Validation Board.
To test all connectivity of the board, we are using several techniques: Flying Probe Test, Boundary Scan Test, dynamic test with bit pattern generator and logic analyzer, dynamic test with spy-memory inside FPGA. 100% of components and nets are tested. The contribution impact of these 4 processes will be shown.
Some inputs are driven by a long cable (15 meter) and signal inside have 280Mhz frequency. To perform this communication, Validation Board has pole zero compensation near the receiver. The motivation of this implantation and the related results will be discussed.
Inputs come from several other electronic rack and crate with several length of cable (2 meter to 15 meter). The mechanism used to synchronise the inputs inside FPGAs will be presented.
At the end, all dialog of this board in the experiment and the result of actual test setup are shown.
To conclude, this talk shows :
• how design a PCB with high speed and high density ;
• what are the important CEM rules ;
• what we must include at the beginning of a conception for the test board ;
• some radiation protection solution ;
• how synchronise many high speed inputs.

Parallel Session A1-Readout, commissioning and integration 1 / 6

Testing, time alignment, calibration and monitoring features in the LHCb front-end electronics

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An overview of testing, time alignment, calibration and monitoring features in the front-end electronics of LHCb is given. General features for this are defined and examples are given of how this has been implemented in sub-detector specific front-end electronics.

Summary:

A sufficient level of well defined timing alignment, monitoring and built-in testing features in the LHCb front-end electronics system will be vital during the commissioning and running phase of the experiment to assure a reliably working large scale system. A set of general features have been defined to allow effective testing to be performed by local sub-systems and also allow these to be used for global system tests:
A: Common definition and timing of calibration pulse injection in detector channels
B: Acceptance of up to 16 consecutive triggers to ease general timing alignment and verify detector pulse shapes and related spill-over.
C: Standardized optical link test used for link qualification, link installation testing and system tests.
D: Standardized readout types to allow calibration pulse injection and other event types to be handled during physics taking.
E: Standardized testing and monitoring features in the interface from sub-detector specific front-end electronics to the general DAQ system.
F: Standardized protocol to perform extensive tests of DAQ links (gigabit Ethernet) and DAQ event building readout network.

The standardized schemes will be presented and examples of how these are integrated within sub-detectors are given.

Poster sessions / 8

Evaluation of Data Transmission at 80MHz and 160MHz Over Backplane, Copper and Optical Links

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The results of data transmission tests over custom backplane, copper and optical links at a multiples of the LHC bunch clock frequency are presented. We have evaluated a parallel data transmission at 80MHz and 160MHz using the GTLP and LVDS standards as well as serial copper and optical links operating at 3.2Gbps.

Summary:

The bunch clock frequency of the LHC accelerator at CERN is specified at 40.07897 MHz. Most of the LHC experiments will utilize this frequency (or its

multiples or derivatives) as the main frequency of data transmission for their Trigger and DAQ electronic systems. For example, the triggering system of the Cathode Strip Chamber (CSC) Endcap Muon sub-detector at the CMS experiment utilizes data transmission at a doubled LHC frequency for most of its data paths, including the LVDS links from an on-chamber electronics to peripheral crates; custom peripheral and Track Finder GTLP backplanes; optical links between the peripheral and Track Finder crates.

A proposed Super-LHC (SLHC) upgrade with increase of the operating frequency

will be challenging for many synchronous data transmission systems. The goal of this work was to evaluate possible solutions for data transmission at 80MHz and 160MHz suitable for the SLHC era. We have used an existing hardware designed for the CSC electronic system for the evaluation of data transmission at 80MHz and 160MHz using the LVDS and GTLP logical standards. We have designed a new evaluation board to study the optical and copper links operating at 3.2Gbps. The results of measurements and possible solutions are presented.

Parallel Session A5-DAQ and Optical technology / 9

A multi-channel optical plug-in module for gigabit data reception

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A plug-in module has been built for reception of optically transmitted data by
gigabit applications. The optical receiving module is based on a 12-channel optical
receiver and an FPGA with embedded deserializers. It is compatible with the G-Link
and Gigabit Ethernet compliant serializer ASIC (GOL) used by many LHC systems. Due
to its compact design, several of these modules could be plugged into VME readout
systems. This module will be the principle element for both the CMS Preshower data
concentrator card and the TOTEM front-end driver. The possible use of this module
for the readout of the ALICE silicon pixel detector is also under examination.

Summary:

Recent studies have shown that the requirements of the Preshower for on-line data-
reduction cannot be met by existing readout hardware designed for use by other CMS
sub-detectors. Hence the need for the development of a CMS Preshower data
concentrator card coincided with similar requirements with the TOTEM experiment.
This gave birth to the idea of a modular VME readout system, common to both systems.

This will allow selection of which constituent modules are to be used, depending on the requirements of each system. The idea of a modular system is also very attractive because it can speed up production, by sharing development between different labs.
The principle element of the new VME readout system is the plug-in module used for reception of optically transmitted data by the front-end electronic systems. The optical receiving module is based on a 12-channel optical receiver and an FPGA with embedded deserializers. The 12-channel digital optical receiver (NGK's POR10M12SFP) used is the one specified for the CMS ECAL optical links. The FPGA used (Altera's Stratix GX family) incorporates up to 20 embedded hardware deserializers with data rate up to 3.125 Gbps. The FPGA is compatible with both the Gigabit Ethernet (8b/10b encoding) and G-Link (CIMT encoding) protocols supported by the GOL serializer ASIC used in the front-end systems of both the Preshower and TOTEM. The deserialized data are provided by the FPGA to the parallel output bus which can be up to 216 bits wide. A 64-bit bidirectional bus is reserved for controlling the module. The optical receiving module also provides an optional connector on top, for attaching an S-Link64 transmitter mezzanine card, if required (i.e. for the TOTEM front-end driver). In addition, an optional electrical gigabit serial output is provided for future use. Although the total number of interconnections is large, its size was kept relatively small (7.5cm x 11.5cm), allowing several of these modules to be plugged onto a VME-9U board.
The functionality of the module has been tested with both the CMS Preshower front-end electronic system and the TOTEM front-end system emulator, and its behavior been deemed satisfactory. Some additional tests done with the PILOT ASIC have shown that the module could also be used for the readout of the ALICE silicon pixel detector.
Besides forming the basis of the CMS Preshower data concentrator card and the TOTEM front-end driver, it is envisaged that this compact plug-in module will also be useful for the readout of other detector electronics systems, for LHC and beyond.

Parallel Session A1-Readout, commissioning and integration 1 / 10

Overview of LHCb electronics installation aspects

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The infrastructure for the electronics, such as cabling, mains power distribution, low and high voltage power supplies, detector safety system, grounding and its installation in the LHCb experimental cavern will be presented. In particular, choices and compromises that have been made for power distribution, racks, cables and cable ducts installation, grounding (EMC) and optical fiber link tests will be described.

Summary:

LHCb presents some particularities compared to other LHC experiments due to its geometry (forward cone coverage). This geometry offers the advantage that most sub-detectors are constructed in two halves that can be opened for maintenance. Accessibility to the on-detector electronics is therefore reasonably easy and equipment such as power supplies can be installed relatively close to front-end electronics. On the other hand, the fact that sub-detectors can be opened implies specific constraints for the cabling and the grounding of the sub-detectors.
A 4 meter thick shielding wall made of concrete blocks protects DAQ interface electronics and a large PC farm of ˜2000 computing nodes against radiation. Cabling from sub-detector specific in/on detector front-end electronics to the protected counting house has a length of minimum 60 meters. The shielding wall acts as an important obstacle for all power, readout and control services that have to pass through a narrow chicane.

The following points are planed to be presented:

- Overview of LHCb electronics installation
- Main choices in electronics and electrical installation o Choice of LVPS and their position in the pit (magnetic stray field and radiation) o Same for HVPS (recommendations) o Cabling recommendations (shielding wall constraints, use of patch panels, moveable parts / use of shielded cables when possible / closed metallic cable ducts for EMC) o Mains power distribution and main choices (separation of farm and electronics distribution, harmonics, remote control, ⋯)
- Grounding scheme in the experimental cavern
- Optical fiber cables o Cable type choice (Multi-mode fibers, MPO connectors, multi-ribbon, gain of space,⋯) o Testing and verification of optical fiber links.
- Racks control and monitoring.
- DSS (detector safety system).

Parallel Session B1-Trigger session 1 / 11

An RPC-based Technical Trigger for the CMS Experiment

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In the CMS experiment, sub-detectors may send special trigger signals, called “Technical Triggers”, for special purposes like test and calibration during the off-beam periods. The Resistive Plate Chambers are part of the Muon Trigger System of the experiment, but might also be used to produce a cosmic muon trigger as Technical

Trigger to be used during the Cosmic Challenge and the later running of CMS. The proposed implementation is based on the development of a new board, the RBC; the test results on prototypes and their performance during the Cosmic Challenge will be presented.

Summary:

In the CMS experiment, sub-detectors may send special trigger signals, called "Technical Triggers", for special purposes like test and calibration during the off-beam periods. The Resistive Plate Chambers are part of the Muon Trigger system of the experiment, but might also be used to produce a cosmic muon trigger to be used during the Commissioning of the detectors to check the efficiency of the installed chambers and, as Technical Trigger, during the Cosmic Challenge and the later running of CMS.
Since this project started only few months ago, when the electronics and cabling in the experimental hall were frozen, this RPC trigger system for the detection of cosmic muons must use as much as possible the existing functionalities and infrastructures and don't introduce major modifications to the existing electronics.
Another constraint is the capability to generate a trigger signal both locally and globally. The local trigger involves the chambers of one Barrel sector and can be used during the Commissioning of the RPCs and the Cosmic Challenge. The global trigger, used as Technical Trigger, involves the whole Barrel and requires infrastructures in the counting room.
In the proposed scheme, the RPC-based Technical Trigger will be implemented by two types of electronic boards: the RPC Balcony Collector (RBC) housed in the cavern and Technical Trigger Unit (TTU) housed in the Counting Room.
Since the RPC signal cables are connected to the Link Boards (LB) for synchronization, data compression and optical conversion, the RBC could access only an OR signal of 96 strips produced by each LB. So each RBC collects the Ors from two Barrel sectors, produces two independent sector-based cosmic trigger as "local" triggers and transmit optically the input Ors to the Counting Room, where the TTU will produce a wheel-level cosmic trigger, to be sent as technical trigger to the Global Trigger of the experiment.
The most convenient position for the RBC is inside the crate housing the LBs. In fact from the backplane can take the power supplies and the slow control signals, while the ORs can be easily taken from the LBs by means of Front-Planes.
The RBC has been designed using FPGA to allow easy upgrades of its firmware by means of JTAG bus. Three prototypes of RBC have been produced, tested and used during the Cosmic Challenge to provide a cosmic trigger from the two barrel sectors equipped with RPC.
In this work the overall scheme of the proposed implementation, the RBC project design, the prototype tests and their performance during the Cosmic Challenge will be shown.

Poster sessions / **12**

The Gigabit Optical Transmitters for the LHCb Calorimeters

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This report presents the boards developed for the optical data transmission of the calorimeter system of the LHCb experiment and test results. We developed two types of transmission boards: the single-channel and the multi-channel ones. Multi-channel boards can be equipped with a variable number of transmitters, depending on the need, with a maximum allowed of 12 channels. Each optical channel allows

transmitting 32 bit data at 40.08 MHz. The boards have been designed and built using radiation hard devices produced at CERN. The optical links have been qualified using the eye diagram and the BERT at 1.6Gbps.

Summary:

The report describes the optical links developed for the data transmission of the LHCb calorimeter system. They are used to establish high speed (1.6Gbps) connections over long distances of about 100 m among the front-end electronics cards of the calorimeter system, the L0 trigger system and the DAQ boards.
The optical transmitters are built as mezzanines boards, i.e. as cards to be plugged to carrier-boards (to the CROC calorimeter boards, to the SPD control boards and to the validation cards). They get power, control signals and reference clock from the underlying carrier-boards. To plug the mezzanines boards to the carrier-boards we plan to use the high-speed connectors by Samtec.
To transmit 32 bits patterns at 40.08MHz through the optical fibers we use the GOL chip (Gigabit Optical Link), radiation hard, produced by the CERN Microelectronic Group. The data transfer rate, running the transmitter at 40.08MHz, including header and parity bits, using the 8B/10B encoding mode, is of about 1.6 GHz per link.
The reference clock will be generated by the carrier-board and distributed to the GOL chips from a clock distributor. The jitter introduced by these devices is guaranteed to be less than 2ps RMS.
As optical transducer in the single-channel transmitter boards we use the VCSEL (Vertical Cavity Surface Emitting Laser) laser diode (1mW at 6mA) by ULM Photonics. It operates on multimode optical fibers at a wavelength of 850nm and is equipped with SMA type fibre connector.
In the multi-channel boards we use a parallel transmitter made by Agilent. The optical transducer is the SNAP12 standard compliant, equipped with the MPO/MTP ribbon fibre connector interface. It operates on multimode optical fibre at a wavelength of 850 nm.
The start up of the GOL is managed by means of the CRT4T power switches.
Special care has been spent in the projecting the PCBs and in placing the bypass capacitors, in order to minimize the noise level and the bit error rate.
The report will describe the test performed on the prototypes to fully qualify the optical link. The link has been qualified using the eye diagram and the BERT. The results show that the BER is better than 10-13 as expected.

Parallel Session A5-DAQ and Optical technology / 13

Status of the TTC upgrade

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The TTC (Timing, Trigger and Control) system broadcasts the timing signals from the LHC machine to the experiments. Once at the detector level, it integrates the trigger information and local synchronous commands with these signals, for transmission to several thousands of destinations. The equipment for this second part of the system is fully produced, but the main network between the machine and the experiments required to be upgraded to ensure its easy maintenance. The design work began at the

end of 2005 The new modules will be tested during the summer 2006 and the structured
test beam in September 2006. A status of this design work will be done, including the
description of the main modules, the results of the tests done on the prototype and
the plans for production and support of this system.

Summary:

The TTC (Timing, Trigger and Control) system broadcasts the timing signals from the
LHC machine to the experiments. At the detector level, it integrates the trigger
information and local synchronous commands with these signals, for transmission via
optical fibres to several thousands of destinations. If the support of the TTC system
at the level of the detectors is well in hand, the main network between the machine
and the experiments required re-development to ensure its easy maintenance.

A proposal to upgrade the TTC backbone was signed in November 2005 by all the
involved parties. This document includes the method and the implementation of the
transmission of the RF timing signals to the experiments, the way these signals are
received and used by the TTC system inside the experiments, and the division of
responsibilities between users and support groups.

The technical solution which has been chosen is a compromise between the short
development time remaining before the start of the LHC, the requirement of a jitter
free solution, and the need of a team available 24hours a day to ensure the on-call
support of this critical system. It is thus based on the solution selected by the
AB/RF group to transmit the timing signals, using one analog optical link per signal
from SR4 (where the RF signals are generated) to each of the experiments.

The final system will consist of VME transmitter boards in the SR4, and of TTC
receiver crates on the experiments' side, including a VME controller and VME modules
to receive the optical signal (RF_Rx), select the sources, adjust their delays and
reduce their jitter (RF2TTC), and distribute them to the experiments (TTC Fanout).
The design of the prototypes of all of these modules is now finished and is currently
being reviewed before being manufactured in May-June. Drivers to control the
selection and the phase adjustment of the signals are currently being written and
will be distributed to experiments.

As the use of analog transmission links is very expensive and not really essential for 70% of the timing signals to be distributed by the AB/RF group (including the Bunch Clocks and the Orbit signals used by the TTC system), the PH/ESS group is working in parallel on a digital optical link which could replace the analog one without any disadvantage.

The complete system, developed by PH/ESS in collaboration with AB/RF, PH/MIC and the four experiments, will be ready for the summer to be fully tested before the September structured test beam. During these 2 weeks of structured test beam, the two systems (RD12 and the upgraded one) will be installed in parallel, to compare their performances and validate the new design.

A status of the system design will be presented, including the description of the main modules, the results of the first tests done on the prototype and the plans for production and support of this system.

Parallel Session A7-ASIC developments / 14

Prototype of the front-end circuit for the GOSSIP (Gas On Slimmed Silicon Pixel) chip in the 0.13um CMOS technology.

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Abstract.
Owing to a novel concept of the detection of the single electrons in gas, the GOSSIP chip will hold certain advantages over an ordinary silicon pixel readout chip. Of these, no need for silicon sensor at all, low detector parasitic capacitance and none of the bias current at the pixel are the attractive features to design a compact low-noise and low-power integrated front-end circuit.
A prototype of the integrated circuit has been developed in the 0.13um CMOS technology. The prototype includes a few channels equipped with the preamplifier, the discriminator and the digital circuit to study the feasibility of the TDC-per-pixel concept.
The measurements demonstrate very low input referred noise (70e RMS) in combination with a fast peaking time (≈40ns) and low analog power dissipation (2uW per channel for 1.2V supply). High frequency switching activity on the clock bus (up to 100MHz) in the close vicinity of the sensitive analog inputs does not cause noticeable extra noise.

Summary:

Summary.
The foreseen GOSSIP (Gas On Slimmed Silicon Pixel) chip will consist of a CMOS pixel

array with a Micromegas grid placed at the distance of 50um on top of it by means of wafer post-processing technology. One mm above this grid a cathode foil is built. The cathode foil and the grid are put at -800V and -400V, respectively, and the pixel array surface is at ground potential. The volume between the drift foil and the pixel array is filled with a suitable gas mixture. When a minimum ionizing (MIP) particle passes the drift gap, some 10-50 electron-ion pairs will be created along the track. Driven by an electric field the electrons will drift towards the pixels. In the Micromegas-pixel gap an avalanche multiplication occurs making the charge sufficient to activate an on-pixel integrated circuit.
The activated pixels will show the projection of the track on the array surface. Moreover the drift time measurements at the activated pixels will indicate the polar angle of the track.
A number of features make the GOSSIP chip advantageous for future particle detectors. It has no thick silicon sensor bulk (slimmed pixel chip). Therefore it has a low material budget and is free from the radiation damage effects taking place in the depletion layer of the silicon sensor. The on-pixel circuit will be radiation hard due to the internal properties of the up-to-date deep-submicron CMOS technology. The value of the parasitic capacitance at the input of the front-end circuit is determined by the area of the pixel pad and consequently could be very low (5fF$\cdots$30fF). This feature enables to design a low-noise (less than 70e RMS) and at the same time very low power circuit. The low power aspect is of primary importance since any additional cooling system involves an increase of the material budget. We expect the GOSSIP chip will dissipate ≈100mW/cmˆ2.
In this work we have developed and tested a prototype of the front-end circuit in the 0.13um CMOS technology.
The front-end circuit consists of the preamplifier and the discriminator. The circuit operates at the low threshold (400e) to provide low single electron inefficiency and good time resolution. The magnitude of the input signal is in the wide dynamic range (1e$\cdots$20000e) due to the low ion-electron production statistics and the avalanche multiplication mechanism in gas. A fast rise time of the circuit's pulse response (≈40ns) is needed to minimize the time jitter related to the variation of the magnitude of the input signals. The circuit does not need to be linear while the value of the channel-to-channel threshold spread is important to keep low (input referred 160e RMS). The charge-sensitive preamplifier follows the scheme proposed by F.Krummenacher. It comprises an extreme low feedback capacitance (1fF) and low input parasitic capacitance (30fF for 40umˆ2 input pad area). This solution provides the input signal charge-to-voltage conversion factor as high as 0.6V/fC. The signal at the output of the preamplifier does not need any additional amplification for the discrimination. The discriminator is based on the current comparator topology and generates CMOS signals at the output. Altogether the front-end circuit dissipates 2uW/channel for 1.2V power supply.
For the drift time measurement each channel of the GOSSIP chip will be equipped with a high resolution Time-to-Digital converter (one bin is 1.6ns). To implement such a TDC a high frequency clock signal needs to be delivered to each pixel. Through the parasitic coupling to the sensitive analog inputs the clock signals may ruin the low-noise performance of the circuit. We have developed a simple high frequency (100MHz) switching digital block on some pixels to characterize this effect.
As far as we have measured the switching noise is hardly noticeable. This accounts for the careful layout of the input traces in combination with the common usage of the isolated NFETs and an increased amount of the substrate contacts throughout in the circuit.

Parallel Session A2-Readout, commissioning and integration 2 / 15

Installation and Commissioning of the On-Detector Electronics for the CMS Electromagnetic Crystal Calorimeter

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The CMS electromagnetic calorimeter is composed of 76,000 PbWO_4 scintillating crystals. The scintillating light is captured by photo-detectors, amplified and digitized. The conversion is performed inside the detector volume and data are transported through optical fibers to the off-detector electronics.
About 25,000 Printed Circuit Boards of 5 different types and 5,500 Gigabit-Optical-Links and fibers should be installed and tested. The integration of electronics, cooling system, mechanical supports, low and high voltage distribution, synchronization and controls are discussed.
Each step of the assembly sequence is followed by extensive test and quality control. Installation, commissioning strategy and the achieved system performance results are presented.

Summary:

A high performance and homogeneous calorimeter based on lead tungstate crystals is an essential part of the CMS experiment.
The CMS electromagnetic barrel calorimeter is composed of scintillating crystals grouped in 36 super-modules of 1700 crystals each. The scintillating light from a crystal is detected by two avalanche photo-diodes (APDs).
The signal amplification and digitization, including the formation of Trigger Tower sums on each group of 25 crystals, is performed inside the detector volume and transported through high speed links (optical fibers) to the counting room. Lower speed links are used to transport timing and control information to and from the detector. This scheme requires a large quantity of radiation hard electronics installed on the detector. The electronics must be highly reliable since it will not be accessible during data taking.
The basic block of the electronics is a Trigger Tower made of 5x5 crystals. It contains 1 Motherboard, 5 Very-Front-End (VFE) boards, 1 Front-End (FE) board, 1 Low Voltage Regulator (LVR) board and 2 Gigabit Optical Hybrid (GOH).
The Motherboard is connected to the avalanche photo-detectors by flexible kapton ribbons and distributes the bias voltage to the APDs and the LV to the VFEs. The LVRB contains three Detector Control Units to monitor input and output voltages and cards temperature. The VFE consists of five identical readout channels, each one consisting of a gain preamplifier (MGPA), a 12-bit 40MS/s 4-channels Analog to Digital Converter and a buffer. It receives and distributes also the 40 MHz clock. The FE board contains the trigger-primitives generation, the digital pipeline and the primary event buffers together with the clock, control links and slow control for configuration. The GOH boards house a data serializer, a laser driver chip (GOL) and a laser diode with an attached fiber pigtail.
Each super-module contains about 552 PCBs (340 VFE, 68 FE, 68 LVRB, 68 MB and 8 token-ring link-boards), 138 Gigabit Optical Links, 17 LV distributors and 12 distributed fiber patch-panels. Each PCB element arrives fully qualified and labeled with bar codes. A total amount of about 4.6 kW of heat has to be removed by the cooling system in order to keep the crystal temperature within the specified tolerance of +-0.1 K.
The installation and commissioning of the 37 (36 + 1 spare) barrel super-modules shall be completed by early spring 2007.
To cope with the construction schedule we have prepared three completely independent assembly stands. Each one consists of a support stand, a cooling unit, a HV and LV system, a readout system for single trigger towers, a database and shared services as the detector control system and the laser. Some extra stands with partial assembly components are also available.
After a super-module arrives in the electronics integration area it is installed in a frame and connected to services. Then the integration sequence proceed in steps, by installing:
1. Motherboards.
2. Cooling system.
3. Trigger Tower electronics (VFE, FE, LVDB).
4. Token-rings including TRLB.
5. GOH, optical fibers and fiber patch-panels.
6. LV distribution, cables and patch panels.
7. Commissioning: one week operation and test of the completed super-module using the standard CMS DAQ and control systems.

At each step the installed components and their locations are registered into a database.
Installation sequence is optimized but still each phase covers the previously installed items, so a full validation of each step is necessary. Extensive testing is part of each installation step to evaluate the full functionality and performance. A pulsed laser is available to test the full chain from crystal to optical fibers outputs (from light-to-light). Internal test pulses are used to test and calibrate the electronics.
The test strategy and procedure during the installation is described and results of the system performance achieved are presented.

Parallel Session A3-Readout, commissioning and integration 3 / **16**

A Read-out Driver for Silicon Detectors in ATLAS

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I present an overview of a read-out driver (ROD) for silicon detectors in the ATLAS experiment at the Large Hadron Collider (LHC). Two silicon-based ATLAS tracking systems, referred to as the Pixel Detector and the Semiconductor Tracker (SCT), are controlled and read-out using a common 9U VME board. A hybrid design of Field Programmable Gate Arrays (FPGAs) and Digital Signal Processors (DSPs) has allowed the Silicon ROD to meet the challenges of format error-counting and event trapping without interfering in the construction and transmission of event fragments to the next level in the read-out system. Performance of the ROD during detector assembly, calibrations and cosmic-ray data-taking are also discussed.

Summary:

The ATLAS experiment is a general-purpose detector centered around one of the LHC pp collision points. Two major ATLAS detector subsystems lie closest to the interaction point–the Pixel detector, comprised of more than 8.0×10^7 channels (1744 modules), surrounded by the SCT, itself containing more than 6.2×10^6 channels (4088 modules); both are essential for providing the tracking information used to tag secondary vertexes from b-hadron decays. The ROD is a 9U VME board common between both of these detector systems and designed to meet the formidable challenge of module configuration and read-out, trigger distribution and event fragment construction.

Each VME board is responsible for the configuration and read-out of up to 48 SCT or 32 Pixel modules. A hybrid architecture of FPGAs and DSPs allow the ROD maximum versatility during physics-running and calibrations. The FPGAs are dedicated to performing ROD setup and module configuration in addition to the formatting, building and routing of events. A single Master" and fourSlave" DSPs reside on the board and are utilized for the control and coordination of on-ROD operations, as well as performing high-level tasks such as data monitoring and module calibration. Once configured, the ROD FPGAs handle the event data path to Level-Two without further assistance from the DSPs.

The Master DSP (MDSP) controls and coordinates ROD operations via a register bank connected to one of its external memory interfaces (EMIF). Two additional EMIFs are utilized for storing additional program code and general data (\emph{ e.g.}, module configuration data). A re-programmable boot ROM is attached to the fourth EMIF allowing the MDSP to load initial code upon start-up. The MDSP's host port interface allows a host CPU continuous access to its internal memory banks.

The four Slave DSPs (SDSPs) are used for error counting as well as event capture and histogramming. One EMIF of each SDSP is connected to a separate pipeline in the Router FPGA, thus allowing events to be transferred independently to any SDSP. SDSP external memory is used to store event histograms. The full memory range of the four SDSPs are available to the MDSP through registers attached the the SDSP host port interfaces.

ROD calibration mode is utilized for running a sequence of module communication and functionality tests that optimize optical receiver settings, verify the function of BC and Level-1 ID counters, set charge injection timing and measure gain offset and noise. Calibration mode has been used extensively during detector assembly–an individual silicon module is thoroughly tested prior to being mounted on a barrel or a disk.

With the advent of SCT commissioning using cosmic-rays, the optimization of ROD software and firmware will continue in concert with working to meet the challenges of Simple Link Interface (S-LINK) readout during physics-running and multi-ROD operation.

Parallel Session A2-Readout, commissioning and integration 2 / 17

Performance of CMS ECAL Very Front End Electronics

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We report the results of tests of 12800 Very Front End (VFE) readout cards for the barrel of the CMS electromagnetic calorimeter. A thorough test sequence was applied to each card including power-on test, burn-in and final detailed calibration. The results show excellent uniformity of the VFE cards. For instance the analogue, digital and buffer currents have average values of 1.59, 0.43 and 0.144 A with RMS values of 0.01, 0.01 and 0.008 A, respectively. The relative gains vary about 1%. Only a few per mille of the cards were failing the power-on test. The results prove the very high quality of the VFE cards.

Summary:

The CMS electromagnetic calorimeter (ECAL) is divided into the Barrel (EB) and two end-caps (EE) made of 61200 and 14648 crystals, respectively. The EB is split up into 36 super modules with 1700 crystals each. The EE is made of 4 DEEs with 3662 crystals each.
The Very Front End (VFE) card is used to amplify, shape and digitize the signals. It comprises five identical read-out channels, serving five crystals. Each channel has a Multi Gain Pre-Amplifier (MGPA) and a four channel ADC followed by LVDS to CMOS level-converters (LVDS_RX). The MGPA shapes and amplifies the signals with 3 different gains (1, 6 and 12). The 3 analogue output signals of the MGPA are digitized in parallel by the four channel 40 MHz 12-bit ADC (AD41240). Digital logic internal to the ADC selects the highest not saturated gain for output. In addition a Detector Control Unit (DCU) reads the leakage currents of the Avalanche Photo Diodes (APD) and the temperature sensors which are mounted on the crystals. All active

components are application specific integrated circuits (ASICS) implemented in 0.25 um technology.
The production and test of the EB VFE cards is completed. The test sequence included:

1. Automatic Optical Inspection (AOI) done by the manufacturer.
2. Power-On test: It is the first electrical test of the VFE cards. It measures the voltages, the currents and performs a functional test of the card.
3. Burn-in test for 72 hours at 60 °C.
4. Calibration of the characteristics of each individual channel by measuring the gain in ADC counts per pC, the pedestal, the noise, the linearity and other relevant parameters.

The voltage distribution measured in the Power-On test for the analogue, digital and buffer voltages are (2.489, 2.499 and 2.45) V with RMS (0.001, 0.001 and 0.03) V.
The relative gains are 5.43 and 10.6 with RMS values of 0.047 and 0.11 compared to the design values of 6 and 12, respectively. This indicates very good uniformity of about 1%.
The MGPA-ADC system was calibrated by injecting 21 different charge pulses distributed over the full dynamic range of 60 pC. Slopes and offsets of the fitted lines are 63.0+/-0.8, 341.7+/-3.8 and 666.7+/-7.7 ADC count/pC and -6.1+/-1.0, 2.4+/-1.2 and 1.7+/-1.0 ADC counts for the gains 1, 6 and 12, respectively.
The noise of completed super modules is found to be 0.58, 0.73 and 1.04 ADC counts with RMS values of 0.04, 0.04 and 0.07 ADC counts for gains 1, 6 and 12, respectively. This corresponds to an expected energy resolution of ˜45 MeV, achieving the design goals.
At the time of writing, 11470 out of 12880 VFE cards had been calibrated, of which 137 did not pass the test criteria and have consequently been rejected.

Parallel Session B3-Trigger session 3 / 18

ATLAS TDAQ RoI Builder and the Level 2 Supervisor system

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The ATLAS High Level Trigger (HLT) uses information from the hardware based Level 1 Trigger system to guide the retrieval of information from the readout system. The Level 1 Trigger elements (jet, electromagnetic, muon candidate, etc.) determine Regions of Interest (RoIs) that seed further trigger decisions. This paper describes the device - the RoI Builder - that collects these data from the Level 1 Trigger and the Level 2 Supervisors (L2SV) Farm that makes these data available to the HLT. The status of the system design and the results of the tests and integration into ATLAS TDAQ system are presented.

Summary:

The Region of Interest Builder (RoIB) is intended to build RoI records from data received from the Level 1 Trigger system and distribute the records at high input rate to a number of Level 2 Supervisors (L2SV) in a farm. From there the RoI records will be distributed to the High Level Trigger (HLT) processors that require it for further event selection and disposition.
The RoIB, located in the underground counting room, takes raw event fragments from

various Level 1 Trigger sources, assembles all the fragments of a given event into an RoI record, selects a target L2SV processor, and then sends the RoI record to this processor. The ROIB is implemented as a number of VME boards in a 9U VME crate with a custom built backplane.
The Level 2 Supervisor farm, located in the surface TDAQ computing farm barracks, is composed of commercial rack mounted PCs. They are connected to the RoIB via ATLAS standard SLINKs and to the High Level Trigger –via Ethernet. A single Level 2 Supervisor processor never sees the full Level 1 rate and it can manage the required input/output event rate.
The RoIB and L2SV system has undergone a number of prototypes, a series of design reviews and several tests, and integration with individual parts of the Level 1 Trigger system and the HLT. Now it enters the commissioning stage via incremental installation of individual RoIB components and connection of the Level 1 Trigger system up to the fully populated RoIB crate. The size of the L2SV farm will be supplemented according to need determined by the increasing event rate during commissioning.

Poster sessions / 19

Large scale production of the Multi-Chip Module of the ATLAS Level-1 Calorimeter Trigger

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The Pre-Processor Multi-Chip Module (PPrMCM) is the main processing block of the Pre-Processor System in the ATLAS Level-1 Calorimeter Trigger. The PPrMCM holds a dedicated signal-processing ASIC and a Phos4 timing-chip together with seven commercial dice mounted on the substrate. Those are four FADCs and three LVDS-serialisers.
The PPrMCM holds the main functionality of the Pre-Proccessor System, namely the digitization, calibration and Bunch-Crossing-Identification of calorimeter signals.
The production phases of the PPrMCMs (more than 3200) and test procedures for quality control at different stages of the production are presented.

Summary:

The Pre-Processor Multi-Chip Module (PPrMCM) is the most crucial part of the of the Pre-Processor System of the ATLAS Level-1 Calorimeter Trigger. The main tasks of the PPrMCM are the digitization, calibration and Bunch-Crossing-Identification of all ATLAS calorimeter signals.
The production of the PPrMCM is done in several steps. The main steps are substrate

manufacturing, dice placing and bonding, “Glob-top”protection and hermetic brass-cover soldering.
Among the chips on the PPrMCM, the Pre-Processor ASIC (PPrASIC) is the major component as it performs the ATLAS-specific digital data processing. Thorough tests of the PPrASIC and of the complete PPrMCM were developed and combined later into a testing framework. The framework contains the software to perform automatic tests in order to verify the full functionality of the PPrMCM. It is applied after each PPrMCM production phase starting with the ASIC-dice production on wafers, up to final acceptance-tests for the complete MCM-assembly. This strategy allows to detect faulty components at early stages of production. Such components can be located and replaced in a repair cycle. This improves initial production yield from 87% to an even higher percentage.
More than 3200 fully functioning PPrMCMs are produced and ready to be installed in the ATLAS Level-1 Calorimeter Trigger. The experience gained from the large scale production of the PPrMCM is reported including the optimization of the test procedures, the production yields, observed problems and corresponding solutions.

Poster sessions / **20**

A compact plug-in module for LHC-like trigger emulation

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A programmable random trigger emulation system has been built for use in high
energy physics, nuclear physics or radiology experiments. The emulator is based on
the generation of trigger time intervals using a true random bit generator. The
system is able to work either as a stand alone trigger emulator or as a plug-in
module for a trigger/readout system.

Summary:

The requirement of a device emulating the arrival of particles on a particle
detector is apparent in the construction phase of the corresponding readout
electronics and DAQ system.
The emulator produces randomly generated trigger pulses with time intervals
following an exponential distribution with programmable mean between 1 KHz and 1
MHz (trigger rate). The source of randomness is the avalanche effect on a
transistor emitter-base diode biased by a digitally controlled voltage source.
Therefore, by changing the diode biasing the desirable trigger rate is obtained.
The output of the random generator is treated by a digital processing circuitry
implemented in an FPGA.
The digital processing includes:
• emulation of experiment specific features e.g. the

arrangement of the LHC
bunches during the LHC operation cycle,
• trigger specific rules e.g. maximum consecutive
triggers with minimum
arrival times.
Burst of 1000 random triggers are recorded and can be
played back. In addition to
the random triggers, the system also supports fully
programmable trigger generation
in order to test other distributions. When working as a
stand alone trigger
generator, the system is controlled by a standard pc via the
USB interface.
The system has been extensively evaluated. The
output of the true random
generator has been verified using the NIST battery of tests
for random number
generators. Finally, the system has been calibrated in
respect to the trigger rate.

Plenary Session P5-LHC experiment electronic upgrades / 21

Charge pump DC to DC converter Inner Tracker Applications

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We present results from a capacitor charge pump DC-DC converter prototype using
0.35um HV-CMOS technology fabricated in April 2006. The purpose of this prototype is
to test the switch technology both for achievable efficiency and for radiation
tolerance. The IC of this test device contains only switches, with all clocks being
externally supplied and driven and the capacitors also external. The configuration
used is a 4 capacitor stack producing a nominal x4 input current multiplication
factor. The goal for this type of device is to be of low enough mass and high enough
radiation tolerance to be placed on individual modules in the innermost layers of the
ATLAS detector. Irradiation results will be presented if available. A prototype test
card for use with a silicon strip stave prototype is under development.

Summary:

We present results from a capacitor charge pump DC-DC converter prototype using
0.35um HV-CMOS technology fabricated in April 2006. The purpose of this prototype is
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radiation tolerance to be placed on individual modules in the innermost layers of the
ATLAS detector. Irradiation results will be presented if available. A prototype test
card for use with a silicon strip stave prototype is under development.

Poster sessions / **22**

Local Trigger Processor Interface Module

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The interface between the ATLAS Central Trigger Processor (CTP) and the sub-detectors read-out systems is done through the Local Trigger Processor modules. These modules allow each sub-system to either run in global mode when it gets the timing and trigger signals from the CTP or in local mode when it handles locally its trigger and timing signals. During the commissioning phase of the detector and for test purposes, it may be necessary to have several sub-detectors able to run locally with the same timing and trigger signals (e.g the calorimeters and the level-1 calorimeter). Although feasible with the current LTP modules, an extra interface module (LTPIM) has been designed in order to void the need for adhoc cabling. The LTPIM is a 6U VME64x module housing two Altera Cyclone FPGAs for VME interfacing and control. All inputs and outputs are configurable through VME accesses. Special care has been taken for handling possible long distance LVDS transmission using active equalizers. The timing of all signals can be adjusted by means of individually programmable delay circuits. The delay circuits, as well as the active equalizers, use an I2C comunication bus controlled by the control FPGA. A description of the module as well as test results will be presented.

Parallel Session B7-DAQ session / **23**

Alibava : A portable readout system for silicon microstrip sensors

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A portable readout system for silicon microstrip sensors is currently being developed. This system uses a front-end readout chip, which was developed for the LHC experiments. The system will be used to investigate the main properties of this type of sensors and their future applications.

The system is divided in two parts: a daughter board and a mother board. The first one is a small board which contains two readout chips and has fan-ins and sensor support to interface the sensors. The last one is intended to process the analogue data that comes from the readout chips and from external trigger signals, to control the whole system and to communicate with a PC via USB. The core of this board is a FPGA that controls the readout chips, a 10 bit ADC, an integrated TDC and an USB controller. This board also contains the analogue electronics to process the data that comes from the readout chips. There is also provision for an external trigger input (e.g. scintillator trigger) and a 'synchronised' trigger output for pulsing an external excitation source (e.g. laser system).

Parallel Session B7-DAQ session / 24

Production Test Rig for the ATLAS Level-1 Calorimeter Trigger Digital Processors

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The Level-1 Calorimeter Trigger is a digital pipelined system, reducing the 40 MHz bunch-crossing rate down to 75 kHz. It consists of a Preprocessor , a Cluster

Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce electron/photon, tau, and jet trigger multiplicities, total and missing transverse energies, and Region-of-Interest (RoI) information. Data are read out to the data acquisition (DAQ) system to monitor the trigger by using readout driver modules (ROD). A dedicated backplane has been designed to cope with the demanding requirements of the system. A number of pre-production boards were manufactured in order to fully populate a crate and test the robustness of the design on a large scale. Dedicated test modules to emulate digitised calorimeter signals have been used. All modules, cables and backplanes on test are final versions for use at the LHC. This test rig represents up to one third of the Level-1 digital processor system. Real-time data between modules were processed and time-slice readout data was transferred to the ROD at a trigger rate up to 100 kHz. Intensive testing consisted of checking the readout data by comparing to hardware simulations of the trigger. Domains of validity of the boards were also measured and dedicated stressful data patterns were used to check the reliability of the system. Tests results have been successful and the Level-1 calorimeter trigger system is proceeding to full production.

Summary:

The ATLAS Level-1 Calorimeter Trigger system reduces the LHC bunch-crossing rate of 40 MHz down to a rate of 75 kHz. About 300 Gbytes/s of input data are processed and events are selected within a fixed time of 2⊠s. The algorithms of selection are FPGA-based to add flexibility to the system. Data are digitised and pipelined by using three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The CP and JEP receive their digitised calorimeter trigger-tower data from the PreProcessor, and provide trigger multiplicity information to the Central Trigger Processor via Common Merger Modules (CMM). Using Readout Driver (ROD) modules, the CP and JEP will also provide Region-of-Interest (RoI) information for the Level-2 Trigger, and intermediate results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

The CP and JEP system receive their data through backplane connections. A custom backplane has been designed in order to cope with the high connectivity demands of the system and to route data between boards in order to accommodate the trigger decision algorithms. The backplane also needs an adaptor for a VME CPU board and an additional module to broadcast the 40 MHz TTC encoded information to the modules in the crate.

The CPM and JEM have common design features. Both received digitised data in LVDS format at a rate of 480 MBaud. Single-ended serialised data between boards across the backplane is processed up to a speed of 160 MHz in case of the CPM. The CMM gathers information through the backplane, but also between crates, and transfers the trigger information to the overall Level-1 Central Trigger Processor.

All Calorimeter Trigger modules transmit their readout data using G-link transceivers. These are connected to RODs, capable of processing up to 18 modules individually.

All trigger modules, with the exception of the VME CPU, are custom designs. Although every module had been developed and tested and seemed ready for production, it was important to validate the final versions of the different modules in harsh conditions. The production was therefore divided in two phases: a first batch was manufactured with an adequate number of pre-production boards to perform a full-crate test, and only after seeing the results would the remainder of the modules be produced. Up to 14 CPMs and 16 JEMs have been built, representing nearly one third of the final digital part of the trigger system. The cables delivering the digitised signals were used, together with the final custom backplane. The source of data was provided by specially designed boards that emulate the total input of one CPM or JEM, corresponding to around 70 Gbytes/s of transferred data when the crate was fully configured. All readout information was fed to a ROD.

Previous tests had been run using the ATLAS online software. It was therefore easily expandable to a system of such a scale by extending the database. With a full crate

in operation, bit-error rate measurements or parity checks were performed over long-term runs. A simulation framework was already available, and individual readout data were compared against the simulation to verify the correct behaviour of the different algorithms. Domains of validity of the data were measured by shifting the 40 MHz clock over its period. To detect any timing misalignment, Level-1 pre-flagged events were sent to a ROD. Trigger rates up to 100 kHz were investigated. Stressful data patterns were created in order to test the reliability of the system with an ATLAS occupancy rate greater than 10 %. The system was also monitored using the PVSS tools to check for current consumption and temperature hot spots inside the crate.

The results of the tests were successful and the ATLAS level-1 calorimeter system is now proceeding to full production.

Poster sessions / 25

Low-noise design issues for analog front-end electronics in 130 nm and 90 nm CMOS technologies

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Deep sub-micron CMOS technologies are widely used for the implementation of front-end electronics in various detector applications. The IC designers'effort is presently shifting to 130 nm CMOS technologies, or even to the next technology node, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. In this work the results of signal and noise measurements carried out on CMOS devices in 130 nm and 90 nm commercial processes are presented. Data obtained from the measurements provide a powerful tool to establish design criteria in nanoscale CMOS processes for detector front-ends in LHC upgrades.

Summary:

Deep sub-micron CMOS technology has met the challenging design requirements for front-end electronics in various High Energy Physics (HEP) detector applications. For instance, CMOS commercial technologies of the quarter micron node have been extensively used for the implementation of radiation tolerant, low noise, low power readout circuits with very high channel density for analog and digital processing in pixel and microstrip detectors at the Large Hadron Collider (LHC) experiments under construction at CERN. The increased luminosity and track densities expected in the experiments at the next generation colliders (LHC upgrades, International Linear Collider, Super B-Factory) set the demand for moving to more scaled CMOS technologies. Nowadays, CMOS processes with 130 nm minimum feature size are widely available for Application Specific Integrated Circuits (ASICs) design, and 90 nm processes are coming on-line as the next industrial generation; therefore, the IC designers'effort is presently shifting to these technology nodes to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. At nanoscale geometries, below 100 nm feature sizes, modeling the behavior of analog parameters of these devices is a tricky problem, since some effects which can deeply affect the MOSFET performance, such as short channel effects, already observed in previous generations of technology, become more difficult to overcome; therefore, these advanced processes require a thorough evaluation of the impact of technology scaling on the main device analog parameters. This work presents the results relevant to the signal and noise characterization of single CMOS devices belonging to two commercial CMOS processes with minimum feature size of 130 nm and 90 nm manufactured by STMicroelectronics. The devices were

characterized at drain currents from several tens of uA to 1 mA, that is, the usual operating currents of input devices in integrated charge-sensitive preamplifiers. In these conditions, deep sub-micron devices are biased in weak or moderate inversion. The behavior of the main signal parameters and of the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width to account for different detector requirements. The wide set of measurements provide a powerful tool to establish design criteria in 130 nm and 90 nm CMOS process. The analysis of the experimental results also includes the comparison of signal and noise parameters obtained from the two technology nodes in order to convey useful hints for the choice of the proper technology node to be used for detector front-end electronics in view of future applications in the field of HEP electronics instrumentation such as LHC upgrades.

Parallel Session A3-Readout, commissioning and integration 3 / **26**

Design and test of the final ALICE SDD CARLOS end ladder board

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The paper presents the design and test of the final prototype of the CARLOS end ladder board. This board is able to compress data coming from one Silicon Drift Detector (SDD) front-end electronics and to send them towards the data concentrator card CARLOSrx in counting room via a 800 MBit/s optical link. The board design faces several constraints, mainly size (54x49 mm) and radiation tolerance: for this reason the board contains several CERN developed ASICs. A test setup has been realized for selecting the good devices among the 500 cards already produced.

Summary:

The Inner Tracking System (ITS) of the ALICE experiment contains six coaxial cylindrical layers. Layers 3 contains 14 ladders each one hosting 6 SDDs (Silicon Drift Detectors), while layer 4 contains 22 ladders each one hosting 8 SDDs. The CARLOS end ladder board is placed on both sides of each ladder with the purpose of acquiring and compressing data coming from each SDD before sending them towards the data concentrator card CARLOSrx in counting room through optical fibers. The board contains the compression chip CARLOS that performs a bi-dimensional compression of the data coming from the SDD front-end electronics. CARLOS 16-bit output bus is encoded with 8B/10B Ethernet protocol and sent to a 800 MBit/s single mode optical fiber using a 1310 nm optical laser.
The CARLOS end ladder board receives the trigger signals and the configuration parameters through a 40 MBit/s serial signal coming from CARLOSrx through an optical fiber and converted using a photodiode.
An other photodiode is used for receiving the 40.08 MHz clock coming from the TTC system. The QPLL ASIC on the end ladder board allows to obtain a clock with a peak-to-peak jitter lower than 50 ps that is used both for the serializer (ASIC GOL) of the board and for the front-end electronics.
A special control unit has been developed with the purpose of monitoring parameters such as voltage, current and temperature related to the whole readout chain. The control unit is remotely controlled from the DCS (Detector Control System) board through the I2C bus. The CARLOS end ladder board also provides power for the analog and digital voltages of the front-end boards under the control of the DCS system.
The board has been tested using the complete setup from the front-end electronics to the data concentrator card CARLOSrx: the test of the board was successful both for

what concerns data transmission and DCS features. Beside that an FPGA based board has been developed as an emulator of the front-end boards with the purpose of generating known patterns after receiving a trigger signal: this allowed us to obtain an estimation of the optical link Bit Error Rate (BER) lower than 10-16.
The CARLOS end ladder board fulfils the requirements on space (54x49 mm with a maximum thickness of 16 mm) and on construction materials for its final use in the ALICE experiment. Up to now 500 boards have been produced and the test of the production is being carried out.

Parallel Session B7-DAQ session / **27**

The Hardware of the ATLAS Pixel Detector Control System

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The innermost part of the ATLAS experiment will be a pixel detector, built around
1750 individual detector modules. To operate the modules, readout electronics and
other detector components, a complex power supply and control system is necessary.
The unique power, grounding and control requirements are described, along with the
custom made components of our power and control systems. These include remotely
programmable regulator stations, the power supply system for the optical
transceivers, several monitoring units and the interlock system.

Summary:

The requirements of the pixel detector have made specific developments necessary for
the hardware components of the detector control system. An efficient operation
requires a preferably individual adjustment of the different control parameters.
Further design constraints are the high power density in the detector volume, the
floating grounding scheme of the ATLAS detector and the sensitivity of the read out
chips developed in deep sub micron technology. Especially the power supply system,
consisting of nearly 5000 individually controllable supply lines, requires solutions
which are adapted to the detector needs and which in parallel are economically priced.
The remotely programmable regulator stations, which are installed as close as

possible to the detector modules, provide individual floating power outputs with low
ripple to the front end electronics. At the same time they protect the sensitive
chips against transients. The internal control of the regulator station is handled by
a FPGA from Actel, while the link into the control system is handled by the ELMB, the
ATLAS wide used front end IO unit.
The design of the supply system for the opto transceiver boards is based on
components, which can directly be controlled by the ELMB. In this way a reasonable
priced solution has been found which allows individual setting and adjustment for
each of the more than thousand channels.
In the positions where common power supplies are used to provide voltages to several
loads additional monitoring units are integrated which allow to investigate the
behaviour of individual modules. The design constraints, precision and compatibility
to the ATLAS grounding scheme, are fulfilled by the presented LV and HV monitoring
systems. In this way more than 8000 monitoring channels complete the low and high
voltage system.
As specially irradiated detector modules can be destroyed by heat ups, a thermal
interlock system is developed which acts directly on the related power supplies. In
addition other equipment can suffer from extreme heat and human being must be
protected against risks due to lasers. Therefore these devices are connected to the
interlock system as well. The presented interlock matrix, whose design is based on
the use of a FPGA, allows a dedicated control of small equipment groups and helps in
this way to keep the number of channels out of service as low as possible.
All presented hardware components passed intensive electrical studies and
investigation in our system tests and are currently under production. To simplify the
production and to have an easy maintenance the systems are built in a modular way,
combining different building blocks. As everywhere the ELMBs are used for
communication, the integration into the ATLAS wide control system can easily be
performed.

Parallel Session A5-DAQ and Optical technology / 28

On the development of the final optical multiplexer board prototype for the TileCal experiment

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This presentation aims to describe the architecture of the final optical multiplexer board (also known as preROD) for the TileCal experiment. The results of the first VME 6U prototype have led to the definition of the final block diagram and functionality of this prototype. Functional description of constituent blocks and the state of the work currently undergoing at the Departament of Electronic Engineering is presented. As no board is still produced, no results are presented but, nevertheless, design issues that has been taking into account as component placement and signal integrity issues will be detailed.

Summary:

1. INTRODUCTION

The Optical Multiplexer Board (OMB), also known as PreROD, will be the module which will decide which of the two optical fibers coming from the Front-End (FE) electronics of the TileCal detector carry error-free data. This is necessary because radiation inside the detector can produce malfuntioning of the digital circuits of the FE. To solve this problem two optical fibers come out from the FE carrying the same data. Should radiation produce any error, the OMB will detect it by checking the CRC codes for the data packect and select the error-free fiber.

A first prototype of this OMB is already functioning and used for ROD commisioning tasks. This prototype only includes two input channels (4 input fibers) and two output channels (2 fibers) and is implements in a VME 6U board. A brief description of this board is presented in the next section.

1. OMB 6U prototype

The basic building blocks of the 6U prototype are:
- the VME slave controller it operates the whole board, keeping records on the number of errors detected in each channel, and sets its working mode which can be normal or

injection. This second mode allows the OMB to inject data blocks either automatically or previously loaded from VME.

- the CRC and link controller it holds two input and one output high-speed link controller and the CRC algorithm calculation and checking logic. It's connected to the VME controller for control and debug operations.

The prototype has two CRC and link controller blocks, one per input channel, and one VME slave controller.

One of the most interesting functionality of the board, provided the TileCal detector is not yet built, is the injection mode. With this mode it has been possible to carry out ROD commissioning tasks at Valencia thanks to the possibility of injecting known data blocks and the selection of trigger inputs, either internally generated or input from NIM logic.

1. OMB 9U description and current work

The good results achieved from the 6U experience are being now used to define the final OMB prototype. This prototype is conceived in a 1 to 1 ratio with respect to RODs. This is to say that each final prototype will have 8 input channels (16 fibers) and 8 output channels (8 fibers). Due to this modification a 9U format has been chosen for this new implementation.

With respect to functionality there are some minor modifications among of which, the inclusion of the TTC receiver chip is the main one. This would lead to the possibility of having trigger directly from the TTC system, something which is not possible now.

Electrically speaking the new board poses some problems related to signal integrity and component placement issues. The use of a single JTAG chain for the programming of all the FPGA chips in the board and the bus connecting the VME controller and the CRC controllers are the main issues. Simulation of this connections as well as firmware modification in the FPGA used are part of the work currently going on and that will be included in the presentation.

Parallel Session B5-Power systems / 29

Evaluation and testing of advanced low-voltage power supplies

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Following a process of proof-of-concept on the requirements for radiation and magnetic filed tolerant low-voltage power supplies to be used to power silicon detectors in LHC experiments, a common procurement action was undertaken by the experiments and PH-ESS group.

The evaluation and testing of advanced COTS radiation and magnetic field tolerant low-voltage power supplies is described. An overview of the design principles of the power supplies is given together with the test methods used and results obtained.

Summary:

Following a process of proof-of-concept on the requirements for radiation and magnetic field tolerant low-voltage power supplies to be used to power silicon detectors in LHC experiments, a common procurement action was undertaken by the experiments and PH-ESS group. Rather than making a custom design matching the electrical requirements and robust enough to work in their specific environments in term of magnetic field and radiations, it has been decided to select COTS devices following the electrical specifications, test them and adjust their design together with the manufacturer, to make them tolerant to magnetic field and radiations.

Based on the requirements of the all four LHC experiments for regulated low voltage DC power supplies, a market survey for COTS devices was thus launched. A common technical specification was established to fulfil all these requirements:
electrical, tolerance to magnetic field and radiations.

Following the market survey, two main manufacturers were selected and their equipments were evaluated.
First of all, electrical tests were performed to ensure their compliancy to the initial requirements. Several parameters were checked, such as static and dynamic regulation, ripple, efficiency, overcurrent and overvoltage protection and stability. To perform this, an in house test set up was implemented. Moreover, electromagnetic compatibility tests were performed in order to verify the harmonic rejection and the power factor.
The tolerance to magnetic field of these power supplies was then evaluated. The part of the power supply or converter intended to be magnetic field tolerant was subjected to a functional test whilst being exposed to a quoted magnetic field in a calibrated, large aperture electromagnet. The test was repeated in three axes in order to check the sensitive components in the worst condition.
Finally, CERN/PH/ESS group in collaboration with LHC experiments have organized radiation campaigns. Many tests were performed using low energy neutrons to analyze possible displacement damage (NIEL) of the control electronics and proton beam to study Single Event Effects (SEE).
If the equipments were matching most of the specifications (specifically in term of electrical parameters and tolerance to magnetic field), the tolerance to radiations was limited and required some parts of the power supplies to be redesigned in collaboration with the manufacturers.

The process of the evaluation and testing of these advanced COTS radiation and magnetic field tolerant low-voltage power supplies will be described. An overview of the design principles of the power supplies will be given together with the test methods used and results obtained.

Parallel Session A7-ASIC developments / 30

An Error-Correcting Line Code for a HEP Rad-Hard Multi-GigaBit Optical Link

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This paper presents an ASIC implementing the line encoding scheme to be used in the GBT system, a multi-gigabit optical link designed for use in future luminosity improvements of the LHC. A general overview of issues specific to optical links placed in radiation environments is given, and the required properties of the line encoding discussed. A scheme that preserves the DC-balance of the line and allows forward error correction is proposed. It is implemented through the concatenation of scrambling, Reed-Solomon error-correction and addition of an 8-bit DC-balanced header. The proposed scheme has been implemented in a fully digital chip fabricated in a 0.13um CMOS technology. Implementation details and test and simulation results are given.

Summary:

The Timing, Trigger and Control (TTC) system is an optical broadcast network used for fast timing and slow control distribution at the LHC. A possible upgrade of this system is under study for future luminosity improvements of the LHC. In the possible upgraded version the link will become bidirectional and the transceiver ASIC has been named GigaBit Transceiver (GBT). This new link will provide the system user with a 64-bit word every 25 ns, opposed to the 2 bits per 25 ns of the present TTC system.
In general, a line encoding scheme has to be built-in in the link in order to optimize the line data stream for the properties of the channel. E.g., a relatively high number of transitions on the bit stream has to be guaranteed in order to facilitate Clock and Data Recovery (CDR) and in particular for low clock jitter.
Additionally, the data stream has to be constituted, in the short term, of approximately the same number of zeros and ones for easy positioning of the decision threshold (property referred to in literature as the code being “DC-balanced”or “DC-free”). As in our application Single Event Upsets (SEUs) on the photodiode are likely to be the main source of errors, the line encoding proposed here includes an error correction scheme particularly targeted to this issue.

Commercially adopted
schemes have also been considered for our application,
even though none of them has
been found fully compliant with our needs, e.g. not
sufficiently efficient or
difficult to integrate with a sufficiently strong error correcting
scheme.
The proposed line encoding scheme addresses all the
previously summarized issues
through the concatenation of a parallel self-synchronizing
scrambler, a Reed-Solomon
error-correcting encoder/decoder and the addition of a DC
balanced 8-bit header used
for frame synchronization. Scrambling is a method of
randomizing the statistics of a
data stream which does not require an increase in
bandwidth. The Reed-Solomon blocks
add 16 redundancy bits to the 64-bit data packet, which
summed to the 8-bit header
lead to a total frame length of 88 bits. The total link speed is
about 3.5GHz and the
overall line code efficiency is about 73%. Low DC-wander
and high number of
transitions are guaranteed while being able to correct the
effects of at least one
SEU on the photodiode per 88-bit word.
A demonstrator ASIC implementing the encoding and
decoding functions has been
fabricated in a 0.13um CMOS technology. The whole encoder
block used about 1700 cells
and the decoder block counted about 5000, for a total area
of 1.3x1mm including the
36 pads. The ASIC has been successfully tested.

Poster sessions / 31

Unified C/VHDL Model Generation of FPGA-based LHCb VELO algorithms

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We show an alternative design approach for signal processing algorithms implemented on FPGAs. Instead of writing VHDL code for implementation, and maintaining a C-model for algorithm evaluation, we derive both models from one common source allowing generation of synthesizeable VHDL and cycle- and bit-accurate C-Code.
We have tested our approach on the LHCb VELO pre-processing algorithms and demonstrate comparison of data processed both off-line and on-line using the two derived models.

Summary:

The LHCb VELO uses silicon-strip sensors featuring 2048 strips per sensor. The analogue readout of each sensor is done using Beetle-chips. Digitisation and pre-processing at level-0 trigger (L0T) frequency of 1.1MHz is accomplished by the TELL1 board.
Different effects introduced throughout the analogue signal chain and the physical

layout of the sensor do require a pre-processing prior to applying a cut to separate hits from background noise (zero suppression).
This pre-processing has been implemented in FPGAs located on the TELL1 allowing the usage of elaborate algorithms for efficient zero suppression yet guaranteeing the required throughput at L0T frequency. A Software (Vetra) written in C emulating the pre-processing allows off-line evaluation of algorithms using generated or recorded data.
As implementation or modification of algorithms for FPGAs (typically using VHDL) does require considerable more time and effort than the corresponding C-code we are concerned about the consistency between the two models rendering feedback from either model useless for the other.
To overcome this limitation, we have created a model description serving as a common source from which synthesizeable VHDL-code and cycle- and bit-accurate C-code can be derived. The language used for the common description is the Confluence hardware description language.

The most important prerequisite to make the suggested scheme work in practice are reliable interfaces, which guarantee that modified models can be immediately inserted into the respective environment (C or VHDL) without the need for further manual adaptations. If this can be achieved, turn-around times for model modifications shrink considerably. Therefore effects of modifications targeting a specific issue (algorithmic, hardware-resources ⋯) on other domains can be immediately evaluated. Iteration on hardware-implemented algorithms becomes feasible.

We will present data sets taken during the LHCb VELO Detector Commissioning Challenge (ACDC2, June 2006) and processed both off-line and on-line. Results and simulation times will be compared.

Poster sessions / **32**

Electronic Devices for Controlling the Very High Voltage in the ALICE TPC Detector

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The Time Projection Chamber (TPC) is the core of the ALICE experiment at CERN. The ALICE TPC is an 88m3 cylinder filled with gas and divided in two drift regions by the central electrode located at its axial centre.
The drift field is generated by a 100kV power supply. The TPC Very High Voltage project covers the development of the control system for the power supply.
This paper reports the project progress, introducing the control system architecture from the electronics up to the control level. All the electronic devices will be described, highlighting their communication issues, and the challenges in integrating these devices in a PLC-based control system.

Summary:

The TPC is the main tracking detector of the ALICE central barrel and, together with the other central barrel detectors, has to provide charged-particle momentum measurements. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift towards the end plates of the cylinder. Moving from the anode wire towards the surrounding electrodes, the positive ions created in the avalanche induce a positive current signal on the pad plane. The readout of the signal is done by the 570132 pads that form the cathode plane of the multi-wire proportional chambers located at the TPC end plates.

Under operating conditions the system must safely apply a DC voltage of 100kV to the central electrode placed half way between the two end plates of the detector. Four resistor rods supply the proper potential to the field cage.
The Control System was developed following the TPC subsystems requirements, covering the following features: control and monitoring of the High Voltage power supply, the current in the resistor rods, the cooling, and some additional equipment. Voltage must be smoothly applied by a ramping mechanism.
The Power Supply (PS) is a Heinzinger PNC 150000 neg-2, customized for the experiment needs. It can provide up to 150kV DC. Its main modification is the addition of an electronic controller that limits the slew rate in case of sudden power up or down. It is the first time that such a high voltage power supply integrates this feature. The PS is also controlled by a RS232 interface. A Programmable Logic Controller (PLC) controls the ramping and several safety features. Thanks to its simple architecture and its stand-alone characteristic, the PLC provides more reliability than a common PC. The chosen PLC is a Schneider Electric P575634M. As it directly controls the PS through the RS232, dedicated communication routines were implemented. Currents in the resistor rods of the field cage are monitored as voltage drops over a resistor. Monitoring is performed by two ELMB reading 16 analog inputs. Each ELMB is connected to the PLC through CAN bus. The PLC controls that the voltages remain in range. Status levels of relevant parameters for the operation of the PS are monitored through 13 interlocks (digital inputs) connected to the PLC. They provide status information about cooling water, UPS, gas condition and circulation.
In case of any failure in the monitored elements, the PLC reacts by triggering a ramp down of the PS. Depending on the error level, the ramping down can be slow (PLC driven) or fast (controlled by the electronic slew rate limiter). The PLC itself is monitored by a device designed in order to trigger a hardware ramp down in case of losing the PLC heartbeat.
As the TPC is fundamental for the ALICE experiment to work, the system was chosen for the PLC reliability. Hence, special effort was put into the development of communication with the electronic devices that, in conventional systems, are usually controlled in transparent way by a common PC.

Poster sessions / 33

Development and test results of a readout chip for the GERDA experiment

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The F-CSA104 is a low noise, fully integrated, four channel preamplifier produced in the CMOS 0.6um XFAB XC06 process, which has been developed for the GERDA experiment. Each channel contains a charge sensitive preamplifier (CSA) followed by a fast differential line driver for driving a 100 Ohm twisted pair cable over 10m. It has a measuring sensitivity of 5.8 mV/fC with an expected ENC of 220e- after 20us CR-(RC)4 filtering when connected to a 30pF load and operating at room temperature. Depending on pulse rate and noise requirements the preamplifier's feedback resistor may be adjusted in fine steps from 1 MOhm to 2.2 GOhm. F-CSA104 has been particularly designed to operate in liquid nitrogen (T = 77K/-196°C).

Summary:

The GERDA experiment under construction at the Gran Sasso Laboratory is searching for neutrinoless double beta decay of 76Ge. Germanium diodes immersed in liquid nitrogen serve as sources and detectors. Since the detectors are

operated in an unprecedented low background environment the amplifiers, which are operated close to the diodes in liquid nitrogen, have to fulfil stringent requirements on low radioactivity, noise performance and be able to drive the signal off detector. The F-CSA104 has been designed to fulfil these requirements by an appropriate technology choice and optimised architecture.

The F-CSA104 has been fabricated in the XFAB 0.6 um CMOS process as it offers a large signal output voltage swing (5V operation voltage), bulk-effect-less(i.e. substrate isolated) NMOS FET devices and no noticeable noise penalty over XFAB's 0.35um CMOS technology. For the low operating temperature of -196℃ the simulation's temperature was matched to the measured device characteristics.

For the GERDA experiment it is desirable to have a completely integrated circuit so as not to degrade the radio-purity of the liquid nitrogen vessel. In particular, integrating the large feedback resistor of the CSA. However, integrating such a large resistor required the use of a substrate isolated NMOS FET operating in the sub-threshold region. Special electronic circuitry and layout has been used to allow the NMOS FET resistor to work in both signal input polarities and to maintain a reasonably accurate and stable resistance.

The F-CSA104's noise performance has been optimized for use with capacitive detectors of 1 - 100pF. Measurements have shown that a PMOS input transistor suffered less flicker noise than an NMOS; Flicker noise being the dominant noise contributor at liquid nitrogen temperatures for optimal filter constants. To minimise the thermal noise, a large width over length PMOS input transistor channel of 9000/0.6 has been implemented. Layout techniques for this transistor have been used to reduce the stray capacitance and to screen the input line from bulk noise. So as the F-CSA104 may find use in other applications where the noise matching to higher capacitance detectors is vital, an external PMOS FET may be connected to the IC and thus operates in place of the integrated input transistor.

A range of F-CSA104's parameters, including offset and preamplifier decay constant, can be programmed by I2C commands for optimisation. Further to this, several options exist to select various reference points for sensitive nodes. An example of this would be the bulk node of the input transistor which can be selected to be either supplied externally (to further reduce bulk resistance noise) or be on chip ground.

F-CSA104's linearity and offset have been designed for use with 14 bit ADC systems. Linearity requires a large open loop gain of both preamplifier and buffer core cells (120 db and 92 db, respectively). This large open loop gain also minimises signal-induced input voltage shifts (max. 0.44 uV) and thus minimises charge collection deficit. Offset cancellation is achieved by a triple DC offset suppression scheme.

The F-CSA104's measured power consumption, noise, S/N and signal output rise and fall times are presented for both room and liquid nitrogen operating temperatures. Other measurements of interest are also presented such as the power supply rejection ratio, channel cross-talk and common mode rejection ratio.

Parallel Session A3-Readout, commissioning and integration 3 / 34

Readout Electronics Tests and Integration of the ATLAS Semiconductor Tracker

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The SemiConductor Tracker (SCT) together with the pixel detector and the Transition Radiation Tracker (TRT) form the central tracking system of the ATLAS experiment at the LHC. It consists of single-sided microstrip silicon sensors, which are read out via binary ASICs based on the DMILL technology and the data are transmitted via optical fibres. After an overview of the SCT detector layout and tracking performance, the final-stage assembly in large-scale structures and the integration with the TRT is presented. The focus is on the electrical performance of the overall SCT detector system through the different integration stages, including the detector control and data acquisition system.

Summary:

The ATLAS Semiconductor Tracker (SCT) will be a central part of the tracking system of the ATLAS experiment and is one of the major new silicon detector systems for LHC. The final system comprises about 4000 individual detector modules with nearly 16000 silicon sensors and more than 6 million readout channels. It has been assembled and is currently being tested as part of the ATLAS Inner Detector Integration effort at LHC point 1. The testing of the readout and control systems constitutes one of the vital tasks for the assembled detectors.

The SCT readout system is based on the ABCD3TA, a binary ASIC designed in the DMILL technology. Each module is read out by 12 ABCD3TA ASICs mounted on a hybrid circuit. Each chip provides binary readout of 128 detector channels. The amplified and shaped input signal is compared to a programmable threshold having two components: a single 8-bit DAC applied across the whole chip, and a channel-specific 4-bit DAC designed to compensate for channel-to-channel variations. In ATLAS, an optical scheme will be used to transmit data from the detector modules to the off-detector electronics and to distribute Timing, Trigger and Control (TTC) data from the counting room to the front-end electronics. The performance of the whole chain of data and control transmission is verified in each step of the detector assembly.

After a brief overview of the SCT detector system and its expected tracking performance, the presentation will focus on the system integration of the SCT and in particular in the installation and testing of the readout system. The final stage assembly of the SCT and the final integration with the Transition Radiation Tracker (TRT) is carried out in the ATLAS SR1 clean-room. Using a silicon test system, which can characterize up to one million readout channels simultaneously, the SCT detector function and performance is tested through the different integration stages, from single barrels up to the final tests as part of the Inner Detector (ID) just before its installation in the pit. Particular attention will be given to the electronics tests results such as electrical connections checks, noise and gain measurements, as well as temperature and leakage current measurements. The outcome of these tests is essential for the validation of the grounding, shielding and cooling system. The detector control system installation will be highlighted as well.

Poster sessions / 35

Radiation tests for Slow Control ALICE TOF systems

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The read-out modules of the ALICE Time-of-flight (TOF) system will be hosted in custom VME crates near the apparatus in a moderately hostile environment.
Commercially available options to provide remote VME connection to the crate have been considered to provide slow control functionalities.

The main slow control channel will be implemented through an optical link based on the commercial cards A2818/V2718 from CAEN for front-end electronics configuration and monitoring purposes.
An additional ethernet link to an ARM CPU running Linux will be available.

Radiation tolerance test results for the critical components corresponding to the abovementioned choices will be presented, as well as estimates of the minimum time between failure while taking data.

The results presented here can be used to estimate upset rates for specific applications of commercially available VME controller cards and Single Board Computer like the CAEN V2718 and A1500.

Summary:

The ALICE Time-of-flight (TOF) system will be a large area (140 m2) detector made OF Multigap Resistive Plate Chambers (MRPC) installed in the barrel region. The read-out modules will be hosted in custom VME crates near the apparatus in A moderately hostile environment (1.2 Gy expected in 10 years of operation). Data collected will be sent to the central DAQ through the custom optical link developed within the ALICE collaboration (ALICE DDL).

The choice VME bus as the backbone to house the readout electronics ALLOWS for commercial options to provide remote VME connection to the crate and to provide slow control functionalities.
The design of the slow control system to access the VME bus while taking data has been thoroughly investigated with respect to radiation tolerance issues.

The main slow control channel will be implemented through an optical link based on the commercial cards A2818/V2718 from CAEN for front-end electronics configuration and monitoring purposes. An additional ethernet link to an ARM CPU (which will be mainly responsible for firmware upgrade), running Linux, will be available.

Radiation tolerance test results for the critical components, corresponding to the above mentioned choices, will be presented. We used, at the CRC Louvain facility, a proton beam OF 60 MeV energy. We irradiated all devices under tests with a total dose of 10 Krad. No latchups have been observed for all the components tested.

The components tested include: optical transceiver HFBR-5911L (from Agilent) coupled to two different SerDes: Pericom HDMP-1636 and Agilent PI90SD1636A.
The total cross sections of the optical link for SEU were measured : 1.9E-9 cm2 and 3.3E-9 cm2 respectively, allowing to select the more radiation tolerant SerDes for the final card. FOR all errors observed the communication was quickly re-established after a simple reset (managed by the Linux driver on the receiving PC).

The ARM processor was originally foreseen to handle firmware upgrade for TDC cards through a custom bus on the VME backplane and not to be operated while taking data and under irradiation.

Due to the fact that we measured for the ARM processor AT91RM9200 from Atmel a device cross section equal to 1.0E-9 cm2 for operating system failures, we plan to use now the card also as a backup slow control link.

For both slow control solutions we actually obtained an estimate of minimum time between failure while in data taking, which is around 20 hours for the whole TOF detector, where 72 slow control optical links will be deployed.

We then tested, for the final card, also the FPGA normally used by CAEN for the V2718 (Altera Cyclone, which has built-in CRC error monitoring for configuration bits) and different memory chips, to be used to stage data during data collection. The result for the Cyclone (cross section 9.0E-9 cm2/device) is very similar to a previous result obtained for an Altera Stratix, when normalized to the configuration bits.

Besides the specific technical solutions adopted in the final VME ALICE card (Data Readout Module, which will host other LHC specific chips, like the TTCrx), the results presented here can be used to estimate upset rates for specific applications of commercially available VME controller cards and Single Board Computer like the CAEN V2718 and A1500.

Parallel Session B3-Trigger session 3 / 36

The Octant Module of the ATLAS Level-1 Muon to Central Trigger Processor Interface

Authors: Attila Krasznahorkay[1]; Georges Schuler[1]; Nick Ellis[1]; Philippe Farthouat[1]; Ralf Spiwoks[1]; Stefan Ask[1]; Stefan Haas[1]; Thilo Pauly[1]; Thorsten Wengler[1]

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The Muon to Central Trigger Processor Interface (MUCTPI) of the ATLAS Level-1 trigger receives data from the sector logic modules of the muon trigger at every bunch crossing and calculates the total multiplicity of muon candidates, which is then sent to the Central Trigger Processor (CTP) where the final Level-1 decision is taken. The MUCTPI system consists of a 9U VME crate with a special backplane and 18 custom designed modules. We focus on the design and implementation of the octant module (MIOCT). Each of the 16 MIOCT modules processes the muon candidates from 13 sectors of the muon trigger and forms the local muon candidate multiplicities for the trigger decision. It also resolves the overlaps between chambers in order to avoid double-counting of muon candidates that are detected in more than one sector. The handling of overlapping sectors is based on Look-Up-Tables (LUT) for maximum flexibility. The MIOCT also sends the information on the muon candidates over the custom backplane via the Readout Driver module to the Level-2 trigger and the DAQ systems when a level 1 accept is received. The design is based on state-of-the-art FPGA devices and special attention was paid to low-latency in the data transmission and processing.

Summary:

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Parallel Session A7-ASIC developments / **37**

Development of a CMOS SOI pixel detector

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We are developing a monolithic radiation pixel detector using
silicon on insulator (SOI) with a commercial
0.15um fully-depleted-SOI technology
and a Czochralski high resistivity silicon substrate in place of a
handle wafer.
Nine types of SOI TEG chips
with a size of 2.5 x 2.5 mmˆ2 consisting of 20um pixels
have been designed and manufactured.
The I-V measurement, a laser light detection test and a circuit test
prove that the TEG chips function properly.
We present basic performance of the detector as well as the comparison
with simulation results.
We also report the radiation effects on the TEG chips.

Summary:

One of the most important topics in the current particle physics is
a search for Higgs particles and new physics beyond the standard model.
In the interactions involving the new particles, bottom and charm quarks and
a tau lepton play the essential role for the search.
A vertex detector placed near the beam colliding position enables
us to detect and measure the decay positions of the heavy quarks
and lepton precisely.
For example, LHC experiments employ a hybrid pixel detector (HPD)
which is a position sensitive silicon detector, a size of about 1cm x 1cm,
consisting of huge number of readout pixels of 0.1mm x 0.1mm,
each is connected to a readout LSI via a bump bonding.

For future collider experiments such as ILC, super LHC, super B factory, further improvements of the spatial resolution and radiation hardness are required, however.
The harsh requirements demand a novel vertex detector that is able to overcome the difficulty in decreasing the pixel size and thickness, and the bump bonding.
One of the candidates is a pixel detector making use of the silicon on insulator (SOI) technology.

The ionizing radiation SOI detector consists of a high resistivity monolithic Si layer in place of a handle wafer, a thickness of about 100um, overlayed by a 0.2um insulating SiO2 layer (Buried Oxide, BOX), and a thin Si film (device layer) over the BOX, in which a readout LSI is formed.
The handle wafer is used for a radiation sensor with a matrix of fully depleted diodes directly connected to the LSI through a hole in the BOX.

We are developing the SOI detector with a commercial 0.15um fully-depleted SOI technology and a Czochralski high resistivity silicon substrate.
Nine types of SOI TEG chips with a size of 2.5mm x 2.5mm have been designed and manufactured.
The I-V measurements, a laser light detection test and a circuit test prove that the TEG chips function properly.
We report the basic performance of the detector as well as the comparison with simulation results.

For the application of an SOI detector to high luminosity collider experiments in future, we need understand its radiation effects.
Some of the TEG chips are irradiated by gamma rays and proton beams, and total-dose and single-event effects on the chips are examined.
We also present the irradiation test results in terms of the threshold voltage shift, mobility degradation, 1/f noise, sensor response on the laser light and beta rays, and the single-event-upset.

Poster sessions / 38

Development and Setup of a Prototype System of Distributed Analysis for ATLAS Tier-2

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The ATLAS experiment currently under construction at CERN's Large Hadron Collider presents data processing requirements of an unprecedented scale. ATLAS will accrue tens of petabytes of data per year, distributed around the world: the collaboration comprises more than 1800 physicists from 150 institutions in 34 countries. The Distributed Analysis (DA) system has the goal of enabling ATLAS physicists to perform analysis on distributed data using distributed computing resources. Both data and resources are widely distributed throughout the world at CERN and at ATLAS Tier-1 and Tier-2 centers. Since DA system is of strategic importance there is a large development activity going on in this area: the ATLAS production system has being evolving to support the analysis jobs which will have a seamless access to all ATLAS resource, as well as another activities that aim to support user analysis by submitting directly to the separate grid infrastructures (Panda at OSG, direct submission to LCG and Nordugrid). The test of DA functionality will be addressed in

the final Service Challenge 4 (SC4), in which the system will exposed to the expected large number of final analysis users. The Spanish ATLAS Tier-2 facility formed by IFIC, IFAE and UAM groups, is participating in several aspects of the Distributed Analysis System. In support of the ATLAS DA activities the IFIC Tier-2 center has developed and deployed a local computational facility which comprises many service nodes, computational clusters and large scale disk and tape storage services. The resources contribute to a variety of activities such as the analysis center facility for the next SC4 in which the technical aspects of DA will be tested and evaluted. In this paper we describe the ATLAS DA as well as we present our experience with the deployment, maintenance and operation of the mencioned DA prototype from the whole ATLAS collaboration and from the framework of the Spanish Tier-2 users point of view.

Parallel Session A4-Optical links / **39**

Potential Upgrade of the CMS Tracker Analogue Readout Optical Links using Bandwidth Efficient Digital Modulation

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The potential application of advanced digital communication schemes in a future upgrade of the CMS Tracker readout optical links is currently being investigated at CERN. We show experimentally that multi-Gbit/s data rates are possible over the current 40 MSamples/s analogue optical links by employing techniques similar to those used in ADSL. The concept involves using digitally-modulated radio frequency (RF) sinusoidal carriers in order to make efficient use of the available bandwidth.

Summary:

Approximately 40 000 analogue readout optical links are being installed in the CMS Tracker sub-detector for operation in the LHC. Each readout link transmits data using analogue Pulse Amplitude Modulation (PAM) and has been specified to be equivalent to a baseband digital PAM system conveying 8 bits of information at 40 MSamples/s. Hence the equivalent digital data rate for the analogue optical links is 320Mbit/s. The next iteration of the CMS Tracker will be operated in the Super LHC (SLHC) environment and will have to cope with significantly increased data rates due to the foreseen tenfold increase in luminosity. The cost of the optoelectronic components represents a large fraction of the CMS Tracker electronics budget. Hence, a digital system reusing the existing components while delivering sufficient performance for SLHC operation could potentially be a cost-effective alternative to a full replacement of the installed links. The feasibility of such a conversion must therefore be explored in terms of performance that can be achieved and implementation complexity.

The theoretically achievable data rate over the existing analogue link has previously been investigated using established communication theory. This theoretical estimate has now been augmented with experimental results from characterization tests performed in the laboratory. An Agilent 4438C Vector Signal Generator was used to transmit randomly generated data through an analogue optical link, using Quadrature Amplitude Modulated (QAM) RF carriers. At the output of the optical link, an Agilent 4440A Spectrum Analyzer demodulated the signals obtained, allowing a detailed analysis of the link's bandwidth and noise characteristics. The

experimental setup and method for determining the capacity of the optical link will be described.

RF digital modulation over fiber has been experimentally proven to be a candidate for a future readout link system operating in the SLHC environment and future experiments. The first estimate of the achievable data rate based upon detailed experimental measurements will be presented, along with potential hardware implementation options for a prototype of the proposed system. Also, the difficulties associated with the proposed upgrade scheme will be reviewed and compared to the expected benefits.

The performance of future detectors will impose even greater requirements on the readout systems, with large amounts of data having to be collected and transmitted over optical fiber. Achieving higher data rates will undoubtedly require employing novel techniques derived from communication engineering and information theory. The current work represents a stepping stone to understanding the benefits –as well as limitations –of the application of such a novel data transmission concept in the context of HEP instrumentation.

Poster sessions / **40**

Time Resolution of a Few Nanoseconds in Silicon Strip Detectors Using the APV25 Chip

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The APV25 front-end chip for the CMS Silicon Tracker has a peaking time of 50ns, but confines the signal to a single clock period (=bunch crossing) with its internal deconvolution filter.
This method requires a beam-synchronous clock and thus cannot be applied to a (quasi-) continuous beam. Nevertheless, using the multi-peak mode of the APV25, where 3 (or 6,9,12,...) consecutive shaper output samples are read out, the peak time can be reconstructed externally with high precision. Thus, off-time hits can be discarded which results in significant occupancy reduction. We will describe this method, results from beam tests and the intended implementation in an upgrade of the BELLE Silicon Vertex Detector.

Summary:

The APV25 is a low-noise, radiation-hard front-end readout chip made in a 0.25um CMOS process, designed for beam-synchronous operation at 40MHz in the CMS Experiment at LHC. Each of its 128 input channels features a 192-cell analog pipeline as well as a switched capacitor filter where the weighted sum of three consecutive samples is calculated.
Using this deconvolution circuit, the preamp/shaper transfer function is essentially undone in a numeric way, which leads to just a single non-zero output value (25ns wide) compared to the shaper output which is approximately 160ns wide. Hence, it is possible to unambiguously identify the bunch crossing from which a particle originated.

If the APV25 clock and the bunch crossings are not synchronous, e.g. in case of a quasi-continuous beam, this method fails.

However, the APV25 can also be operated in a multi-peak mode where still three consecutive samples are stored in the pipeline with each trigger, but the deconvolution filter is turned off and all three samples are read out. By applying several triggers spaced by 75ns (minimum trigger distance), up to ten triplets (=30 consecutive samples) can be read out, which represent the shaper output waveform.

In order to reconstruct peak time and amplitude, a fit can be applied to each event. This method was successfully demonstrated with APV25 data obtained in beam tests and resulted in an RMS time resolution of approximately 2ns at a cluster signal-to-noise ratio of 25.

The innermost layer of the BELLE Silicon Vertex Detector at KEK (Tsukuba, JP) currently suffers from high occupancy in the order of 10%, which stems from the fact that its VA1TA readout chip has a shaping time of about 800ns. In summer 2007, an upgrade is planned for the two inner layers where the silicon sensors essentially remain the same, but the readout will be done by APV25 chips. Its faster shaper already reduces the occupancy by a factor of 12.5 (not exactly the ratio of shaping times due to deviations from the ideal CR-RC shape). By using the proposed peak time finding method, comparing the hit timing to the trigger time and discarding off-time hits, another factor of up to 8 (depending on the S/N ratio) can be gained. Hence, the projected occupancy will be well below 1% in the current environment, allowing headroom for future luminosity increase.

Obviously, a fit applied to each hit is not suitable in an experiment. Hence, we developed lookup tables which fulfill the same purpose, perform almost equal to the fit function, but much faster, and are very easy to implement in FPGAs.

Finally, we will also present the VME-based data processing boards which are called “FADCs” but actually do much more than just digitization. Several Altera FPGAs perform channel re-ordering, pedestal subtraction, a 2-pass common mode correction, hit finding (zero suppression) and time finding on the APV25 data. All functions are pipelined, such that the modules are dead-time free. Since the signals are sparsified on the module, the output data rate is considerably reduced compared to transparent readout.

Parallel Session A7-ASIC developments / 41

Irradiation of 0.13um ATLAS pixel test chip

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We present the results of irradiation tests of a 0.13um test chip containing ATLAS pixel analog front end circuits and various types of memory cells. The irradiations were carried out at the LBNL 88”cyclotron with 50 MeV/c protons and 16 MeV/c light ions for SEU studies. The front end circuits perform well up to the highest dose achieved at the moment, which is 1E15 p/cmˆ2. The linear energy transfer (LET) thresholds have been measured for SEU in five different latch structures. We plan to increase the radiation dose to 1E16 p/cmˆ2.

Summary:

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Poster sessions / **42**

Wafer test of the LHCb Outer Tracker TDC-Chip

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The OTIS-TDC is a 32 channel time to digital converter chip developed in Heidelberg for the LHCb Outer Tracker experiment.
Designed in a 0,25 μm CMOS process, it can measure times with a resolution better than 1\,ns.
As the chip is directly mounted to its board, the test have to be performed on the wafer itself.
As the testing period for 7\,000 chips was only three weeks, many test routines have been implemented on a FPGA.
The tests are described and results presented on overall yield and performance.

Summary:

The LHCb Outer Tracker consists of 55\,000 drift tubes.
The gas amplified signal created by the drift electrons is further processed by a Pre-amplifier.
The result is a pseudo LVDS signal, which is fed into the OTIS-TDC chip.
This chip was developed in Heidelberg and is produced in a 0,25 μm CMOS process.
It is able to measure the arrival time with a resolution better than 1\,ns on 32 channels simultaneously.
As this chip is directly mounted on a board, various tests have to made to ensure the functionality.

In order to test the chips within a short time period while getting a full characterization nearly all test routines were implemented on a FPGA.
The FPGA Firmware analysis the incoming data resulting in various histograms.
Only these histograms are then read out via the PCI-Bus to the PC.
To benefit from the 1\,MHz readout scheme of LHCb, the trigger, reset and clock generation were also implemented on the FPGA.

The test setup was the build using two PCs.
The first PC controlled the FPGA via a LABVIEW application.
The second PC was in charge of the infrastructure and overall control of the test.
Also running a LABVIEW application it took care of the power supply, the wafer tester itself, the measurement of the analog voltages and power consumption.
The data exchange between the two PCs was realized by using the UDP protocol

With this setup it was possible to test 47 wafer containing about 7000 Chips altogether within three weeks.
The time to test one chip alone was about one minute.
From this MPW-run we got 6000 working chips while the experiment is in need for 2000 chips.
Therefore all chips for the front-end electronics of the LHCb Outer Tracker has been produced.

Parallel Session B1-Trigger session 1 / 43

Design and Test of the Off-Detector Electronics for the CMS Barrel Muon Trigger

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Drift Tubes chambers are used in the CMS barrel for tagging the passage of high Pt muons generated in a LHC event and for triggering the CMS data read out. The Sector Collector system synchronizes the track segments built by trigger modules on the chambers and deliver them to reconstruction processors (Track Finder, TF) that assemble full muon tracks. Then, the Muon Sorter has to select the best four candidates in the barrel and to filter fake muons generated by the TF system redundancy. The hardware implementations of the Sector Collector and Muon Sorter systems satisfy radiation, I/O and fast timing constraints using several FPGA technologies. The hardware was tested with custom facilities, integrated with other trigger subsystems, and operated in a beam test. Constraints, design, test and operation of the modules will be presented.

Summary:

In CMS barrel, the Drift Tubes (DT) chambers for muon detection were designed to be used in the trigger system. The first stage of DT Muon Trigger is the Local Trigger, i.e. electronics mounted on chambers, that processes DT hits to find track segments. Local trigger data are collected by the Sector Collector (SC) system, located on detector nearby “towers”.
Each SC module handles chamber links from one sector of the detector and performs data reduction and synchronization. Spy features allow trigger data to be transmitted to the DT readout modules for inclusion in the readout data. Finally, the SC is able to return a trigger signal to each chamber of the sector, generated as a boolean function of the trigger bits received from the single chambers. In this way a sector-level complete trigger system is implemented.
SC modules are built by several units: a VME 9U motherboard, hosting a board controller device that provides the VME interface, the interconnection with the readout system and the sector trigger generation; four mezzanine cards, receiving data from the four chambers of the sector; and a fifth mezzanine card, hosting serializer (GOL) chips and the optical drivers for the fiber connection to the counting room.
In the counting room, segment data are used by the Track Finder system to build full muon tracks. In the last stage, the Muon Sorter (MS) selects the highest transverse momentum muons in the barrel region. The high redundancy and efficiency, granted by the partitioning of the Track Finder, generates, as a by-product, fake tracks. The MS can run a fake suppression algorithm that can reduce the fake track rate down to 0.5%. After fake suppression, the best four muons are selected among all muon candidates in the barrel (up to 144), according to rules that privilege high reconstruction quality and high transverse momentum.
Muon Sorter algorithms are performed in two stages, with two different hardware

modules. The first stage is based on Wedge Sorters (WS). Each WS module collects all muons found in a longitudinal 30° section (wedge) of the barrel detector and sorts up to two muons to ensure dimuon efficiency. Final sorting of the four best candidates in the barrel is performed by a single board, the Barrel Sorter (BS).
The hardware implementation of the systems profits of custom processors implemented on FPGA devices using VHDL programming. The different requirements have been satisfied with several different technology choices. The SC system is based on flash-FPGAs, ensuring high fault immunity in a moderate radiation environment. The MS system located in the underground counting room has no requirements on radiation tolerance, thus it is based on sram-FPGAs that provide very large I/O and computational power on single devices, simplifying the design of the modules.
In order to validate the designs through exhaustive tests, adapter boards were designed to emulate the final operation using custom general purpose I/O modules, Pattern Units (PU). Test setups allow data patterns to be injected at 40 MHz into boards and to read back and check outputs. Custom VME and JTAG software performs bonding checks, dynamic tests, device programming and board parameters configuration.
After stand-alone tests, modules were integrated with other subsystems to validate the interconnection and the synchronization. A full test of the DT Trigger electronics system has been performed at the CERN SpS with a dedicated muon beam pulsed at 25 ns frequency. The trigger electronics chain, comprising prototypes or final parts of the SC and MS systems, could be effectively synchronized and operated.

Poster sessions / 44

Data Acquisition and Management in the Calibration Processes of the CMS Barrel Muon Alignment System

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The CMS Barrel Muon Alignment System is composed of a series of elements - each of large quantity - to be calibrated individually and together after assembly. This requires an approach based on modular control and data acquisition hardware and software including data validation features during data taking. The measured data of all calibration steps (including full images) are stored in a database together with the final results obtained after the processing and evaluation of raw data. A dynamic WEB-based reporting tool makes it possible to follow the status of calibration and assembly, and provides an easy search for any data. In the paper this approach is shown on the example of the two main element groups.

Summary:

The CMS Barrel Muon Alignment System is composed of a series of opto-mechanical and opto-electronical elements. These elements can be arranged into two main groups, the chambers and MABs (Module for Alignment of the Barrel). The starting element of the chamber group is the light source (called “fork”) containing 10 LED light sources. The forks (1000 pieces altogether) are mounted on the barrel muon chambers (4 forks on each of the 250 chambers). The chambers are mounted on the CMS detector. The starting element of the MAB group is a 2D video-sensor that is -

together with an imaging lens - enclosed in a camera-box. The camera-boxes (600 pieces in total) are mounted on the MABs (large-scale rigid carbon-fibre mechanical support structures, 36 pieces in total). The MABs are mounted on the CMS detector in a way that the camera-boxes can observe the LEDs on the forks. The images captured by the video sensors serve as an input to reconstruct the locations of the chambers inside CMS with submillimeter accuracy.

To achieve this goal the position of the elements within the system must be known with a precision beyond the manufacturing accuracy, ie:
- the location of the centre-of-mass of the emitted light spot of the LEDs on the forks with <10 micrometer;
- the location of the forks on the chambers with <70 micrometer
- the homogeneity, sensitivity and linearity of the video-sensors with <1%
- the lens-sensor distance in the camera-box with <10 micrometer and the perpendicularity of the sensor to the optical axis of the box with <3 millirad
- the location of the camera-boxes on the MABs with <50 micrometer and 50 microrad.

Therefore each piece of all element types have to be identified, calibrated and the position of each embedded element on the enveloping object must be known and followed.
Given the large number of elements and the complexity of the system, the data handling procedures of the calibration and assembly were automated as much as possible.

Five calibration facilities have been built to calibrate the forks, the chambers, the sensors, the camera-boxes and the MABs. They are very different in size and complexity but similar in nature: in all of them LED-type light sources have to be switched on and off and driven with given current and their images have to be captured by camera-boxes. These functions are complemented -depending on the task- by other control and DAQ functions like 2D-motion table control, video-multiplexing or environmental (temperature and humidity) measurements. Therefore all the facilities are also similar from control, data acquisition and data handling point of view.

The core hardware elements of the control and data acquisition system are the microcontroller-based modular units that - together with the control software - can easily be adapted to any particular calibration step. As the primary result of all the measurements are either full video-images or light spots, the image processing and transfer solutions can be reused at each calibration step.

The intermediate and final calibration values are stored in a relational database. Each step of the calibration procedure heavily relies on the results obtained in the previous steps, so the online query and update features offered by the database system are vital to our design. A dynamic WEB-based reporting tool makes it possible to follow the status of calibration and assembly and to search for any data in an easy way without direct database-operations. In the paper these points are discussed in detail.

Poster sessions / **46**

Design and performance of a PASA for the FAST-TRD Detector of the CBM experiment at FAIR

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The Compressed Baryonic Matter (CBM) experiment is a dedicated heavy-ion experiment at the future accelerator Facility for Antiproton and Ion Research (FAIR), in Darmstadt.
A Fast Transition Radiation detector will be part of this experiment. The high reaction rates up to 10ˆ7 event sˆ-1 require electronics with fast shaping time.
A preamplifier for the FAST-TRD detector has been developed in AMS 0.35 micron technology. The ASIC has an FWHM of 70ns and noise equivalent of 445 e for a detector capacitance of 10 pF with a noise slope of 12e/ pF, fulfilling all requirements.
The chip has been produced in a MPW run and it has been tested. Simulation and measurement results agree very well. This prototype has been successfully used in a physic test beam at GSI (Darmstadt) in February 2006.
A comparison of simulated and measured performance will be presented. In addition I will report on the status of the R&D project, namely a preamplifier-shaper in IBM 0. 13 micron technology that could be used for several detectors.

Parallel Session A4-Optical links / 47

Radiation Tests of the ATLAS Inner Detector Opto-Electronic Readout System for SLHC

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The readout system of the ATLAS inner detector for SLHC will need to cope with ten time's higher radiation doses than the current ATLAS inner detector readout system. It is an open question of whether the current opto-electronic readout system could be used at SLHC. We irradiated VCSEL and Si-Pin arrays at a 20 MeV neutron beam up to the levels expected at SLHC and monitored their performance during irradiation and annealing. We performed very low dose irradiations of SIMM fibres at a gamma source. The results of these irradiations are summarized.

Summary:

Plans are being formulated at CERN for a luminosity upgrade to the Large Hadron Collider (LHC) machine. The LHC upgrade (SLHC) is being designed to increase the luminosity from 1034cm-2s-1 to 1035cm-2s-1. The expected time-scale would be around year 2015. The fluences at the SLHC will be 10 times higher than at LHC. For radii greater than 20 cm the expected fluence is 1015 hadrons/cm2. It is not clear, if the current opto-electronic components of the inner detector readout system are able to cope with this challenging radiation environment of SLHC.
Previous radiation tests have shown that the opto-electronic components can survive 10 years of LHC operation. Radiation tests by the Pixel group have demonstrated that these components can survive fluences and doses up to a factor of two higher than the SCT values.
Therefore there is an open question of whether this type of opto-electronics could be used on the upgraded SCT detector at the SLHC. This is a critical question for the design of this detector as it will have a major influence on the layout of all the readout services and therefore needs to be answered before the detector design can advance very far.
We irradiated VCSEL and Si-Pin arrays at a 20 MeV neutron beam up to the levels expected at SLHC and monitored their performance during irradiation and annealing. We performed very low dose irradiations of SIMM fibres at a gamma source. The results of these irradiations are summarized.

Parallel Session A4-Optical links / 48

Bandwidth of Micro-Twisted Cables and Spliced SIMM/GRIN Fibers and Radiation Hardness of PIN/VCSEL Arrays

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We study the feasibility of fabricating an optical link for the SLHC ATLAS silicon tracker based on the curret
pixel optical link architecture. The electrical signal between the current pixel modules and the optical modules
is transmitted via micro-twisted cables. The optical signal between the optical modules and the data acquisition system is transmitted via rad-hard SIMM fibers spliced to rad-tolerant GRIN fibers. The link has
several nice features. We will present the result of a study of the bandwidth of the link and an irradiation of
PIN/VCSEL arrays with 24 GeV protons at CERN to SLHC dosages.

Summary:

The SLHC is designed to increase the luminosity of the LHC by a factor of ten to 10ˆ35 /cmˆ2/s. The optical
components of the present pixel detector are mounted on patch panels (PP0) instead of directly on the pixel
modules. The radiation level at the optical link location is also expected to increase by a factor of ten. After
five years of operation at the SLHC, we expect a silicon component (e.g. ASIC and PIN) of the optical link to be
exposed to a maximum total fluence of 2.5 x 10ˆ15 1-MeV neq/cmˆ2. The corresponding fluence for a GaAs
component (e.g. VCSEL) is 1.4 x 10ˆ16 1-MeV neq/cmˆ2.
In the present pixel detector, the electrical signal between the pixel modules and the optical modules (opto-
boards) is transmitted via ˜ 1 m of micro twisted cables. The opto-boards contain optical packages with PIN
and VCSEL arrays to receive and transmit optical signal. Each array in an package couples to a rather robust
fiber ribbon with a removable MT connector. Each ribbon consists of 8 m of rad-hard SIMM fibers spliced to
70 m of rad-tolerant GRIN fibers.
The design of the present pixel optical links has several nice features:
• Much reduced radiation level: Since the optical components are mounted on PP0 instead of directly on the
pixel modules, the radiation exposure is much reduced.
• Separation of pixel modules and opto-boards production: The separation of the opto-boards from the pixel
modules decouples the production of both components and greatly simplifies their design and fabrication.
• Removable and robust fiber ribbon: An optical package on a pixel opto-board couples to a removable and
robust 8-channel fiber ribbon terminated with an MT connector.
For the SLHC, we would like to take advantage of the several years of R&D that produced this design.
We currently transmit optical signals at 80 Mb/s and expect to transmit signals at ˜ 1 Gb/s at the SLHC. We
have studied the feasibility of an upgrade for the silicon tracker based on the present architecture. If the
present architecture can transmit signals at the higher speed, the constrain of requiring no extra service space
is automatically satisfied. We will present our measurement of the bandwidth of the micro-twisted cables and

the spliced SIMM to GRIN fiber ribbon. In addition, we will present the results on irradiation with 24 GeV
protons at CERN to SLHC dosages for candidate PIN and VCSEL arrays from various vendors, including measurements of the single event upset (SEU) rates.

Plenary Session P6- LHC Machine / **49**

The LHC beam loss monitoring system's data acquisition card

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The beam loss monitoring (BLM) system is one of the most important elements for the protection of the Large Hadron Collider (LHC). It aims to protect the superconducting magnets from quenches and the machine components from damages, caused by beam losses. The losses are measured with ionization chambers and secondary emission monitors at likely loss locations. About 4000 monitors will be placed along the LHC mounted at the outside of the cryostats. The detectors produce a current proportional to the impacting secondary particle flux.

The acquisition cards are placed near the detectors and are exposed to particle irradiation. During the design process of the acquisition cards several irradiation tests have been carried out to verify the radiation tolerance of the chosen components.
The large variations of the quench levels with the beam energy and the particle loss duration, require the acquisition and digitalisation of the detector currents over eight orders of magnitude. The high dynamic range is covered by a current to frequency converter (CFC), which measures currents between 10 pA and 1 mA. An additional ADC measures the output voltage of the CFC to improve the data acquisition cards resolution.
The signals of eight detectors are digitalised on one acquisition card. The data, together with card status information, are transferred to the processing card via two optical links.

Poster sessions / **50**

ATLAS Pixel Detector Timing Optimisation with the Back of Crate Card of the Optical Pixel Read out System

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The ATLAS detector is one of the LHC experiments going to start data taking in 2007. The innermost subdetector of ATLAS will be a pixel detector. It consists of 1744 pixel modules which are controlled and read out via optical signals. The off detector end of the optical link is the Back of Crate card which is performing the optical-electrical conversion and adopting the timing for the detector and the readout hardware.
Studies to test the timing capabilities have been done during a combined test beam

which will be presented. Additionally information about the production of this card and the optical link are given.

Summary:

The Back of Crate card will be used in two subdetectors of ATLAS, namely SCT and the Pixel detector.
It is a 9U VME card paired to one Read out Driver each. In the pixel detector 132 Back of Crate cards will be used. The card is the electrical-optical interface between the Read out Drivers and the detector modules on one hand and between the Read out Drivers and the Read out Buffers on the other hand.
It has to control data transmitting, laser control, data receiving and recovery, and the timing of the on and off detector electronics.
The electrical-optical conversion itself is performed on plugin boards, the TX-plugins and RX-plugins, housing laser arrays or pin arrays.
The timing capabilities of the Back of Crate card are important to drive the pixel detector efficiently. The Back of Crate card is responsible for the timing of the on detector and off detector electronics. It receives the 40MHz system clock from a Timing-Trigger-Control Interface Module and copies it to the Read out Driver and to the modules.
The clock for the detector modules is encoded on the Back of Crate card with the control data for a module into one bi-phase mark signal. This signal is decoded at the on detector system and passed to the module. It enables the system to use only one optical
fibre per module to transmit the control signals and the clock. The data transmission from the modules to the Back of Crate card is done over one or two fibres per module depending on the transmission bandwidth.

The timing of the individual modules is quite important. If a read out trigger (LV1) is sent to the module, all hits registered in the clock cycle matching the trigger timestamp are read out. The hits being registered in the front end electronics have a timewalk depending on the deposited charge in the sensor. Therefore hits coming from a small charge deposition are registered significantly later than hits with higher charge depositions. If the timing is not optimised, hits will be associated to a wrong bunch crossing.
Because of cable length differences and different locations of the modules in the detector the clock timing and trigger arrival has to be adopted for each module individually, by modulewise delaying the encoded clock and data signal being transmitted to the module.

During the ATLAS combined testbeam a study of this timing functionality has been performed. It shows that it is possible to optimise the timing for the modules and therefore increase the read out efficiency.
The read out window width of 25ns is confirmed and all hits being registered in the correct 25ns wide clock cycle window are read out. Additionally an estimation about the smallest amount of charge, which is necessary to associate the hit to the correct bunch crossing, can be determined.

Poster sessions / **51**

Background for High Energy Space Instrumentation at ISS

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The aim of this paper is to present the preliminary background modelling results of the Miniature X-and Gamma-ray Sensor (MXGS) instrument in the Atmospheric-Space Interaction Monitor (ASIM). ASIM is an atmosphere event observatory with a wide energy range (from optical to gamma-ray) foreseen to be located at the external facility of the Columbus Module at the ISS in 2009.

The model takes into account the most important background sources: cosmic protons and trapped particles in the Earth Geomagnetic Field.

The preliminary results shown that MXGS will be able to distinguish between RHESSI TGF's for at least 75% of observing time.

Summary:

The MXGS instrument is a spectrometer based on a 576 cm2 CdZnTe (5 mm thickness) pixellated detector plane optimized for the energy range from 10 up to 500 keV. The MXGS main scientific objective consists on the study of the Earth atmosphere gamma ray burst, so called Terrestrial Gamma-ray Flashes (TGF) (Nemiroff et al.,1997).

The TGF expected to be observed at the ISS is 5 ms. Burst with a fluence of ph/cm2/msec/keV similar to those derived from the analysis of RHESSI data. Therefore, the MXGS sensitivity will be determined by the environment background at the ISS orbit.

The ISS environment has been simulated using the SPENVIS (ESA) and the CREME96 (NRL) tools. Decay products have been simulated using the Geant4 toolkit.

The cosmic proton flux has been simulated using CREME96 assuming a solar quiet model (absence of flares) during a solar minimum period. The integrated flux (orbit average) for the cosmic protons source in the detector is 0.14 counts/cm2/sec.

Trapped particles have been simulated using SPENVIS having as inputs the AP8-MIN and AE8-MIN trapped particle models. The main conclusion is that MXGS will be under a very high flux of trapped particles 20% of orbital time.

Protons dominates background spectra with an expected count rate from 3000 counts for deeper South Atlantic Anomaly (SAA) crossing to 8-5 counts for marginal SAA passes. The remaining components of background, like electrons and photons, are responsible of less than 20% of the expected count rate.

Finally, these preliminary results have been obtained in the ASIM mission Phase A. The current objective, to be performed during mission Phase B) is to identify the decay products from the inputs simulated in GEANT4 and to perform a detailed MXGS background model.

Plenary Session P7-Beam, SLHC & closeout / 52

Proposal for a First Level Trigger using pixel detector for CMS at Super-LHC

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A proposal for a pixel based Level-1 trigger for the Super-LHC is presented. The trigger is based on fast track reconstruction using the full pixel granularity exploiting a readout which connects different layers in specific trigger towers. The trigger will implement the current CMS High Level Trigger functionality using dedicated ASIC and FPGA, in a novel concept of intelligent detector. A possible

layout is discussed and implications on data links are evaluated. Finally the performances are shown.

Poster sessions / **53**

A Test Stand System for High-Energy Physics Applications

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The Front-End R&D group at Fermilab has been developing pixel hybridized modules and silicon strip detectors for the past decade for high-energy physics experiments. To accomplish this goal, one of the activities the group has been working on includes the development of a high-speed and high-bandwidth data acquisition and test system to characterize front-end electronics. In this paper, we present a general purpose PCI-based test stand system developed by the Front-End group at Fermilab to meet the stringent requirements of testing silicon strip and pixel detectors. The test stand is based on a platform that is flexible enough to be adapted to different types of front-end electronics. This system has been used to test the electrical performance of the electronics for different experiments such as BTeV, CDF, CMS, and Phenix. The paper presents the capabilities of the system and how it can be adapted to meet the testing requirements of different applications.

Summary:

The Front-End R&D group at Fermilab has been developing front-end electronics to meet the stringent requirements of high-energy physics (HEP) experiments. A peripheral component interconnect (PCI) based test stand was developed at Fermilab to meet the high-speed readout requirements of the electrical characterization of the silicon strip and pixel modules used in HEP experiments. This test stand is developed around a PCI test adapter (PTA). The PTA has a Xilinx Virtex4 field programmable gate array (FPGA) that gives it the flexibility necessary to meet, for example, the changing demands of the pixel module characterization (e.g., as new ICs are designed) and different applications. The data bus from the pixel modules is connected to the low-voltage differential signaling (LVDS) ports, and the data is packed by the FPGA and stored in the local ZBT memory banks until further readout by the PCI bus. A 66MHz PCI-mastering device (PLX Technology PCI9056) maps the local ZBT memory banks to the computer's memory using direct memory access (DMA). The PTA has other features such as a USB2.0 interface (useful for applications using a laptop computer) and a pair of high-speed serializers - deserializers (SERDES) used to expand the data traffic capabilities of the board. The PTA is distributed with drivers and middleware that works in both Windows and Linux environments. Data acquisition and data analysis software have been developed for both operational systems as well. Over 100 PTAs have been produced, distributed, and being used in test stands around the world. One of these applications is testing pixel modules using the third version of the Fermilab pixel chip (FPIX2).
PTA Specifications
PCI: The PTA uses the PCI9056 Bus Mastering PCI interface from PLX. The PLX9056 is a 32bit/66Mhz PCI Master that has a 32bit/66Mhz local bus.
FPGA: The PTA uses the Xilinx 4VLX25 Vertex4 FPGA. The Vertex4 series FPGA's have built in LVDS termination resistors that save PCB space and make it much easier to change designs.
LVDS Ports: The PTA has 4 I/O connectors. In the default PTA configuration the 4 ports will be configured for differential LVDS. The LVDS termination resistors can be turn on and off inside of the Xilinx FPGA: No resistors will have to be placed/removed when the PTA is used for a different test stand.
Each connector has 18 pairs of signals, and grounds. The signal pairs can be used as 18 differential pairs or 36 singled ended signals.

Memory: The PTA has two banks of 8M ZBT memory that runs up to 266MHz. The Xilinx FPGA has 1.3Mbits of memory.
USB: The PTA uses the Cypress FX2 USB2.0 interface chips. The PTA has a connector for an external power supply so it can be power out of a PC. The PC will then be able to use the PTA through the USB port. The Cypress FX2 chips have transfer rates above 20MB/s.
Miscellaneous: The PLX9056 is be able to boot the Xilinx FPGA via the JTAG port. The Virtex4 FPGA has LVDS SERDES ports. Each port has TX data and clock pairs and RX data and clock pairs. Depending on the speed grade of the FPGA, the SERDES can run up to 1Gbit/Sec.

Parallel Session B1-Trigger session 1 / 54

Integration of the CMS regional calorimeter Trigger hardware into the CMS level-1 Trigger

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The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced and tested. The RCT hardware consists of 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8 bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger after processing.

Before installation, integration tests were performed. Data was successfully received from the TPG electronics and read out with a RCT Jet Capture Card. These tests, other tests involving more trigger subsystems, their results, and the RCT installation will be described.

Summary:

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid (CMS) Experiment have been produced and the individual boards and crates validated. The RCT hardware consists of 18 9Ux680mm double-sided crates containing custom boards with custom ASICs and backplane. Including spares, almost 1800 boards of 6 different types have been produced. Included are a backplane, Clock and Control Card (CCC), Receiver Mezzanine Card (RMC), Receiver Card (RC), Electron Identification Card (EIC), and Jet/Summary Card (JSC). This

system will receive 8
bit transverse energies (ET) and a characterization bit from over 8000 hadronic and
electromagnetic calorimeter towers via 4 GBaud copper links and sum these ET's over
4x4 tower regions for jet-finding, missing ET, and total ET. Additionally, the
individual tower energies and characterization bit are used to find electron
candidates. These quantities are then forwarded to the Global Calorimeter Trigger
(GCT) for further processing and sorting.

After the production and validation of the system, and before integration with the
other trigger sub-systems, two special test boards were developed to verify the input
and output of the RCT. The Serial Test Card mimics the input from the calorimeter
Trigger Primitive Generators (TPGs). This card was used to validate the links and to
check all routes on the board that could not be validated without active links. The
Jet Capture Card (JCC) was developed to capture the output of the JSC and if needed,
generate an external trigger. Using the ability of the RCT to repeatedly cycle
through its LookUp Tables (LUTs), it was possible to validate the data paths with
changing patterns for an extended period of time.

Before the JCC long-term tests were performed, small-scale integration had already
begun. The HCAL and ECAL TPGs were each integrated separately, providing input data
to the RCT. Data was received successfully at the RCT from the TPGs on up to 24
links simultaneously. The RCT JCC was used to verify that the data was aligned in
time. Additionally, the RCT LUTs were used to send data patterns from a single crate
to the GCT for verification.

Currently, integration tests are performed in a purpose-built aboveground facility,
with a row of racks identical to what exists underground at CMS. At this facility
integration of multiple trigger sub-systems can be performed at once. The ECAL and
HCAL TPG's have now sent data simultaneously to the RCT. This was performed with a
real CMS clocking system. In this facility the RCT sent pattern data from two crates
to the GCT. After the GCT in the trigger chain is the Global Trigger (GT), where data
was seen using the JCC trigger output, using patterns generated by the RCT.

Tests to be reported on include long term tests using patterns with the HCAL and ECAL
TPGs, integrating with the HCAL TPG's in the Magnet Test and Cosmic Challenge, and

using real cosmic ray data from the detectors. The RCT will also send activity
triggers from the JCC to the GT.

Details of past and forthcoming tests and their results will be described. In
addition, the installation and integration for CMS trigger will have begun
underground, and this will be covered as well.

Poster sessions / **56**

”CMAD”, a Full Custom ASIC, for the Upgrade of COMPASS RICH-1

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In this paper we present an 8 channel full-custom ASIC prototype, named “CMAD”, designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN.

The task of the chip is amplifying the signals coming from fast multi-anode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

CMAD was developed using a 350nm commercial CMOS technology.

Summary:

COMPASS is an experiment at the CERN SPS designed to study the structure and Spectroscopy of hadrons with diverse types of high intensity beams.

One of the key components of the experimental apparatus is a Ring Imaging Cherenkov (RICH) detector, used to perform particle identification.

In order to improve the reconstruction efficiency of the RICH, an upgrade is under development. The experience gained with the first physics runs has, in fact, shown that a trigger rate of 100 kHz and a single channel rate of 5 MHz should be sustained in order to reach optimal performance.

These tight requirements can be achieved by detecting the photons produced in the sensitive volume by photomultiplier tubes equipped with fast read-out electronics. The granularity of the system demands the use of compact multi-anode photomultipliers (MPT).

In this paper we present an 8 channel full-custom ASIC prototype, named “CMAD”, which has been developed for the read-out of the MPTs in COMPASS. Produced in AMS 0.35 um CMOS technology, the chip performs binary read-out of the MPT signals. Each processing channel features in fact a low-noise transimpedance amplifier followed by a fast shaper with baseline restorer and a comparator.

The gain of the preamplifier can be adjusted from 0.6 mV/fC to 1.5 mV/fC in eight steps. This allows to compensate at least partially for the channel-to-channel gain variation of the MPTs. Additionally, the threshold of each comparator can be adjusted on a channel by channel basis via a local 8-bit D/A. The gain of the front-end and the D/A values are programmed using a digital control unit and the IC2 standard.

The peaking time at the output of the shaper is 10ns. The system has been designed to cope with a rate in excess of 5MHz/Channel.

The output pulses are stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels.

The chips have been extensively simulated and prototypes were fabricated. The chips are currently being tested and results of the measurements will be reported in the final paper.

Poster sessions / **57**

Radiation Tolerance Qualification Tests of the Final Source Interface Unit for the ALICE Experiment

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The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE sub-detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. Tests showed that configuration loss of SRAM-based FPGA devices used on the prototype of DDL SIU card was not acceptable. We developed a new version of the SIU card using ACTEL ProASIC3 device based on flash memory technology. In order to detect bit errors that occur in the embedded user memory, we implemented a parity check logic in the FPGA device. The new SIU card has been extensively tested using neutron and proton irradiation to verify its radiation tolerance. In this paper we describe the methods and the results of these irradiation measurements.

Summary:

The ALICE Detector Data Link (DDL) is a high-speed, duplex, point-to-point optical link designed to interface the readout electronics of all the ALICE sub-detectors to the DAQ computers in a standard way. The DDL consists of the Source Interface Unit (SIU), an optical cable of up to 300 meters, and the Destination Interface Unit (DIU). The DDL provides enough bandwidth to transfer data from the detectors at 200 MB/s. The SIU will be attached to the Front-end Electronics; hence it will be exposed to the radiation caused by the interacting particles. According to the latest simulations, the highest radiation level for the SIU card is expected at the inner radius of the TPC detector, where the total ionizing dose is 1.3 krad and the 1 MeV equivalent neutron fluence is 1.47 × 1011 neutrons/cm2 for 10 years of operation.

In the previous, prototype versions of the DDL SIU cards the logic functions of the DDL protocol was implemented in SRAM-based FPGA devices. According to several radiation tolerance measurements, beside single bit errors caused in the registers and in the embedded memory cells of the device, the high-energy particles may also

alter the content of the configuration memory cells of the device causing the corruption or loss of the device configuration. Therefore we changed from SRAM based FPGA to another type of logic devices, namely to an ACTEL ProASIC3 FPGA. This device is based on flash memory technology that is inherently much more insensitive to configuration loss. The first irradiation measurements carried out on the new SIU card proved that no device configuration loss occurred and the number of errors in the FPGA register cells due to the radiation also remained negligible compared to the bit-error rate always present during optical transmission. However, the number of bit errors in the embedded memory cells of the FPGA used for data buffering was too high to be left undetected. In order to detect these bit errors that may occur in these memory cells, we also implemented parity check logic in the FPGA device.

In order to test and verify this redesigned, radiation tolerant SIU card we developed and carried out several series of radiation tolerance tests and measurements. With these tests we measured the register and memory bit error rates and tested they detection in radiation environment. The series of measurements were carried out at TSL, (Uppsala, Sweden) using protons at energy of 150 MeV and 180 MeV and at ATOMKI (Debrecen, Hungary) using neutrons with spectrum extending up to En=14 MeV. The methods and the results of the measurements are shown in this paper.

Parallel Session B4-Trigger & DAQ session 1 / 58

The ALICE silicon pixel detector read-out electronics

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The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system. The SPD contains 10 million pixels organized in 120 detector modules (half staves) connected to the off-detector electronics via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the routers. This paper describes the detector readout, control and off-detector electronics.

Summary:

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system which contains 10 million pixels organized in 120 detector modules called half-staves. Each half-stave contains one multi chip readout module and two detector ladders with each 5 pixel chips bump-bonded to one sensor. The ALICE SPD off-detector electronics controls, configures and reads out the detector via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the

routers.
Each of the two link-receiver channels has three optical fibre links; two links for the clock and the serial trigger, control and configuration data and one 800 Mbit/s G-link compatible link to receive data from the detector.
The Routers receive the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip and forward the trigger commands to the pixel detector. Upon reception of the L1 trigger signal the pixel data are copied into multi-event buffers on the pixel chips. After reception of a positive L2 decision data are sent from the detector to the link receivers. On the link receiver the pixel data stream is de-serialized and stored in a buffer-FIFO before data are zero suppressed, encoded, re-formatted and written to a dual port memory. Once the link receiver has processed the data the router processor is informed to read the data from the link receiver dual port memory.
Each Router sequentially reads one event from each of the link receiver channels in order to merge data from the 6 channels and label them with trigger and status information to build one router sub event. The sub events of each of the routers are sent to the ALICE-DAQ system through the ALICE detector link (DDL). The read out data stream can also be copied to a dual port memory, where it is accessible for data monitoring and analysis via the VME-interface.
The data access for the SPD control and configuration is performed via the router VME-interface. The router converts the data to JTAG compatible commands which are sent to the detector on the optical links with a maximum data rate of 5 Mbit/s.
The full SPD read out chain was successfully operated with two half staves during a beam test in November 2004 where detector modules of all ITS systems (silicon pixel (SPD), silicon drift (SDD) and silicon strip detectors (SSD)) where installed. The functionality and the interface of the off-detector electronics to the ALICE TTC, the DAQ, a simplified version of the DCS system and the on-detector electronics were verified in a combined run with SSD and SDD during 11 hours where some 5 000 000 events were recorded without errors.
The SPD detector system including the off-detector electronics is currently pre-installed in the CERN DSF where the full detector system is integrated and commissioned before being moved to the underground area.

Parallel Session B2-Trigger session 2 / **59**

The Level-0 Decision Unit of LHCb experiment

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The Level-0 Decision Unit (L0DU) is the central part of the first trigger level of the LHCb detector. The L0DU receives information from the Calorimeter, Muon and Pile-Up sub-triggers at 40 MHz via 24 high speed optical fiber links running at 1.6 Gb/s. The L0DU performs simple physical algorithm to compute the decision in order to reduce the data flow down to 1 MHz for the next trigger level. The processing is implemented in FPGAs using a 40 MHz synchronous pipelined architecture. The algorithm can be easily configured with the Experiment Control System (ECS) without FPGA reprogramming. The L0DU is a 16 layer custom board.

Summary:

The Level-0 Decision Unit (L0DU) is the central part of the first trigger level of the LHCb detector. It is a full custom 16 layers board using FPGAs in BGA package. The L0DU receives information from the Calorimeter, Muon and Pile-Up sub-triggers at

40 MHz which arrive at different fixed times. The Level-0 sub-triggers transmit the data via high speed optical links running at 1,6 Gb/s. A total of 24*16 bits @ 80 MHz is expected as input of the L0DU while up to now 17*16 bits @ 80 MHz are used. The processing is implemented in FPGAs using a 40 MHz synchronous pipelined architecture. The L0DU latency budget is 500 ns, counted from the last arrival of the sub-triggers data. It performs simple physical algorithm to compute the decision in order to reduce the data flow down to 1 MHz for the next trigger level.
The L0DU decision is sent at 40 MHz in LVDS level to the Readout Supervisor which takes the ultimate decision to accept or not the event. The unit sends a summary block to L1 and HLT trigger for further analysis purpose. The L0DU is plugged on a TELL1 board which is the standard Data Acquisition interface module used by the sub-triggers in LHCb. The L0DU is synchronised by the Timing and Trigger Control (TTC) and is connected to the Experiment Control System (ECS) via a CC-PC. An additional USB interface is implemented for the control of the board without the ECS standard.
The internal design of the processing FPGA is composed by a Partial Data Processing (PDP) and a Trigger Definition Unit (TDU). The aim of the PDP is mainly to adjust the clock phase, perform the time alignment and prepare the data for the TDU. Moreover, the PDP implements specific functions to monitor the links and check the data time alignment.
The TDU is flexible and allows to configure through the ECS different decision algorithm with the same programmed architecture in order to answer to the need of algorithm evolution during the functioning of the detector and to adapt the algorithm parameters to the luminosity of the detector. The flexibility is introduced by the use of an internal switching matrix, AND network and OR network that are configurable via the ECS. The TDU architecture is similar to a PLD device and allows to define various trigger channels that are ORed to obtain the final L0DU decision. All the trigger channels are downscaled in order to tune permanently the 1 MHz at this trigger level despite of the luminosity decrease of the detector during run. All threshold and downscaling factors are parameterized through the ECS without reprogramming the board. The TDU also implements monitoring function in order to check the efficiency of the trigger channel and the global efficiency of the decision algorithm. The L0DU software gives the rate of trigger channel and global decision, and alarms the user if the output trigger rate is different of 1 MHz. An internal test bench is implemented on the L0DU to check the behaviour of the L0DU.

Parallel Session B4-Trigger & DAQ session 1 / 60

The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector

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The ALICE Silicon Pixel Detector contains 1200 readout chips. Fast-OR signals indicate the presence of at least one hit in the 8192 pixel matrix of each chip. The 1200 bits are transmitted together with data on 120 optical links using the G-Link protocol. The Level 0 Pixel Trigger System extracts and processes them to deliver an input signal to the Level 0 trigger processor within a latency of 800 ns. The system is modular and based on FPGA devices. The architecture allows the user to define and implement various trigger algorithms.

Summary:

The ALICE [1] Silicon Pixel Detector [2] data stream includes 1200 Fast-OR signals indicating the presence of at least one pixel hit in each of the detector readout chips [3]. This information is used in the ALICE Level 0 trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs [4].
A Pixel Trigger System has been designed to extract the Fast-OR signals from the optical data lines and process them to provide an input signal for the Level 0 trigger decision in the ALICE Central Trigger Processor. The modular electronic system satisfying the requirements is described in this paper.
The input to the Central Trigger Processor is to be provided in about 800 ns from the interaction time. This latency budget is largely used for the Fast-OR generation, the serialization-deserialization of the data and the optical transmission from the detector to the trigger system. Only a small fraction of the latency is available for the extraction and processing of the signals. A careful choice of the degree of the parallelism of the data flow is required to comply with the short latency budget while maintaining a reasonably limited number of data lines.
The Pixel Trigger System does not affect the Silicon Pixel Detector readout system. The detector data stream is divided into two optical readout lines by passive optical splitters. One output is sent to the data readout modules in the counting room. The other one is connected to the optical inputs of the Pixel Trigger System, located in the vicinity of the Central Trigger Processor.
Ten optical input boards extract the Fast-OR signals, each one receiving 120 Fast-OR bits from twelve detector modules every 100 ns. The input boards are based on optical receivers, dedicated G-Link ASIC decoders and one FPGA. Prototype G-Link receivers using only FPGAs containing on chip decoders have also been realized and tested. They did not satisfy the latency constraint.
The 1200 extracted signals are transferred to a processing board by time division multiplexing on 600 dedicated lines. Optional high speed serial output links are provided on the optical input boards. The Fast-OR signals are processed in a FPGA with a large number of input-output pins. The output of the processing unit is then transmitted to the Central Trigger Processor.
The system architecture is independent of the processing algorithm. A set of different algorithms for the generation of the input to the Level 0 trigger is foreseen. They are based on the topology of the event or on the occupancy. The system allows remote configuration of the processing FPGA to enable the definition and implementation of the algorithms by the user. Remote control, monitoring and configuration of the system are provided by a dedicated processor on the processing board. Communication with the control room is via an Ethernet link.

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Poster sessions / 61

A high level modelling approach to design and manage 18 electronics configurations used for the ECAL's endcaps hardware design

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The ECAL sub detector of the CMS experiment is composed of one barrel and two endcaps. The crystals of the endcaps are arranged on an X-Y grid. Mapping signal clusters on to the eta-phi coordinate system required for the trigger therefore presents a problem. The 48 channels Trigger Concentrator Card (TCC48) is designed to compute the trigger primitives of the different parts of each endcap sector. Each card has to support 18 electronics configurations. Based on FPGA devices, an architecture supporting all possible configurations in one design will be presented. An automated approach to extract all configurations for each trigger tower will be described in this contribution. It will also be shown how a high level model based on SystemC language is used to cover all modelling and simulation aspects.

Summary:

For each crystal inside the ECAL sub detector, the very front end electronics board (VFE) provides a digital version of the output signals form. Because of the endcaps geometry, the deposited energy is not summed over 25 crystals like in the barrel, but over 5 sets (pseudo strips) of 5 crystals. The results are sent by 5 high-speed links to the off detector TCC48 board. As a consequence of the eta-phi geometry of the trigger tower, the trigger tower signals are defined using a different association list (18) of pseudo strip signals depending on the phi sector. Moreover each endcap phi sector is split into an inner and an outer part. The full architecture requires 72 cards for the endcaps detectors.

- For each trigger tower of each inner and outer part of each phi sector, the pseudo strips association list is extracted from a database. From this information, a software algorithm is applied to define the right effective hardware structure. Without any manual intervention, it allows specific parameters association into a predefined generic hardware model. In addition, with this approach, a unique type of electronics card and its associated firmware can be used to cover all the configurations providing an easy maintainability of the system.
- Modelling and simulating a design that has to take into account a large set of parameters is a real problem. An approach is to use a high level modelling language like SystemC. With the NEPSYS tool from PROSILOG, we use SystemC to model efficiently and simulate our design. A close collaboration with PROSILOG to help us and include our requests in their products has been a key point to achieve our goals. The specific aspects of this design are supported by NEPSYS.

This presentation will describe a solution for an efficient modelling and simulation of a complex electronics card that must respond to many different configurations. Automated parameters extraction, hardware structure fitting and the high level modelling, experimented in this design will be presented.

Parallel Session B7-DAQ session / 62

Algorithms in the ROD DSP of the ATLAS hadronic Tile Calorimeter

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The hadronic Tile Calorimeter of ATLAS generates ˜10000 digitized pulses of 10-bit samples spaced in time 25 ns. In order to read-out and process these data the Read Out Driver boards (RODs) are equipped with real time fixed-point Digital Signal Processors. The processed information is sent to the second level trigger. This paper explains the performance of an algorithm to reconstruct the amplitude of the pulse, which is proportional to the energy deposited in the calorimeter, and an algorithm to identify muons of low transverse momentum. Comparisons of simulated processing time and time measured in the laboratory are shown for both algorithms. We also compare the precision on the energy calculation with the precision obtained with other algorithms executed in floating-point processors. Efficiencies and fake rates of muon identifications are also shown in this paper.

Summary:

The hadronic Tile Calorimeter of ATLAS (TileCal) is a sampling calorimeter made out of iron as absorber material and plastic scintillating plates as active medium. The light produced in the scintillating tiles is collected through wavelength shifting fibers and read-out by photomultipliers. The analogue electrical signal of the photomultipliers is digitized in 10-bit samples taken each 25 ns which is the latency of an LHC bunch crossing. Therefore, the ˜10000 photomultipliers of the calorimeter produce up to ˜164 Gbps of data. These data are read-out and processed by the Read Out Driver boards (RODs) of the TileCal back-end electronics. The RODs are equipped with the TMS320C6414 Digital Signal Processors (DSPs) of Texas Instruments in order to execute energy reconstruction algorithms in real time. The aim of this is to provide information about energy deposition in the calorimeter to the second level trigger. The latency of the second level trigger is ˜10 microsec

thus the main requirements of the algorithm are the processing time and the precision on the reconstructed energy. Besides the energy reconstruction algorithm the ROD implements additional algorithms to provide useful information to the second level trigger. We propose in this paper a fast algorithm to tag muons of low transverse momentum (pT) inside the calorimeter.

The front-end electronics of TileCal is designed to produce pulses with an amplitude proportional to the energy deposited in the active medium. The algorithm that we propose for the energy reconstruction is the so called Optimal Filtering (OF). OF reconstructs the amplitude of the photomultiplier signal by means of a weighted sum of the digital samples. The weights are obtained from the pulse shape of the photomultipliers and the noise autocorrelation matrix. The process to calculate them minimizes the effect of the noise in the amplitude reconstruction. Optimal Filtering also reconstructs other magnitudes related to the signal such as timing and pedestal through different weighted sums of the samples. Additionally to Optimal Filtering, a fast muon tagging algorithm,the MuTag algorithm, is also implemented. The aim of the MuTag algorithm is to make up for the lack of efficiency in the standalone muon spectrometer trigger for soft muons (pT < 5 GeV/c) which are characteristic of some interesting B-physics channels. The MuTag algorithm seeks energy deposition patterns inside a module of the calorimeter using the energy previously reconstructed with Optimal Filtering.

This paper explains the performance of both algorithms in the ROD DSPs. The TMS320C6414 DSP is a real time fixed-point processor which performs up to 32-bit data Multiply and Accumulate (MAC) instructions. We use low level functions in oder to reduce the processing time. We compare the processing time obtained from the simulation with the one measured in the laboratory. The precision on the reconstruction is also compared with the one obtained with other algorithms, for instance, the fit of the photomultiplier signal or the same weighted sum calculated in a floating-point processor. This paper also shows the study of the processing time of the MuTag algorithm as well as its efficiency and fake rates calculated with Monte Carlo data and its online performance with cosmic muons.

Parallel Session A1-Readout, commissioning and integration 1 / 63

The Front End Electronics of the Scintillator Pad Detector of LHCb Calorimeter

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In this paper the Front End electronics of the Scintillator Pad Detector (SPD) is outlined. The SPD is a sub-system of the Calorimeter of the LHCb experiment designed to discriminate between charged particles and neutrals for the first level trigger. The complete system design is presented, describing its different functionalities implemented through three different cards and two ASICs. These functionalities are signal processing and digitization, data transmission, interface with control and timing systems of the experiment, low voltage power supply distribution and monitoring. Special emphasis is placed on installation and commissioning subjects such cabling, grounding, shielding and power distribution.

Summary:

In this paper we will present a system level design view of the Front End electronics of SPD. The detector uses scintillator pads readout by wavelength shifting fibers that are coupled to 64 channel MaPMT (Multianode Photomultiplier) via clear plastic fibers. MaPMT are placed at the top and at the bottom of the detector. Electronics comprise a Very Front End (VFE) card with the fast readout electronics, a Low Voltage (LV) distribution and monitoring card and a Control Board (CB) to connect the VFE and LV cards to the Experiment Control System (ECS). Grounding, shielding and power distribution is also described.

The VFE card hosts the MaPMT and performs the particle type discrimination. The signal processing is performed by eight ASICs of eight channels each which integrate the signal, perform pile-up compensation, and compare the level obtained to a programmable threshold. An FPGA programmes thresholds and pile-up subtraction levels. Four LVDS serializers send output data to the Calorimeter Front End Racks, placed on a platform over the ECAL. The challenging requirements on distance, about 30 m for VFE cards on SPD bottom, and on data rate, 280 Mbits/s per pair, made necessary the development of a special method to compensate the skew. Combining this method with frequenxcy response equalization, a high performance copper link is obtained (up to 5 Gbits/s over 30 m), using simple electronics and standard Local Area Network cables.

The LV card is based on CERN-ST Radiation Hard low drop-out regulators. The complex power requirements of the VFE card makes necessary the use of several regulators per card and advises monitoring to be integrated in the same board. This is done using an FPGA which performs periodic analogue readouts of voltages and currents. LV card also performs temperature measurements using onboard probes and probes embedded in VFE cards.

The CB card is designed to deliver ECS interface, clock, and TFC signals to the VFE and to LV cards. It includes an SPECS (Serial Protocol for the Experiment Control System) mezzanine board to communicate with the ECS. It can interface up to eight VFE or LV cards. A custom delay chip (1 ns step) performs fine phase tuning of LHC clock for each VFE card independently. CB also participates in the level zero trigger by

computing the SPD multiplicity with the trigger data coming from PreShower Front End card, sending the result to the trigger system in the barracks through an optical link.

Interconnection of the three sets of boards and the corresponding power supplies turns grounding a relevant issue. The calorimeter ground configuration is a heavily interconnected ground network (mesh structure). The main power supplies are floating and the ground connection is done at the load (LV and VFE cards) to avoid returning currents through the ground network. It is intended to minimize the current return through the ground network using separated connections for ground and for the current return (neutral conductor) of each power supply.

Parallel Session B2-Trigger session 2 / 64

The Level-0 muon trigger for the LHCb experiment

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The Level-0 muon trigger looks for straight tracks crossing the five muon stations of the muon detector and measures their transverse momentum. The tracking uses a road algorithm relying on the projectivity of the muon detector. The Level-0 muon trigger analyzes every LHC bunch crossing. It handles about 130 GBytes per second. It finds muon tracks for a bunch crossing in about one microsecond. The architecture is pipeline and massively parallel. The processor is based on high speed optical and copper links, custom backplane as well as on the Stratix GX family of FPGA.

Summary:

The Level-0 trigger is an important part of the LHCb trigger reducing the bunch crossing rate from 40 MHz down to 1 MHz in less than four microseconds. It is composed of three sub-triggers: the Level-0 calorimeters trigger, the Level-0 muon trigger and the pileup system.

The muon detector is composed of five tracking stations equipped with 1368 Multi-Wire-Proportional-Chambers and 24 triple-GEM chambers. Each station is divided into four regions, with increasing distance from the beam axis. The chamber topology is complex depending on the station and on the region occupied. In addition, chambers are equipped with pads or strips. The layout of the channel is projective to ease the Level-0 muon trigger processing. The latter receives 25,920 bits every 25 nanoseconds.

The muon detector is divided in four quadrants. Each quadrant is connected to a Level-0 muon processor. These four processors are identical. They are composed of twelve processing boards, a controller board and a custom backplane. A processing board houses four processing elements, a best candidates selection unit and a credit card PC. A processing element analyzes the data coming from a “muon tower” corresponding to 1/48 of a quadrant. It is connected to the five muon stations through eight high speed optical links running at 1.6 Gbps. A processing element is embedded in an FPGA from the Stratix GX family. Processing elements have to exchange a huge number of logical channels to avoid inefficiency on the border of a tower. Copper serial links running at 1.6 Gbps are used between processing elements and on a custom backplane.

All boards are in production now. A processing board, the key element of a processor, is a 9U board with a width of 220 mm. It contains five Stratix GX, about 1500 components and seven pressfit connectors. The printed circuit is made of 18 layers. The minimal size of the track and the minimal distance between two tracks is

120 microns. The total number of links running at 1.6 Gbps is close to 100. The impedance of these tracks is controlled within 10%. High speed serializers and de-seriliazers are those embedded in FPGAs.

Dedicated software tools have been developed to handle the complexity of the data flow. Dedicated tests have been prepared to validate boards during production and to validate a processor in our institute before its installation at CERN.

Parallel Session B7-DAQ session / **65**

New RPC front-end electronics for hades

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Time of flight detectors are used for both particle identification and triggering. RPC detectors are becoming widely used because their excellent TOF capabilities and reduced cost. The new ESTRELA Resistive Plate Chamber (RPC) detector, which is currently being installed in the HADES detector at Darmstadt GSI, will contain 1000 RPC modules, covering a total active area of 8 m2. It has excellent TOF and good charge resolutions. Its Front-End electronics is based on a 8 layer Motherboard (MB) providing impedance
matched paths for the output signals of each of the eight 4-channel Daughterboards (DB) to the TDC.

Summary:

HADES is a High Acceptance DiElecton Spectrometer currently installed at GSI Darmstadt (Germany), which has as main goal the detection of electron pairs produced in relativistic pion-nucleus and nucleus-nucleus collisions, with high invariant-mass resolution and high acceptance, to obtain information about the modification of the properties of vector mesons in nuclear matter, both normal and hot and compressed. HADES consists of several subdetectors providing triggering, and particle identification and discrimination capabilities. Among these subdetectors there is a TOF system, built of plastic scintillator rods read by photo-multiplier tubes at large angles and of Resistive Plate Chamber (RPC) detectors at low angles, where the particle rate is low enough. This new low angle ESTRELA detector, which has recently been approved, covers a polar angle between 18 and 85 deg. with 2pi azimuthal acceptance, and consists of a RPC wall containing 1000 double-sided

readout detectors (2000 channels) distributed in 6 sectors, covering an active area of 8 squared-meters.

The Front-End electronics consists of 2 kind of boards: 4-channel daughter boards (DB) and 32-channel motherboards in which 8 DB are allocated. Accurate timing measurement are performed by adjustable threshold discriminators.

The charge of RPC signals are measured from the time-over-threshold of the integrated signals (with sliding reference threshold in the next upgrade) via a comparator with latch-enable, and are encoded as LVDS signals. Output signals contain information about both detection time and ionization charge. Time information is given by the rising edge of the output signal, which gives the detection time. Charge information is given by the width of the output pulse. The 6-layer DB boards provide a digital LVDS output signal containing accurate time and charge information in a compact design, using a reduced number of commercially available and inexpensive components.

The MB is a 8-layer board providing voltage regulation. Stable thresholds for time-of-flight and time-over-threshold are set by DAC circuits daisy-chained on the motherboard and remotely programmable by Serial Peripheral Interface. A 3-stage circuit of summing operational amplifiers generates a multiplicity signal to be used for low level trigger purposes.

The motherboards are 8-layer PCBs, use the novel technique of plugged vias and are completely impedance matched to reduce signal reflections and distortions. Connectors have been carefully selected, and are high frequency, differential and impedance matched.

Measurements for both electronic pulses and gamma ray sources show, respectively, about 15 ps (for pulses above 100 fC) and 40+-5 ps TOF resolutions values. Studies of data with several channels firing simultaneously show levels of cross-talk below 1% for a threshold of 25 fC, and a worsening of the time resolution of 10 ps at most. Recent data for cosmic rays and secondaries from 1 GeV C-C collisions show efficiencies larger than 90% and a time resolution about 75 ps (including the detector response).

Plenary Session P3-Optoelectronics / 66

State of the art technologies for front-end hybrids

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Co-authors: A. Gris [1]; A. Teixeira [1]; D. Berthet [1]; E. van der Bij [1]; S. Ferry [1]

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The front-end hybrids for solid state and gas detectors will be crucial components
of the next generation detectors. Requirements such as high-density and high-speed
interconnects, low mass, radiation resistance and high-current and high-power
dissipation capabilities are examples of the challenges to be solved concurrently.
Over the past ten years we have been working on these problems for a variety of
projects.

The technologies for front-end hybrids developed at CERN are presented and future
possibilities such as embedding active and passive circuits are described. Comments
are made concerning the ability to access these technologies for large scale
production by industry.

Summary:

The front-end hybrids for solid state and gas detectors will be crucial components
of the next generation detectors. There are many different technologies that can be
used to make those circuits that interconnect the different components.
Unfortunately low cost conventional PCB technology shows rapidly its limitations
when high pin count components, high density connectors or chips without packages
are used.

Other technologies such as HDI, MCM/D and MCM/C can increase the density but also
have their weak points. Another way to increase the density without impacting too
much the costs is to split the boards and to keep the high density only there where
it is needed, for example with pitch adaptors.

As the front-end hybrids carry many signal lines in a small area other problems due
to high speed signals arise such as crosstalk. Apart from optimising the layout of
the signal lines, care should be taken to choose good dielectrics (low loss) and
metals (skin effects).

Increasing density will often create thermal management problems as the space
available for heat sinks decreases and the power density increases. There are many
ways to place thermal management devices in these modules for which each time the
three ways of power cooling (convection, conduction, and radiation) should be
considered. The heat sink material itself is often also an issue.

With the need for circuits with a very low mass as not to influence particles in

their trajectory, HEP front-end electronics differs from modules usually made by
industry. To this end CERN has developed a unique process to fabricate multi-layer
circuits from polyimide with aluminium conductive layers instead of copper. This
process has been used to make circuits for the ALICE pixel detector and for low
mass aluminium cables carrying power and data.

To increase the density in commercial applications, industry is developing methods
to embed passive components such as resistors and capacitors directly in the
circuit board. Even several methods for embedding active components have been
tested with good results but they need special treatment of the dices. It is also
possible to stack active silicon dies. The way of building these blocks is the
basis of embedding active components in PCBs.

Many of these highly advanced technologies are attractive for front-end
electronics. However, mass production of them is not easy as our experience with
specialised companies has shown. Technology transfer and collaborations are crucial
to make mass production a success.

Poster sessions / **67**

Optical pattern generator board

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The GPL board is an optical pattern generator for the L0 Decision Unit (L0DU). Its design is based on three FPGAs in BGA package which can send 24*16bits @ 80 MHz via 24 optical fiber link running at 1.6 Gb/s. One FPGA is used for the control of the board, via USB or through L0DU, and two processing FPGAs are used to control the optical channel. Each processing FPGA controls twelve deserializers which send the data to an optical transceiver. The GPL board is a 16 layer custom board.

Summary:

The GPL board is an optical pattern generator used for the external test bench of the Level0 Decision Unit. Its design is based on three FPGAs in BGA package which can send 24*16 bits @ 80 MHz via 24 optical fiber link running at 1.6 Gb/s.
One FPGA is used for the control of the board and two processing FPGAs are used to control the optical channel. Each processing FPGA controls twelve deserializers which send the data to an optical transceiver. For stand alone test purpose, an additional single optical channel transceiver is implemented. The GPL board is synchronized by the Timing and Trigger Control which delivers, through the TTC mezzanine and the QPLL, the clock reference with low jitter required by the

deserializers. A 32 bit LVDS input is implemented in order to receive the Readout Supervisor word from the L0DU. The acquired data is saved and compared to the expected results to elaborate the diagnostic of test. The GPL board allows to emulate the full L0DU environment at laboratory and will be the same rack of the L0DU for the commissioning test.
Two tests mode are foreseen. The first one consists in sending a 16 bits counter one every optical fiber link in order to qualify the bit error rate of each optical fiber link. The second test, the content of FPGA's internal memory or external memory is sent to the L0DU to check the behaviour of the L0DU. This mode allows testing the L0DU algorithms with realistic data generated from a sample of simulated physics events, and check the behaviour of the L0DU when erroneous data or optical transfer errors are introduced in the data flow.
To control the board, two interfaces are provided. The first one is an USB interface based on a commercial device, which allows to connect the board directly to a PC to configure the board. The second one is done through the L0DU and the CC-PC of the TELL1 board. In this configuration, the GPL board is seen as a part of the L0DU and can be controlled and configured by the Experimental Control System (ECS).
The same software interface is used to configure both boards. It allows to easily set up the internal register and the pattern RAM with graphical panels and to analyse the test results. The L0DU environment in the LHCb experiment could be emulated by the GPL board which is a 16 layer custom board.
It is the central part of the external test bench of the L0DU. It allows to qualify the bit error rate of each optical fiber link on the receiver side and to emulate the L0DU input informations which are sent by the L0 sub-triggers.

Poster sessions / 68

The Level-1 Global Trigger for the CMS Experiment at LHC

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The trigger of the CMS experiment consists of two stages: the first stage, or Level-1 Trigger is implemented in hardware processors while the second stage, or High-level Trigger is implemented in software running on a computer farm. The Level-1 Trigger has to deliver a trigger decision for each LHC bunch crossing, i.e. at a rate of 40 MHz. The Level-1 Global Trigger uses objects supplied by the calorimeter and muon trigger systems. Its decision is based not only on energy and momentum thresholds but also on complex event topology, making use of space, charge and quality information calculated by the Global Calorimeter and Global Muon Trigger electronics.

Summary:

At the CMS experiment, the event rate at the nominal LHC luminosity will approach 1 GHz (about 20 events at each "bunch crossing"

every 25 ns). This enormous rate will be reduced to the data taking capacity of 100 Hz in a two-stage process, where the first, hardware-based stage of the "Level-1 Trigger"has to reduce the rate by a factor of 10,000 to below 100 kHz. Due to the limited length of the digital pipelines in the various subdetectors, the Level-1 trigger decision must be available within 3.2 microseconds. The Level-1 trigger and therefore also the L1 Global Trigger will operate in an intrinsically dead-time free, synchronous mode, where a yes/no decision is calculated for each bunch crossing and becomes available at a fixed delay after the event.
Information from calorimeters and muon triggers systems is used to calculate this decision for up to 128 different trigger algorithms, which are calculated in parallel. Different downscaling factors can then be applied to these 128 trigger bits, which are subsequently combined into a single decision ('FinalOr'). Based on this decision, a "Level-1 Accept" trigger signal is issued if all parts of the CMS detector and read-out systems are ready to accept a trigger.
The primary trigger objects are electrons or photons, muons, taus, jets, and very weakly interacting particles detected indirectly through missing transverse energy. Muons are detected by three systems built up of drift tubes, cathode strip chambers, and resistive-plate chambers. The information from these three systems is combined in the "Global Muon Trigger"(GMT), which also receives information from the calorimeters to see if a muon candidate is isolated or not, and if it corresponds to a minimum-ionizing particle. Information on all other particles is yielded by the electromagnetic and the hadronic calorimeters and combined first in the "Regional"and then in the "Global Calorimeter Trigger".
The hardware of the Level-1 Global Trigger consists of custom-built VME modules using FPGA technology, which are housed in one 9-U VME crate together with the module of the Global Muon Trigger and the central trigger control module. Signals from the muon systems are received by the GMT module while signals from the calorimeters are sent to "Pipeline Synchronizing Buffer"input modules, which assure that all signals referring to one particular event enter the "Global Trigger Logic"(GTL) module at the same time. All trigger algorithms are

implemented in the
firmware loaded into the FPGAs of the GTL module and may thus be changed at
any time. The “Final Decision Logic”module combines the trigger bits
calculated by the GTL as well as “technical”trigger bits sent by other
systems (for purposes of calibration etc.) after applying the individual
downscaling factors and sends its decision to the “Trigger Control System”
module (TCS), which also receives information on the state of the various
subsystems (“ready”, “busy”, “overflow warning”, “error state”etc.) and
then issues a “Level-1 Accept”(L1A) signal if a trigger is requested and
the detector is ready to accept it. Eight independently running control
units (PTC) allow to combine subdetectors to groups during calibration and
test periods.

Plenary Session P7-Beam, SLHC & closeout / **69**

Beam Phase and Intensity Monitor for the LHCb experiment

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The LHC RF clock is transmitted over kilometres of fibre to the experiments where it is distributed to thousands of front-end electronics boards. In order to ensure that the detector signals are sampled properly, its long-term stability with respect to the bunch arrival times must be monitored with a precision of <100ps. In addition it is important to monitor the LHC bunch structure and the trigger conditions by measuring the intensity of each bunch locally in the experiment.
For this purpose a beam phase and intensity acquisition board (BPIM) is being developed for the Button Electrode Beam Pickups which will be installed on both sides of all the LHC interaction points. The board measures the two quantities per bunch, and processes and histograms the information in an onboard FPGA. The information is read-out by the Experiment Control System and directly fed to the LHCb Timing and Fast Control system.

Summary:

The LHC bunch clock frequency of 40 MHz is transmitted to the experiments via a network of optical fibres which is partly based on non-phase-stabilized fibres. In the case of the LHCb experiment the non-phase stabilized distance is about 4.6km. In LHCb the bunch clock is locally distributed by the Timing and Fast Control system to all the detector front-end electronics where it is used to sample the detector signals. In order to sample the detector signals, which typically have a maximum plateau of a nanosecond, at the optimum point, the timing system provides several means of making a complete timing alignment at the level of 50ps. Since the LHC

fills are expected to last for more than ten hours, it is of extreme importance that the phase of the LHC clock remains stable with respect to the bunch arrival times. However, several effects such as temperature variations influence the phase. Measurements show that the time drift on the transmission fibres could be as large as 200ps over a period of 24 hours, and up to 8ns have been observed over a period of a year. Clearly the phase must be monitored and regular timing alignments must be performed.

In order to monitor the bunch arrival times with respect to the clock a special Button Electrode beam pickup will be installed 180m away from the interaction points on each side. Since the pulses of the four buttons of each pickup will be summed, the signal per crossing becomes independent of the position of the beam and thus also allows measuring the currents of the bunches. This is of high interest since the LHC bunch structure can be monitored and the bunch currents can be correlated with the actual physics triggers.

The current paper proposes a beam phase and intensity acquisition board (BPIM) capable of performing the two measurements per bunch crossing. The analogue unit of the board consists of a separate circuit for the phase measurement and the intensity measurement. Since the shape and the amplitude of the pulse will vary, the phase measurement circuit contains a special pulse detect circuit which is independents of the shape, and the intensity measurement circuit contains a programmable gain amplifier. The digital processing of the board is based on an FPGA which performs response linearization, averaging and histogramming in the memory of the FPGA of the measurements. The control interface is based on an embedded Credit-Card-sized PC from Digital Logic. The controller has Ethernet and is one of the standard interfaces to the Experiment Control System in LHCb. The control of the analogue circuits, such as gains and thresholds, is handled through the FPGA. In addition to reading out the measurements via the control interface, they are also output on the front-panel of the board at 40MHz with LVDS. The latter allows directly interfacing the board to the Timing and Fast Control system in order to add the bunch current information to the data of each event.

The board is in development. A first full design has been made and simulated. One of the authors has also implemented and tested the design in the context of an intensity monitor for the CERN PS accelerator.

Parallel Session B3-Trigger session 3 / 70

Commissioning of the ATLAS Level-1 Central Trigger

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The ATLAS Level-1 Central Trigger consists of the Central Trigger Processor (CTP) and the Muon to Central
Trigger Processor Interface (MuCTPI). The CTP receives trigger information from the Level-1 Calorimeter
Trigger system directly, and from the Level-1 Muon Trigger systems through the MuCTPI. It also

receives
timing signals from the LHC machine, and fans out the Level-1 Accept signal, together with additional timing
and control signals, to all sub-detector systems. From them, it collects BUSY signals in order to throttle the
Level-1 Accept generation. Upon Level-1 Accept, the trigger systems send Region-of-Interest information to
the Level-2 Trigger system.

The systems are in part already installed in the ATLAS underground counting rooms. We present their current
status, both in hardware and software, and the different commissioning steps that have led to it. Particular
emphasis is put on the integration of the Central Trigger with the Muon and Calorimeter Trigger systems, the
Level-2 trigger, and the read-out part of the different sub-detectors. We describe what has already been
achieved, what we have learnt, and the future steps we will take in order to arrive at a fully functioning
system.

Poster sessions / **71**

The LHC Beam Loss Monitoring System's Surface Building Installation.

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The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is presently based on the Beam Loss Monitoring (BLM) system. At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary. The BLM system can be sub-divided geographically to the tunnel and the surface building installations. In this paper the surface installation is explored, focusing not only to the parts used for the processing of the BLM data and the generation of the beam abort triggers, but also to the interconnections made with various other systems in order to provide the needed functionality.

Summary:

The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is presently based on the Beam Loss Monitoring (BLM) system. At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary.

The BLM system can be easily sub-divided geographically to the tunnel and the surface building installations. It consists of around 4000 detectors, placed at various locations around the ring, tunnel electronics, which are responsible for acquiring, digitising, and transmitting the data, and surface electronics, which receive the data via 2km optical data links, process, analyze, store, and issue warning and abort triggers. The later provides also the connections to the Beam Interlock, the Beam Energy Tracking, the Logging and the Post Mortem systems. In this paper, the surface

building's electronics are explored providing details for the different parts combined to provide the needed functionality.

This installation foresees VME crates spread over all of the eight LHC interaction points accommodating the processing modules, a timing card, a CPU card and a Combiner card.

The processing module is comprised by the DAB64x and the BLM Mezzanine cards. The BLM mezzanine card handles the de-serialisation and decoding of four optical gigabit data transmission lines in parallel. This mezzanine provides the received data to a reconfigurable FPGA which is the backbone of the DAB64x card. Each module is able to process in real-time up to 16 detector channels.

The timing card is the Timing Trigger and Control (TTC) card developed by the Beam Instrumentation group. In this application it will provide the Time-Stamp and the Post Mortem triggers.

The CPU is a PowerPC with LynxOS as operating system. Its main purpose is to access periodically the processed data from each processing module, normalise them with their corresponding threshold values and provide them to the Logging system before they are displayed on the fixed displays in the control room. Moreover, it will collect and time-stamp the Post Mortem data, stored on the circular buffers, whenever the relevant trigger arrives.

The final receiver of the beam permit lines is the Combiner card, located at the last slot of the crate. The two beam permit lines are daisy chained through each of the processing modules using a custom-made backplane in the crates. If any of the modules decides to break any of these lines a beam dump request will be given to the LHC Beam Interlock System (BIS). As an additional use, those lines will be used by the Combiner card to provide a continuous supervision of the operation of the cards in the crate. Thus, it will be able to discover immediately a disconnection from the circuit or a failure and a dump will be requested for any of those cases.

Finally, the system has been designed with reliability and availability in mind. The processing modules can operate independently of CPU and Timing card failures. There is redundancy in the optical transmission with additional powerful error detection. The beam permit lines in the backplane are also redundant and the connection to the BIS is tripled.

Parallel Session B1-Trigger session 1 / 72

The Drift Tube Track Finder Muon Trigger at the CMS Experiment

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The Compact Muon Solenoid (CMS) is a general purpose experiment designed to study proton-proton collisions at the Large Hadron Collider (LHC). At the LHC, proton beams will cross each other at a rate of 40 MHz, producing in average 20 p-p interactions. The CMS L1 Trigger must select interesting collisions at a rate smaller than 100 kHz. The Drift Tube Track Finder (DTTF) implements the CMS DT L1 Regional Muon Trigger. The DTTF motivation and design, its electronic implementation and the production status will be presented. Tools for configuration, data acquisition, and monitoring will be described. Performance at Beam Tests and at the 2006 Cosmic

Challenge will be discussed. Finally, recent results on expected rates for single muon and dimuon triggers, and prospects for operation at the first year of the LHC will be reviewed.

Summary:

At the Large Hadron Collider (LHC), muons of large transverse momenta are expected to play a crucial role in the physics under study. The Compact Muon Solenoid (CMS) is a general purpose experiment designed to study proton-proton collisions at the LHC. At the LHC, proton beams will cross each other at a rate of 40 MHz, producing in average 20 p-p interactions. The CMS L1 Trigger must select interesting collisions at a rate smaller than 100 kHz. In this report we describe the Drift Tube Track Finder (DTTF) Muon Trigger.

CMS will combine three different technologies for precise muon detection and efficient triggering: drift tube (DT) chambers in the barrel region ($|\eta| < 1.2$), cathode strip chambers (CSC) in the forward region ($0.8 < |\eta| < 2.4$), and resistive plate chambers (RPC) in both regions ($|\eta| < 2.1$). The DT muon chambers are located in the gaps of the barrel iron yoke. The yoke is organized in five wheels along the detector axis. Each wheel is divided in twelve 30^o sectors in azimuth, and four concentric stations in the radial direction: MB1, MB2, MB3, MB4. In every station in a sector, one DT muon chamber contains twelve layers of drift cells organized in two $r-\phi$ superlayers and one $r-z$ superlayer (except the MB4 chambers that do not contain $r-z$ superlayer).

The information delivered by the DT muon chambers is processed by the DT L1 Muon Trigger, which is divided into a DT Local Trigger and a DT Regional Trigger. Hits in the DT muon chambers are first organized in segments and assigned a beam crossing by the DT Local Trigger, and delivered to the DT Regional Trigger.

The DTTF system implements the DT Regional Trigger. The task of the Drift Tube Track Finder Trigger is to reconstruct full muon tracks originating at the interaction point, and to assign them physical parameters.

The DTTF Trigger is physically realized using a sophisticated electronic system. The DTTF logical segmentation replicates the CMS barrel detector geometrical structure. The system is organized in twelve modules stored in six crates. Each module processes the information that originated in a 30^o wedge of the barrel detector. One module is formed by eight boards: six Phi Track Finder (PHTF) sector processors (one PHTF for wheels ± 1 and ± 2, and two PHTF boards for wheel 0), one Eta Track Finder (ETTF), and one Wedge Sorter. Two modules share the same crate and the same VME Controller, Timing, and Data Link boards. A 7th crate contains the Trigger Timing and Control system, the Barrel Sorter, and the interface to the CMS DAQ system.

The Phi Track Finder sector processors (PHTF) reconstruct muon tracks in the $r-\phi$ plane. The PHTF track finding algorithm is implemented in three logical steps: (i) Extrapolation, (ii) Track Assembling, and (iii) Parameter Assignment (transverse momentum, position in ϕ, electric charge, and quality).

In every 30^o wedge, the Eta Track Finder (ETTF) reconstructs the muon trajectory in the $r-z$ plane. The ETTF uses a pattern matching procedure which is implemented in three logical

steps. First, patterns of $r - z$ segments are recognized among a predefined set (η-patterns). Second, η-patterns are matched to PHTF tracks. Finally, if the pattern matching step was successful, the PHTF track is assigned a fine value of η. If no η-pattern could be matched, a rough η value is assigned.

The DT Sorters select the four highest rank DTTF muons in the barrel detector and, after a clean-up procedure, forward them to the Global Muon Trigger.

The DTTF system is realized in Field Programmable Logic Array (FPGA) technology, and is largely programmable. Its optimal exploitation requires the setting-up of logic and lookup tables, that can even be tuned to the physics that is to be explored. All DTTF functional elements were specified using VHDL behavioral code. In addition, real-time software to operate, test and monitor the system has been produced.

The final design of the DTTF boards was decided after an extensive prototyping phase. The PHTF and ETTF final designs concentrate almost all the track-finding functionalities in a big Altera Stratrix FPGA. By March 2006, all electronic boards for the DTTF system had been produced. Quality Control of the produced boards has almost finished.

In October 2004 the behavior of parts of the DTTF were studied under realistic experimental conditions at the CERN Test Beam. The results were excellent. More complex tests of the DTTF system will take place before the LHC era. In 2006 the integrated CMS Trigger will be tested with cosmic muons at the Magnet Test/Cosmic Challenge. Production, installation, and commissioning of the DTTF trigger will happen in 2006 and beginning of 2007, to be ready for the first LHC collisions in April 2007.

Parallel Session B5-Power systems / 73

: Distributed low voltage power supply system for front end electronics of the TRT detector in ATLAS experiment

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We present a low voltage power supply system which has to deliver to the front end electronics of the ATLAS TRT detector ca. 24 kW of electrical power over the distance of 40-50 m (which adds another 24 kW). The system has to operate in magnetic field and under radiation environment of the LHC experimental cavern. The system has ˜ 3000 individual channels which are all monitored and controlled (voltage and current measurement). The hardware solutions are described as well as the system control software.

Summary:

Modern, highly integrated front end electronics of the experimental physics profits from the technological progress in the field of modern electronics. Higher the functional density of custom designed chips, higher the power consumed. The space constraints in design of the collider experiment detectors create severe problems with the power delivery to the front end (to say nothing about evacuation of this

power when converted to heat).
Amount of heavy material –copper –in cables is another negative aspect of the supplying harnesses for electronics (both economical and affecting the detector performance).
The detectors and its electronics will have to withstand also the high radiation level produced by proton-proton collisions at LHC. Peripheral system, those like power supply have to be radiation tolerant as the minimum. The ATLAS configuration of magnets adds another aggressive factor –magnetic field –which has to be tolerated by the power supply systems. This concern all electronics located in the experimental cavern.
ATLAS TRT is a straw detector with > 400000 individual channels. Front end electronics located on the detector surrounding the interaction point consumes power of ˜ 24 kW and another 24 kW is dissipated in cables and regulators.
System consists of three basic parts :
1. Control unit and AC-DC converters located in the control room delivering 380 V DC to 2/. (distance ˜70 m)
2. DC-DC converters located on the supporting structure within experimental cavern serving as bulk power supplies delivering voltages in 2-8 V DC range. (distance ˜ 40 m)
3. Control , monitoring and regulating boards located within the volume of ATLAS setup, supplying individual loads located on the detector (distance ˜ 12 m)
The parts 1 and 2 are commercially available units produced by WIENER. Control unit and AC-DC converter are not resistant to either radiation nor magnetic field thus stay in friendly environment of the control room.
Part 3 consists of custom designed boards where by means of the regulators is realized distribution (or fan-out) function to individual loads. The components used are special design radiation hard regulators and radiation tolerant industrial IC and optocouplers.
The regulators can be disabled/enabled allowing for switch off/on of every channel. The output voltage can be adjusted in range of ˜ 1.5 V to compensate for possible changes in necessary voltage due to radiation aging of front end chips. This is done with help of radiation hard DAC'located in a custom design chips.
The control of the board is performed via ELMB (Embedded Local Monitoring Board) which is interfaced to the industrial SCADA system PVSSII. Some additional piece of software has been designed for performance optimization and ease of digital control of the DAC's.
64 channels ADC on the ELMB board allows for current and voltage measurement of the individual channels. Whole software has been embedded into CERN FrameWork (extension to PVSSII) to allow for use of CERN-specific functions.
Functionalities description and conclusions from running experience will be given.

Parallel Session A7-ASIC developments / 74

Silicon strip readout using Deep-Submicron Technologies

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For the years to come, Silicon strips detectors will be read using the smallest available integrated technologies for room, transparency, and power considerations. CMOS, Bipolar-CMOS and Silicon-Germanium are presently offered in deep-submicron (250 down to 90nm) at affordable cost through worldwide integrated circuits multiproject centers. As an example, a 180nm CMOS readout prototype chip has been designed and tested, and gave satisfactory results in terms of noise and power. Beam tests are under work, and prospectives in 130nm will be presented.

Parallel Session B1-Trigger session 1 / 75

Revised CMS Global Calorimeter Trigger Hardware Design

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An alternative design for the CMS Global Calorimeter Trigger (GCT) is being implemented. The new design adheres to all the CMS specifications regarding interfaces and functional requirements of the trigger systems. The design is modular, compact, and utilizes proven components. Functionality has been partitioned to allow commissioning in stages corresponding to the different capabilities being made operational. The functional breakdown and hardware platform is presented and discussed. A related paper discusses the firmware required to implement the GCT functionality.

Summary:

The Global Calorimeter Trigger (GCT) is the last stage of the calorimeter trigger chain. It's main task is to receive the data from 18 Regional Calorimeter Trigger (RCT) crates, process it, and transmit the results to the Global Trigger (GT), where it is used to compute the first level trigger accept (L1A). Since the FIFO memories that store the event information are quite limited in depth, the processing and transit delay must be kept to a minimum.

The functionality of the GCT can be divided into several tasks, transporting data from the RCT and to the GT, combining RCT data to classify and build event types, and sorting the event objects found according to size and position. While these tasks are not completely independent, they are physically concentrated in four different hardware modules.

The task of transporting the input data from 18 RCT crates is handled by the source card, a 6U VME module. Each source card accepts 2, 80 bit ECL cables and provides outputs on four optical serial links. The parallel input data is accepted at 40MHz, and output at 1.6GHz using industry standard serializers and 8b/10b encoding. In addition to its data transport function, the source card also provides the capability to capture snapshots of RCT data, and generate test patterns for link test and synchronization.

The leaf module is responsible for the bulk of data combining and event object building. Implemented as a double PMC module, it accepts 32 optical links and processes the data in two large Xilinx Virtex 2Pro FPGAs. RCT jet data is processed in six leaf modules, three for each half barrel of CMS. RCT electron data is processed in two additional leaf modules. In the case of jet data, each half barrel is treated as a continuous data space, so the three leaf modules which process the data must communicate directly, sharing data in a ring topology. The processed data is passed to the wheel card via the PMC data lines at 40MHz DDR. In addition to the data processing task, the leaf also provides the capability to capture the raw source card input inject test data for system test.

The wheel card is a 9U VME module, and is used for jet data sorting. It carries three leaf modules, processing jet data for one half barrel of CMS. The wheel card accepts data from the three double PMC sites at 40MHz DDR, and outputs sorted and ranked jet objects to the concentrator via a 40MHz DDR LVDS parallel interface. The processing is implemented by two large Xilinx Virtex 4 FPGAs. The wheel is a logically simple device, required to support the leaf modules and reduce the jet data. In addition to its processing function, the wheel also provides data capture for system test, and an additional PMC site for functional expansion.

The concentrator is the last stage of GCT processing, and is a combination of leaf, wheel and source functionality. It is implemented as a 9U VME board, carries the two electron leaf modules directly, and accepts LVDS data from two wheel cards. The concentrator needs to finish the jet object building from the center of CMS, where the leaf modules cannot share data directly. It then combines this data with the sorted jet objects from each wheel card, performing the final sort before sending the processed data to the GT. The electron data is collected from the two leaf modules, sorted, and passed on to the GT as well. The output data is serialized on 14, 1.6GHz links for transport to the GT. In addition to its data processing functions, the concentrator provides the system VME interface and S-link readout for the entire GCT.

The new design is discussed, although most firmware details are not covered since they are addressed in a separate paper. The design involved various tradeoffs and risk reduction strategies, which are presented in some detail. Upgrade capabilities and presently unused features are also discussed.

Poster sessions / **76**

Signal integrity analysis for the electronic design of printed circuit boards

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LHC detectors and future experiments will produce very large amount of data that will be transferred at multi-Gigabit speeds. At such PCB data rates, signal-integrity effects become important and traditional rules of thumb are no longer enough for the design and layout of the traces.

Simulations for signal-integrity effects at board level provide a way to study and validate several scenarios before arriving at a set of optimized design rules prior to building the actual PCB.

This article describes some of the available tools at CERN. Two case studies will be used to highlight the capabilities of these programs.

Summary:

Increasing clock-speeds and decreasing signal rise- and fall-times means that PCB traces on typical high-speed designs can no longer be considered as perfect point-to-point connections. Typical signal-integrity effects can lead to crosstalk, reflection and power-distribution noise problems that can cause false signal switching. These problems are exacerbated with the introduction of vias or other discontinuities.

It becomes necessary to provide more accurate models of interconnects and associated discontinuities on a typical PCB. Electromagnetic field solvers can be used to provide very accurate representations of interconnections but they are time- and compute-intensive to obtain so can only be used to characterise relatively small regions of the design. Using such a method for a full board simulation is impractical. To overcome this problem, the electro-magnetic tool derived model is typically extracted and used in a conventional circuit simulator to analyse signal-integrity effects more fully.

Two examples will be discussed.

The Alice Silicon Pixel Detector design calls for an optimum low-mass cable which minimizes crosstalk between a pair of 1.6Gbps signals and the adjacent traces. The HFSS electro-magnetic field solver from Ansoft was used to analyse this cable and provide such a design. The extracted corresponding model was subsequently used to simulate in HSpice a full transmission channel incorporating a custom designed LVDS transceiver.

The second case involves the study of the transmission of 1.6Gbps signals through via discontinuities within a 18 layer PCB stack-up. A prototype board had already been designed for the read-out chain of the LHCb experiment using the Cadence SI-tools. These programs can give sufficiently accurate results for reasonably complex designs but in this case, it was thought that the complexity of the via interconnects warranted deeper study. Electromagnetic field solvers were again used for further analysis.

In conclusion, these two case examples show that reliable high-speed PCB digital design needs to take into account all design aspects that will affect signal propagation. These can be examined using commercially available programs to provide an efficient and practical way to study signal integrity effects.

Parallel Session A1-Readout, commissioning and integration 1 / 77

Front-end Electronics Test for the LHCb Muon Wire Chambers

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The document to be presented will describe the electronic scheme and procedures of a system implemented to test the Multi-Wired Proportional Chambers after front-end dressing for the LHCb Muon Detector and its results. Given a dressed chamber, this system is able to diagnose every channel based on front-end output drivers' response and noise rate versus threshold analysis, in addition it evaluates if the noise rate at the experiment threshold region is within appropriate limits. The project has foreseen as well an electronic identification of every chamber and front-end board, and results archiving in a way to make it available to the Experiment Control System (ECS).

Summary:

The LHCb Muon Detector will contain 120 thousands physical channels, corresponding to Front-End (FE) Electronics input, and 26,000 logical channels used for

triggering purposes and off-line muon identification. Each physical channel
consists of an independent Amplifier-Shaper-Discriminator (ASD) circuit. A single
FE board consists of two 8-channel ASD chip called CARIOCA and one mainly digital
chip called DIALOG. In front of each channel connected to the chamber output, there
are spark protection and chamber-to-FEB connection circuits. A method to test
physical channels operation is important to avoid inefficiencies due to failures on
detector read-out region: chambers strip/pad lines, physical connections, FE
circuitry functionality, among others.
LHCb Muon System has foreseen 20 geometrically different MWPCs. Depending on its
type, chamber capacitance can vary from roughly 40pF to 250pF and signal can be
read from anode and/or cathode connections. Due to the later requirement, CARIOCA
has been developed to process both polarities by implementing 2 different pre-
amplifiers at the very ASD input stage. They show slightly different signal
responses depending on the chosen polarity operation. The on-detector circuitry is
composed of three building blocks: OR-PAD, Spark-Protection (SPB) and CARDIAC
(CARIOCA and DIALOG Circuitry). The first two boards make use of passive components
while the third board processes and digitalizes chamber signals. Those are some
considerations covered by the method used to evaluate such chambers.
The test apparatus presented in this document has been developed to evaluate the
front-end and chamber conditions before assembling it to the detector. Diagnostics
are given based on FE output lines response, noise rate versus threshold analysis
and evaluation of noise rate given reasonable threshold values. To test output
lines functionality, FE auto-injection fixture is used to generate signals on the
circuit input; control of their responses is done by means of external counters.
With noise rate versus threshold analysis, considering a Gaussian noise presence in
a discriminator input and a Gaussian time response distribution, it is possible to
obtain information about three fundamentals characteristics: the circuit bandwidth,
offset and its equivalent noise. Once such characteristics are known, it is
possible to estimate other parameters as: chamber capacitance, FE equivalent noise
charge and sensitivity. Finally, operational threshold efficiency can be evaluated
by considering the relationship between threshold, in charge (fC), and noise rate.
It will be presented results obtained during chamber tests.
To carry out such test and diagnostic procedures it has been used two VME modules,
one used as external counters and another as interface VME-

USB, together with the
official LHCb Muon FE control electronics and a CANopen-USB
board plus a C++ and
Root integrated software, resulting in a fixture able to
perform FE control, data
acquisition and analysis. Additionally a barcode scheme has
been implemented
permitting identification of chambers and FE boards.

Parallel Session B4-Trigger & DAQ session 1 / 78

The ALICE Silicon Pixel Detector Control system and online calibration tools

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The ALICE Silicon Pixel Detector (SPD) contains nearly 10ˆ7 hybrid pixel cells. About 2000 parameters and ˜50000 DACs must be controlled in real-time during the detector integration, commissioning and operation. Information on each channel is stored in a configuration database. Timing and data management are critical issues. An overview of the SPD detector control system is presented, focusing on front-end controls and the SPD calibration strategy. An outlook of future implementations is presented.

Summary:

–Introduction–
The ALICE Silicon Pixel Detector (SPD) contains nearly 10ˆ7 hybrid pixel cells. About 2000 parameters must be controlled in real-time during experimental data taking and in detector calibration runs. Configuration and calibration for each channel (˜50000 DACs in total) must be applied during the detector integration and commissioning as well as at different phases operation. Information on each channel is stored in a configuration database. Timing and data management (˜6 GB of raw data each calibration) are critical issues.

–ALICE SPD layout–
The SPD constitutes the two innermost layers of the ALICE Inner Tracking System (ITS). The SPD consists of 120 half-staves (HS), each one consisting of two ladders (5 readout chips bump bonded to a

sensor for each ladder) and one Multi Chip Module (MCM). The MCM distributes the timing signals, provides the required analog references and controls the readout.
The communication between the MCM and the counting room is via optical links. In the counting room 60 Link Receiver cards (LRx) perform zero suppression and data encoding of the data streams. Three LRxs are plugged on 20 VME based router module with optical links to the experiment DAQ and trigger system.
The LV power is supplied by 20 CAEN A3009 modules (12 LV channel each) and the sensor bias is provided by CAEN A1519 modules 10 (12 HV channel each).
The FE electronics power dissipation is ˜1.3kW.
The cooling is based on an evaporative system with C4F10. The operational temperature of the detector is ˜25 ℃.

–SPD Calibration procedure–
The detector calibration is based on electrical pulses generated on the FE chips. The detector efficiency as well as the uniformity of response of the pixels matrices are studied by varying the pulse amplitude at various threshold settings (S-curves).
Automated configuration calibration procedures are implemented in the Detector Control System (DCS) that is able to emulate the ALICE DAQ and trigger system.
The raw data produced by the detector are analyzed online by the DCS that provides a configuration parameter set that will be used by the detector during the physics data taking.

–The SPD Control system–
The system is based on Supervisory Control And Data Acquisition (SCADA), PVSS. The system controls two Front End Device (FED) Servers (C++ based) that communicate with the hardware and carry out the calibration and control procedures. PVSS agents control the status and apply intervention as required by communicating both with the Experiment Control System (ECS) and the FEDs. The detector data are sent to a ROOT based analysis tool that produces online information on the pixels response and define the configuration for the whole system. The analysis tool is controlled via PVSS. The system structure allows fast remote operator intervention and is highly modular. The communication between the different software platform applications is via Distributed Information Management System (DIM - TCP/IP).
Most processes are fully automated in order to obtain the required reliability and safety of operation.
The power system (HV and LV) and the cooling systems are controlled directly by PVSS.
The logical control of the full system is carried out through a Finite State Machine (FSM, SMI++ based) that defines the sequences of commands to the different sub-systems. The FSM represents also the operator interface to the detector and allows the interconnection with the general ALICE DCS.

–SPD DCS status–
The prototype of the system is close to completion and has already been used to test two SPD sectors during integration and commissioning. The final electronic readout chain, the cooling and power systems are operational. The integration with the ALICE DCS and DAQ is in progress and will be soon completed. An overview of the system status and performance, focusing on front-end controls and analysis tools, is presented. The solutions for data management and storage are discussed. An outlook of future work is shown.

Poster sessions / 79

Implementation of the Control System for the LHCb Muon Detector

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The Muon Detector of LHCb will be equipped with about 1380 Multi-Wire Proportional Chambers. Within the Framework of the CERN Control System Project, using PVSS as the main tool, we are developing an instrument to manage such a system. Adjustment and monitoring of High and Low Voltage power supplies, on-line diagnostics and fine tuning of the Front-End read-out devices, data acquisition from the gas system and the monitoring of pressure and temperature of the experimental hall are being implemented. The system will also look after long term data archiving and alert handling. The Control System performance is currently under evaluation in a cosmic ray station. Built as a final quality control of the LHCb Multi-Wire Proportional Chambers, allowing acquisition of data from as many as 600 Front-End readout channels, the cosmic ray station is fully managed by means of a Control System prototype.

Summary:

In order to manage and monitor the LHCb Muon Detector, a Control System is now being developed and tested. A Finite State Machine architecture has been adopted, following the CERN Joint Controls Project (JCOP) recommendation: "The experiment control systems are modelized as a hierarchy of Finite State Machines (FSM). In this model there is a state/command interface between a parent and its children. Commands are passed from a parent to its children and the states/alarms of the children are passed to the parent who derives its state from those of its children.". Each item (Device Unit) is thought of as having a set of stable states. Items can move between their allowed states by making transitions triggered either by commands or state changes of a dependent FSM. After a change of state the Device Unit generates a signal to inform the Control Unit about its state. The main Control Unit is called Muon System. It sends commands and

receives States and
Alarms to and from a set of children Control Units (called High Voltage, Low
Voltage, Environment Sensors, Electronics and Gas System) which interact with the
hardware Device Units.
A first down scaled implementation of the Control System is now being used and
tested to fully manage a cosmic ray station built for the studies of the LHCb MWPC.
The cosmic ray stand is able to house 6 MWP chambers and allows the acquisition of
as much as 600 Front-End channels. PVSS programs are now being used to manage high
voltage power supplies, front-end readout devices and to monitor the environmental
parameters. This system is giving a unique possibility to study in details the
different features of the Control System and is an useful tool to test its
robustness. In this document it will be described the software tools together some
example of the studies performed with the cosmic ray stand. Usage of the tools
developed to manage a Cosmic Ray Station, already in use for tests and performance
valuation of the LHCb Muon Chambers, makes possible to have a fast feedback on the
usefulness of the implemented features and to test for robustness of the Control
System itself. Routines for calibration and diagnostics of the front-end
electronics and for high voltage setting and monitoring have already shown to work
very well and result of great importance for the automation of the Muon Detector
Control System.

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Revised CMS Global Calorimeter Trigger Functionality & Algorithms

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A revised design of Global Calorimeter Trigger (GCT) has been implemented. The
primary function of the GCT is to process the Regional Calorimeter Trigger (RCT)
data and transmit a summary to the Global Trigger (GT) which computes the First
Level Trigger Accept (L1A) decision. The GCT must also transmit a copy of the RCT
and GCT data to the CMS DAQ. This paper presents an overview of the revised design,
concentrating on the firmware structure and algorithms.

A separate paper presented
in this conference details the hardware design.

Summary:

The Global Calorimeter Trigger (GCT) is the last stage of the calorimeter trigger
chain. The primary purpose of the GCT is to reduce the number of calorimeter
trigger objects that need to be considered by the Global Trigger (GT) for a First
Level Trigger Accept (L1A) decision. The pipeline memories that store event
information prior to a L1A request have only limited depth and thus data
transmission and processing time must be kept to a short, critical time period.

The trigger objects sent to the GT are listed below. The "rank" of an electron or
jet is at present its transverse energy, however in principle it could also be
derived from jet location and energy. The jet transverse energy is the sum of both
the hadronic and electromagnetic calorimeter.

- 4 isolated and 4 non-isolated electrons of highest rank
- 4 central, 4 forward and 4 tau clustered jets of highest rank
- total transverse energy: sum of all jet transverse energy (magnitude)
- missing transverse energy (magnitude and angle)
- jet transverse energy: sum of found clustered jets (magnitude)
- 12 jet counters based on rank and position criteria

These trigger objects are calculated/extracted by the GCT from information supplied
by the Regional Calorimeter Trigger (RCT). The original task of the GCT was to sort
electron and jet trigger objects received from the RCT using rank. Jets are
subdivided into and for central, forward and tau jets based on a tau veto bit and
eta. The task of the GCT has now been extended to perform jet cluster finding and
subsequent conversion of jet energy to rank to create trigger objects before
performing the sort.

The electron sort operation must determine the 4 highest rank objects from 72
candidates for both isolated and non-isolated electrons from a significant data
volume (29Gb/s per electron type).
The jet cluster finding and subsequent sort is more challenging because of the
larger data volume (172.8 Gb/s) and the need to share data between processing
regions to perform cluster finding. The latter can require data flows of a similar
magnitude to the incoming data volume depending on the

cluster algorithm used. The
baseline algorithm of a 3x3 sliding window requires
substantial data sharing, making
the system more complex. An alternative algorithm is
presented and compared to the
original.

In addition to these tasks the GCT: (a) acts as a readout
device for both itself and
the RCT by storing information until receipt of a L1A and
then sending the
information the DAQ via a SLINK64 interface (b) extracts
trigger information for the
muon system from the calorimeter data stream (c) monitors
the LHC luminosity.

The revised design is discussed, although the hardware
details are kept to a minimum
as they are presented in a separate talk at this conference.
The data processing
firmware, in particular the algorithms, data flow and
associated latency within the
revised GCT are presented.

Poster sessions / **81**

System tests and debugging using Python

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The CMS Global Calorimeter Trigger (GCT) control and
test software is described. An
object-oriented model of the GCT hardware, based on
the CMS Hardware Access Library
(HAL), was written in C++. The SWIG software interface
generator was then used to
produce a python interface to the model. This allows
the hardware to be controlled
from a python script or shell, providing a flexible
environment for rapid development
of hardware and firmware tests without requiring
detailed knowledge of software.

Summary:

The CMS Global Calorimeter Trigger control and test
software is based on an object
model of the hardware and firmware, that is itself based on
the CMS Hardware Access
Library (HAL). Classes are included to represent boards,
devices, busses, links and
firmware blocks. Each class contains methods to build and
navigate the model, and
methods to initiate operations on the hardware or firmware

component represented by
the class. A single GlobalCaloTrigger object provides a point of entry for the user
that automatically initiates building of the model, hidden from the user. The
navigation methods follow the physical structure of the hardware, and the logical
structure of the firmware. For example, one may obtain (pointers to) the module
objects from the crate object, or the firmware blocks within an FPGA from the object
representing the FPGA. The operation methods include low-level register read/write
commands that are generally common to all objects, and higher-level methods that are
generally specific to the component being represented, eg. the Link object has a
method that initiates a self-test.

A SWIG header is written for each class, including the navigation and operation
methods, but not the build methods, as they are only required internally. The
resulting python library allows the user to navigate and control the hardware from a
python script, or interactively from the python shell. The user then requires very
little software knowledge to write scripts to perform complex operations and tests,
or to access and debug the hardware interactively. Python scripts are also envisaged
to be the main mode of initialising the system for all modes of operation, include
running tests and taking data.

The control software is integrated with CMS run control by including the object model
in a XDAQ application. This allows a SOAP interface to the object model to be
defined, which generally uses the highest-level methods on the GlobalCaloTrigger
object. The XDAQ application also includes an embedded python interpreter, allowing
the use of python scripts within the run control framework.

Parallel Session B5-Power systems / 82

Electromagnetic Compatibility of a Low Voltage Power Supply for the ATLAS Tile Calorimeter Front-End Electronics

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The front end electronics of the ATLAS Tile Calorimeter is powered by DC/DC conveters that sit close it. The performance of the detector electronics is constrained by the conducted noise emissions of its power supply. A compatibility limit is defined for the system. The noise susceptibility of the front end electronics is evaluated, and different solutions to reduce the front end electronics noise are discussed and tested.

Summary:

I. POWER DISTRIBUTION SCHEME FOR THE TILE CALORIMETER

The amount of power required by the front-end electronics of the Tile Calorimeter of the ATLAS experiment imposes the presence of switched power supplies made of custom radiation tolerant DC/DC converters. The power supplies are located inside the detector near the front-end electronics.
The noise of the DC/DC converters deteriorates the performance of the detector: it must be filtered out.

II. EVALUATION OF NOISE PERFORMANCE

The high frequency noise seen by the fast readout electronics is estimated from the pedestals data acquired with the complete data acquisition chain. The noise of the system is estimated by a selection of parameters computed over several runs and on all the channels:
• RMS of the pedestals distribution.
• Gaussian property of the pedestals distribution.
The low frequency noise is evaluated from data sampled by the current integrators ADC.
On the other hand, the noise performance of the power supply is measured on each low voltage output as common mode current amplitude and as voltage ripple for the differential mode component.

III. NOISE PROPERTIES OF THE CONVERTERS

The DC/DC converters emit large common mode currents at the switching frequency and its harmonics, exceeding the limits in use. Beyond the switching frequency, the CM current amplitude is below the usual limits.
The common mode current path is modelled and the amplitude is measured. From this, appropriate filters can be applied.

IV. FRONT-END SUSCEPTIBILITY

The measurements made show that the fast readout electronics is sensitive to high frequency common mode currents (5MHz to 100 MHz). The DC/DC converters noise was already below the usual limits, but further filtering is required due to the high susceptibility of this part of the electronics.
Similar measurements on the slow readout electronics show that this part of the electronics is very sensitive to low frequency ripple (below few kHz). The operating point of the converters must be tuned to minimize the ripple.

V. FILTERING METHODS

Several methods allow reducing and filtering the common mode currents. Among those, the following devices were tested: common mode chokes on the primary and secondary side of the converters, ferrites on the low voltage outputs, decoupling capacitors between each input and output pins to the case. The chokes show the best performance, especially when placed on each output; however, they are too bulky to fit in the tight space of the low voltage box. As an alternative, ferrites and decoupling capacitors were successfully tested.
The low frequency ripple is minimized by setting the DC/DC converter operating

point around mid-capacity. This adjusted at the feedback components of the converters.

VI. CONCLUSION

The noise properties of the DC/DC converters were compared with the susceptibility of the fast and slow readout electronics. From this a noise coupling model was established, and different filtering solutions were exercised. Among those, the use of ferrites and common mode decoupling capacitors appeared to be most suitable method that allows operating the front end electronics within the detector noise specifications.

Poster sessions / 83

CMS Optical Links - Lessons learned from Mass Production

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The CMS Tracker will install over 40000 optical links in its data readout and control system, representing an unprecedented deployment of this technology in a Particle Physics Experiment. After reviewing the Quality process employed in this project, a summary of the performance data measured during production will be shown. The analysis of this data will then be used to illustrate how the performance of the installed system may be predicted, giving confidence that the specified functionality will be attained in the final system. Completion of the production has allowed reflection upon the processes used and improvements for future such projects will be given in the form of some lessons learned.

Summary:

Production of components for the 40000 optical links of the data readout and control system of the CMS Tracker is now complete. The Quality Assurance process put in place for the production yielded detailed performance data for each individual component produced. The QA process put in place before component-production started will be outlined. For such an unprecedented (in the field of Particle Physics) scale of production all components were produced by industrial partners. This was made possible through the choice of COTS-based components with only minimal modification to meet the criteria set by the CMS Tracker environment. Production proceeded in batches, with the manufacturers providing per-device measurements of the key performance parameters with delivery of the batch. Batch-level acceptance was then carried out at CERN to verify these measurements.
The large number of components produced has yielded a unique data set of component performance that can be used to make statistical predictions on the overall performance of the links that will be installed in CMS. Analysis of this data will be presented, showing on the one hand the progression of production from start to finish and highlighting the issues that occurred along the way; and on the other hand giving data that can be used to predict the performance margins of the installed links. For the analogue readout system of the CMS Tracker the gain of the individual links is of utmost importance, since it directly affects the overall dynamic range of the full readout chain. It will be shown that the final performance dataset confirms the prediction that all links will enable data to be transmitted with sufficient margin. For the digital control system that is based upon the same components as the analogue readout system these data allow the confirmation of the operating margins.

We will also reflect upon the progression of the production and the problems encountered along the way. The most critical phase of the process for all components was the start-up phase during which the manufacturing process was qualified by CERN. It was in this phase that the largest number of issues had to be resolved so that the production could then proceed smoothly to the end. We will conclude by providing some lessons learned for future projects of this scale.

Parallel Session B3-Trigger session 3 / **84**

The ATLAS Barrel Level-1 Muon Trigger Calibration

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The ATLAS experiment uses a system of three concentric Resistive Plate Chambers detectors layers for the level-1 muon trigger in the air-core barrel toroid region. The trigger classifies muons within different programmable transverse momentum ranges, and tags the identified tracks with the corresponding bunch crossing number. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The on-detector electronics providing the trigger and detector readout functionalities collects input signals coming from the RPC front-end. Because of the different time-of-flights and cables and optical fibers lengths, signals have to be adjusted in time in order to be correctly aligned before being processed. Programmable delay logics are provided in the trigger and readout system to allow for time adjustment, for hit signals as well as for LHC Timing, Trigger and Control signals.
The trigger calibration provides the set of numbers used during electronics initialization for correctly aligning signals inside the trigger and readout system. The functionality scheme and the algorithm of the calibration are presented.

Summary:

The ATLAS barrel level-1 muon trigger system has to identify muon candidates crossing the spectrometer and associate them to a specific bunch crossing, to a detector region of $\Delta\eta X\Delta\Phi=0.1X0.1$ granularity and classify them by their Pt thresholds.
The ATLAS barrel level-1 muon trigger system has the following main requirements: coarse measurement and discrimination of the muon transverse momentum pT; bunch crossing identification; fast and coarse tracking to identify tracks in the precision chambers that are related to the muon candidate; 2nd-coordinate measurement with a required resolution of 5–10 mm.
The muon trigger system in the barrel is based on full granularity information coming from three station of a dedicated trigger detector, Resistive Plate Chamber, covering a region of $-1<\eta<1$. Two stations are located near the centre of the magnetic field region, inside the air-core toroids, and provide the low-pT trigger (pT > 6 GeV), while the addition of the third station, at the outer radius of the magnet, allows to increase the pT threshold to more than 20 GeV, thus providing the high-pT trigger.
A trigger station is made of two detector layers, each one is composed by two RPC detectors, read out by two orthogonal series of pick-up strips of about 3 cm pitch: the η strips parallel to the MDT wires (z direction) provide the "bending"coordinate of the trigger detector; the φ strips, orthogonal to the wires, provide the second "non-bending"coordinate.
To reduce the rate of accidental triggers, due to low-energy background particles in the ATLAS cavern, the algorithm is performed in both the η and φ projections for both low-pT and high-pT triggers. The first stage of the trigger algorithm is performed separately and independently for the two projections. A valid trigger is generated only if the trigger conditions are satisfied for both projections. The trigger logic

requires three out of four layers in the middle stations for the low pT trigger and, in addition, one of the two outer layers for the high-pT trigger. The η and φ trigger information is combined to generate the Regions-of-Interest (RoI), identifying areas in the apparatus in which track candidates are found with a granularity of ˜0.1×0.1 in the η-φ pivot plane.
The signals from the RPC detector are amplified, discriminated and digitally shaped on-detector. In the low-pT trigger, for each of the η and the φ projections, about 200 RPC signals of the two detector doublets, RPC1 and RPC2, are sent to a Coincidence Matrix (CM) board, that contains a CM chip. This chip performs almost all of the functions needed for the trigger algorithm and also for the read-out of the strips. It aligns the timing of the input signals, performs the coincidence and majority operations, and makes the pT cut on three different thresholds. It also contains the level-1 latency pipeline memory and de-randomising buffer. The CM board produces an output pattern containing the low-pT trigger results for each pair of RPC doublets in the η or φ projection. The information of two adjacent CM boards in the η projection, and the corresponding information of the two CM boards in the φ projection, are combined together in the low-pT Pad Logic (Pad) board. The four low-pT CM boards and the corresponding Pad board are mounted on top of the RPC2 detector. The low-pT Pad board generates the low-pT trigger result and the associated RoI information. This information is transferred, synchronously at 40 MHz, to the corresponding high-pT Pad board, that collects the overall result for low-pT and high-pT. In the high-pT trigger, for each of the η and φ projections, the RPC signals from the RPC3 doublet, and the corresponding pattern result of the low-pT trigger, are sent to a CM board, very similar to the one used in the low-pT trigger. This board contains the same coincidence-matrix chip as in the low-pT board, programmed for the high-pT algorithm. The high-pT CM board produces an output pattern containing the high-pT trigger results for a given RPC doublet in the η or φ projection. The information of two adjacent CM boards in the η projection and the corresponding information of the two CM boards in the φ projection are combined in the high-pT Pad Logic board. The four high-pT CM boards and the corresponding Pad board are mounted on top of the RPC3 detector. The high-pT Pad board combines the low-pT and high-pT trigger results. The information is sent, synchronously at 40 MHz, via optical links, to a receiver and Sector Logic (SL) board, located in the USA15 counting room. Each SL board receives inputs from up to height Pad boards, combining and encoding the trigger results of one of the 64 sectors into which the barrel trigger system is subdivided. The trigger data elaborated by the Sector Logic is sent, again synchronously at 40 MHz„ to the Muon Interface to the Central Trigger Processor (MUCTPI), located in the same counting room. Data are read out from high-pT Pad boards only. These data include the RPC strip pattern and some additional information used in the LVL2 trigger. The read-out data for events accepted by the LVL1 trigger are sent asynchronously to Read-Out Drivers (RODs) located in the USA15 underground counting room and from here to the Read-Out Buffers (ROBs). The physical link between on-detector and off-detector electronics is shared between trigger and readout data. In particular the read-out data are sent when trigger results are not available for the detector region of interest.

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Setup for testing LHCb Inner Tracker ladders

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The Inner Tracker of the LHCb experiment is a silicon microstrip detector consisting of 336 detector modules with either one or two sensors. The module production is now underway and we present here the setup employed for module testing during the production. The setup is based in the same electronics that will e used in the final experiment. We perform burning and ageing tests with the help of a custom made Temperature Cycling Box controlled with LabVIEW under Windows. The DAQ is done in another pc running Linux. Here we integrate the different C/C++ libraries used to communicate to the LHCb Time and Fast Control system, Esperiment Control System, and Data Acquisition.

Poster sessions / **86**

Functional and linearity tester system for the LHC beam loss monitoring data acquisition card

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In the frame of the design and development of the beam loss monitoring (BLM) system for the Large Hadron Collider (LHC) a flexible tester has been developed to qualify and verify during design and production a data acquisition card. It permits to test completely the functionalities of the board as well as realizing analog input signal generation to the acquisition card. The system utilize two optical receivers, a Field Programmable Gate Array (FPGA), eights flexible current sources and a Universal Serial Bus (USB) to link it to a PC where a software written in LabWindows (National Instruments) runs. It includes an important part of the measurement processing developed for the BLM in the future LHC accelerator.

Summary:

The beam loss monitoring system for the LHC uses a radiation tolerant acquisition card (BLECF) to measure the current of ionization chambers. The data are transmitted to the surface to a VME board (DAB) using optical links. The data are processed in it and decisions are taken in case of dangerous losses. In order to visualize and test the BLECF in an efficient way, a single board with dedicated software has been developed with flexible and powerful features.

The board is able to check the linearity of the measurement from the BLM acquisition card. A complex current source has been developed to be able to feed the inputs with current from 10pA to 1mA (8 orders) with a reasonable accuracy (better than the input tolerance). To check if the results are in the expected tolerances a sequence of current settings is launched with the software to scan the whole dynamic range. When the system works in the similar mode to the future LHC system (Running Sums acquisition), it is possible to check different indicators like the number of wrong Cyclic Redundancy Check (CRC) of the optical link or the type of error appearing in the receptions of the packet. In order to check specific data during the development of the BLECF, visual displays have been implemented in the software for the values of the current-to-frequency converter and the sampled value of the Analog to Digital Converter (ADC) entering in the calculation of the final current.

The use of a USB module has been launch by a student in his thesis. The choice of the modules have been determined by their speed which they reached (use of USB 2.0) and by the availability of a complete library of functions. The optical receivers use photodiode with automatic gain control and are interfaced with an 8b/10b transceiver. The FPGA holds the reception logic for the data, the processing of them

(taken from the future LHC BLM system) and the logic for the link to the PC (including control and acquisition). The software is able to integrally control the board in its different mode of operation including a reading of the raw data, a high speed reading, visualization of the resulting processing of the FPGA calculation (running sums) and the functional and linearity tests. The program has been written in C and linked with a user friendly interface. The board can be powered over the USB of a laptop.

The system has been successfully used during the development phase at CERN and especially used by the designer of the BLECF during the validation of the FPGA description. Since the processing of the data is similar to the final system and very compact, the board has been successfully used as readout system during radiation tolerance campaigns for the BLECF at PSI. For the same reason, the system will also be used during installation and commissioning of the LHC BLM. Another use of this system will be the investigations for the beam condition monitor of the LHC CMS experiment using diamond detectors.

Parallel Session A2-Readout, commissioning and integration 2 / 87

FEC-CCS: A common Front-End Controller card for the CMS detector electronics.

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The FEC-CCS is a custom made 9U VME64x card for the Off-Detector electronics of the CMS detectors. Special effort has been invested in the design of the card in order to make it compatible with the operational requirements of multiple CMS sub-detectors namely the Tracker, the ECAL Crystals and ECAL Preshower, the PIXELs, the RPCs and the TOTEM. This paper describes the design architecture of the FEC-CCS card focusing on the special design features that enables the common usage by the CMS subsystems. Results from the integration period in the sub-systems and performance measurements will also be reported. The design of a custom made testbench for the production testing of the 150 cards produced will be presented and the attained yield will be reported.

Summary:

The CMS Tracker control system, initially developed for the needs of the CMS Tracker sub-detector, has now been adopted by the majority of the CMS sub-detectors as a common control system for their front-end electronics. The CMS sub-detectors using this “common”control system are the ECAL Crystals and ECAL Preshower, the PIXELs, the RPCs and the TOTEM. This fact made apparent the need of a having common Front-End Controller card for the off-detector electronics part for those sub-detectors thus minimizing the effort and the associated cost for the development of the card and facilitate the maintenance during the operation period of the CMS experiment.
The FEC-CCS card is a 9U VME64x compliant card following design rules for custom VME hardware in CMS. The main functions of the FEC-CCS card are to distribute both the fast timing signals (40MHz clock and Trigger Commands) and the slow control data through the optical control links to the front-end electronics ASICs. The FEC-CCS card functions as a VME carrier for the mezzanine Front End Controller modules

(mFECs) that host the functionality of the master node controller for the front-end control links. The FEC-CCS can be populated with up to 8 mFEC modules.
The VME FEC-CCS card features a Local Bus that interconnects the mFECS. An FPGA circuit implements the interface logic between the VME bus and the on-board Local Bus. Slow control information passes though the VME bus and the Local Bus. Instead the fast timing signals are distributed to the mFECs though a different FPGA circuit that implements the sub-detector specific Trigger Command handling. To enable the seamless utilization of the FEC-CCS modules across the different CMS subsystems a high level of programmability has been introduced in the firmware design so that not only an identical module but also a unique firmware version could be deployed to all the modules for all the sub-systems thus minimizing the effort for system maintenance and support for the years to come. For the ECAL Crystals, Preshower and TOTEM subsystems the FEC-CCS card delivers some extended functionalities like the fanout of the TTC signal and the merging of the TTS (Trigger Throttling Signals) signals via a private special backplane connector.
Nearly 40 prototype FEC-CCS cards have been produced up until now and delivered to all the involved CMS sub-systems to participate in various detector testbenches and test beam data taking systems. Test results from selected test setups will be reported along with some preliminary performance measurements. The power dissipation of a fully loaded card has been measured and found to be 30 W.
The current status of the FEC-CCS production is at the phase of the production testing. A custom made hardware and software has been developed for this purpose at CERN. The paper will conclude by briefly discussing the production test bench and the production yield attained.

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n-XYTER - A CMOS read-out ASIC for a new generation of high rate multichannel counting mode neutron detectors

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For a new generation of 2-D neutron detectors developed in the framework of the EU NMI3 project DETNI [8], the 128-channel frontend chip n-XYTER has been developed. To facilitate the reconstruction of single neutron incidence points, the chip has to provide a spatial coordinate (represented by the channel number), as well as time stamp and amplitude information to match the data of x- and y-coordinates. While the random nature of the input signals call for self-triggered operation of the chip, on-chip derandomisation and sparsification is required to exploit the enormous rate capability of these detectors (up to 10ˆ5/s/channel). The chosen architecture implements a preamplifier driving two shapers with different time constants per channel. The faster shaper drives a single-pulse discriminator with subsequent time-walk compensation. The output of this circuit is used to latch a 14-bit time stamp with a 2ns resolution and to enable a peak detector circuit fed by the slower

shaper branch. The analogue output of the peak detector as well as the time stamp are fed to a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. The chip will be submitted for manufacturing in AMS's C35B4M3 0.35um CMOS technology in June 2006.

Summary:

In the framework of the EU NMI3 project DETNI [8] a new generation of detectors for imaging and time-of-flight applications with neutrons is under development. The project targets the realisation of three different high rate, solid neutron converter based detectors, one of which is a double-sided Silicon micro-strip detector, coupled to a Gadolinium neutron-converter layer (Si-MSD). The other two detector types are gas based: The "Cascade" GEM detector using a Boron converter and a Hybrid-MSGC detector with Gd-converter. Either one of the detectors is characterised by a comparatively high number of readout channels per coordinate (up to 640 x 640 for the Si-MSD) and a specified event-rate, unprecedented in single event counting neutron or X-ray detection technology.
To accomplish the readout of these detectors the 128-channel n-XYTER readout ASIC has been developed. It will allow determining both, time of incidence as well as pulse height of the detected signals. The former will allow localising the point of conversion of neutrons through coincidence on both coordinates, the latter serves to further enhance spatial resolution through centre of gravity calculation on one hand and to realise X-ray background discrimination on the other hand. Particular attention is paid to address the statistical nature of the incoming signals in the purely data driven acquisition architecture.
Either one of the DETNI detectors is inherently capable of enormous neutron conversion rates. The targeted rate capability for these detectors will entirely be limited by the bandwidth of readout electronics and time resolution, which determines coincidence resolution for position correlation. With an expected neutron conversion rate of 100MHz on the detector, each signal needs to be tagged with a 2ns resolution. Further, as neutron data is statistical in nature, and readout bandwidth limited, a derandomization scheme together with a sparsification concept needs to be employed. To achieve these goals, the chosen architecture implements a charge-sensitive preamplifier for ultra low-noise and wide dynamic range. It drives two shaper stages with different time constants per channel. The time constant of the faster shaper was chosen just long enough to completely integrate the signal of a silicon sensor. It drives a single-pulse discriminator with subsequent time-walk compensation. The latter is required to restrict the amplitude-dependent time walk of the discriminator to less than 2ns. The output of this circuit is used to latch a 14-bit time stamp from a 500MHz grey code counter and to enable an auto-resetting peak detector circuit fed by the slower shaper branch. The noise of the discriminator readout path is expected to be only ˜1000e with a 30pF detector, which together with threshold correction on a per-channel basis will ensure a sufficient S/N ratio without compromising efficiency. The analogue output of the peak detector as well as the time stamp are fed to a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. Due to the unique properties of this architecture, implementations with a lower number of channels, targeted for applications with even higher rates, are also planned.
We present the scientific output of an evaluative prototype together with the design and implementation of the first full scale version. realised in silicon on the AMS 0.35um C35B4M3 process.

[8] (http://jra1.neutron-eu.net/jra1)

Parallel Session A2-Readout, commissioning and integration 2 / 89

Integration and Installation of the CMS Electronics system

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The electronics systems used to control, trigger, and acquire data from the four experiments at LHC are, for the field of High Energy Physics, of unprecedented level of complexity and sophistication.
In the case of CMS, users are gaining access to the counting room (USC55) at a late stage with respect to the official LHC start-up date.
Measures taken to reduce the time required between when the access is granted for installation and the experiment is ready for physics are presented along with the current status and plans.

Summary:

When it became obvious that the CMS cavern was going to be delivered to the collaboration at a very late stage, measures were taken to cope with the situation. An Electronics Integration Centre (EIC, in building 904, CERN), used by all electronics subsystems across CMS, was created in order to allow system integration to take place during the year before any electronics could be installed in the underground counting room. The electronics integration centre is currently being intensively used by practically all subsystems, including the Detector Security System (DSS). The DSS is responsible for the control and security in the racks where the electronics modules under test are located. The goal is to use, as far as practical, the same technology in the EIC as will be used in the underground control room.
As an additional test, most subsystems contribute to an integration test attached in time to the CMS magnet test with the goal to detect, trigger, and read out events originating from cosmic particles. The event goes under the name Magnet Test Cosmic Challenge (MTCC).
Fractions of the sub-detectors are mounted in the final positions inside and outside the large solenoid, contributing with the S in CMS. A complete slice of the electronics for the control, trigger, and readout systems is deployed, providing a last chance for verification before the experiment is lowered and the electronics system is finally installed for commissioning in the underground control room.
After a successful integration in the EIC, every subsystem has to go through an installation readiness review where every system having a direct interface has to agree that no visible problem exist. This review is estimated to be a useful preparation for installation, leaving only the new interconnects to verify during and after installation.

The plan for the electronics installation in USC55 has initially been developed together with TS-LEA, the CERN group responsible for the overall coordination at Point 5 in Cessy. The overall plan is vast and very complete, integrating the day to day work of external subcontractors performing a large variety of tasks, including installation of infrastructure and civil engineering.
As the site becomes ready, the actual electronics installation schedule becomes a detached planning.
The result is a day to day program detailed down to the hour. The installation of each subsystem has to follow the program with great precision, meaning finish on time. Failing to do so, the user might see the access to the underground refused the next morning due to some scheduled event.

After completion of the electronics system commissioning, the EIC facility will continue to serve as a centre for hardware, firmware, and software development. This development may be either for upgrades, or to achieve the design performance of the

experiment.
The development task is likely to become major, since no guarantees can be given that the initial developers, who have the detailed knowledge about how and why the system actually works, are available even one year after the first physics run.

Parallel Session A3-Readout, commissioning and integration 3 / 90

Long Term Testing of VeLo detector modules in Vacuum

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LHCb is the only dedicated B physics experiment on the Large Hadron Collider (LHC) ring. It is an spectrometer whose vertex detector(VeLo) has been optimise for the reconstruction of vertices near the beam. This is achieved by placing the silicon strip detector modules inside the primary beam pipe. Hence they are expected to operate in vacuum (10^{-6}mbar) and withstand high levels of radiation. Long term testing under vacuum was performed on these modules as part of their quality assurance during the VeLo production. These included thermal cycling and monitoring its electronic performance. Results will be presented of the modules tested so far and the unique challenges of vacuum operation.

Summary:

LHCb is the only experiment within the Large Hadron Collider (LHC) whose geometry has been optimised for the study of B physics. One of its aims is to study CP violation phenomena and thus probe for physics beyond the standard model. LHCb is an spectrometer whose design includes a vertex detector called the VeLo. It allows the reconstruction of displaced vertices of the $B - \bar{B}$s which are found close to the beam and decay into shallow tracks. The aim of the design was to minimise the track extrapolation distance to obtain a better impact parameter measurement which led to the modules being inside the primary beam pipe. The VeLo modules thus not only have to withstand the high levels of radiation expected but also have to operate in vacuum (10^{-6}mbar).

Each module has two single sided 300μm silicon n-on-n strip sensors positioned back to back. One sensor has its strips radially arranged while the other has concentric strips allowing the module to provides a three dimensional point for each traversing charged particle. Each side is instrumented by 2048 strips of different pitch (38μm to 98μm) and length(6.2mm to 3cm) which are read by 16 $Beetle$ chips. The resolution of the module depends on the angle of the track and its optimal has been measured to be 4μm. The detector is composed of two halves which

are centred around the beam. Each half, containing 22 modules placed orthogonal to the beam, can move towards and away from the beam.

The aim of the long term testing was to uncover any latent defects on the manufacturing and electronics suffering from infant mortality. This has been achieved by operating the modules under the extreme conditions expected during operation in the experiment. This includes thermal cycling (-30C to 30C) and operation under vacuum for a total of 64 hours. The effect of the temperature cycling and vacuum on interfaces such as glue are monitored by the comparison of before and after thermographs while the module electronics are monitored by periodically exercising them. Results will be presented of the modules tested so far and
the unique challenges of operating silicon strip detector modules in vacuum.

Poster sessions / **91**

Total Dose and Single Event Effects in a 0.25 μm Silicon-On-Sapphire CMOS Technology

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Silicon-On-Sapphire (SOS) CMOS technology has been attractive to radiation tolerant applications. The Sapphire substrate eliminates single-event latch-up (SEL) and reduces the possibility of single event upset (SEE), but the back-channel leakage current could cause problems to circuitry made in this technology. To better understand the radiation effects in this technology and evaluate its feasibility in applications such as Large Hadron Collider (LHC) experiments, we have developed a custom test chip containing various test structures of MOSFET devices and circuits using Peregrine Semiconductor's 0.25μm SOS CMOS technology. This paper presents the total ionization doze (TID) and SEE measurement result and characterization obtained through the chip.

Summary:

Silicon-On-Sapphire (SOS) CMOS technology has been attractive for radiation tolerant electronics. With the insolating sapphire substrate, this technology eliminates the parasitic transistor in the bulk silicon substrate and hence removes the mechanism for latch-ups. This insolating substrate also reduces the possibility of Single event upset (SEU).
SOS technology, like any Silicon-on-insulator technology, does have another source of leakage in the devices, in addition to the edge leakage —back channel leakage at the interface of Sapphire and SiO2. The leakage could cause problems to circuitry since no layout techniques can mitigate this effect. To better understand the radiation effects in this technology and evaluate its feasibility in applications such as Large Hadron Collider (LHC) experiments, we have developed a custom test chip using Peregrine Semiconductor's 0.25μm SOS CMOS technology. We plan to characterize MOSFET devices and circuitry fabricated with respect to TID and SEE.
The test chip contains various configurations of NMOS and PMOS devices, ring-oscillators, resistors, digital standard cells, and D-Flip-flop (DFF) test structures for SEE characterization.
A. Single transistors
The test-chip contains NMOS and PMOS devices with three different channel lengths

(W/L=10μm/0.25μm, W/L=10μm/0.5μm, and W/L=10μm/1.0μm). Each transistor is implemented in four different types of layout: standard, edgeless, two-finger and four-finger.
Since backchannel leakage is proportional to the channel length, we have designed transistors with different length to characterize the back-channel leakage current.
Edge leakage current is proportional to the number of edges in a transistor, therefore the transistors laid out in standard (one-finger), two finger and four-finger transistors can provide us information on the leakage current in transistors without using edgeless layout.
B. Ring oscillator
The test chip contains three different types of ring oscillators to characterize the effect of TID on circuit performance (speed) as well as power dissipation. The ring oscillators include CMOS ring oscillators made of minimum-size inverters, both in standard layout and edgeless layout, and ring oscillator made using current-mode logic.
C. Shift-registers
In order to characterize the single-event effect, we have designed multiple 32-stage shift registers (DFFs) with various setup. The test structures include shift registers with standard-layout, shift-registers with edge less layout, and shift registers with majority-vote circuitry.
In addition, resistively hardened cells have been used extensively to make SRMs rad-hard. In this test chip, we have designed shift-registers with different resistors (1k, 2k, 4k, 8, 16k, 32k, 64k and 128k ohms) connected in the feedback path of the latch to characterize the SEE of the latch and DFF cells.
D. Digital standard cells
The digital standard cells in the test chip include INVETTER, NAND, and NOR gates in both standard and edgeless layout.
E. Current mirrors
we also put down matched current mirror structures in the test chip to characterize possible leakage current in the current mirrors under different radiation levels.

We are currently working on the test bed development for the 0.25μm SOS CMOS test chip. The results will be presented at the workshop.

Parallel Session A4-Optical links / 93

Integration of the CMS Tracker Optical Links

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Analogue and digital optical links developed at CERN are currently being integrated into the CMS Tracker in the magnet-test/cosmic challenge (MTCC), Tracker Integration Facility (TIF) and at the experiment site in Point 5. Similar activities with the same or very similar optical links are also underway for CMS ECAL as well as other CMS detector systems. Recent hardware developments include the dense, in-line optical patch-panels as well as back-end patch-panels. Quality assurance and quality control procedures have been developed and practiced, including the cabling and connection procedure, acceptance tests for the cabling and connections, and tests of final system performance, in particular the analogue optical link gain and dynamic range. A summary of the progress of the integration is given along with the results to date from the various acceptance and performance tests in the MTCC and TIF.

Summary:

The CMS Tracker uses analogue optical links (˜40000 channels) and digital optical links (˜3000 channels) for analogue readout and digital control respectively. The optical links are typically 60m long between the Tracker in the CMS experimental cavern and the counting room in the adjacent cavern. The optical links are based on commercial off-the-shelf parts including 1310nm edge-emitting lasers, InGaAs photodiodes and single-mode fibre-optic cables. The active components are integrated onto compact, rad-hard opto-hybrids at the front-end and into commercial modules at the back-end. The fibre-plant includes single-fibre, 12-way ribbon and 8x12 multi-ribbon cables. There are three patch-panels for the optical fibre connections: one at the front-end, close to the optohybrids, a second very dense, in-line patch-panel within the CMS magnet coil, and the final connection point at the back-end modules.

Recent hardware development has focused on mechanical parts for the in-line and back-end patch panels as well as management of the cable routing on the racks and the storage of excess cable lengths. The in-line patch-panel (optical-PP1) consists of a box in each of 32 phi-sectors of CMS that hold optical cables. Each of these optical-PP1 boxes has 4 removable cassettes that together manage the connections for up to 20 multi-ribbon cables per sector, i.e. up to 1920 optical fibre channels per optical-PP1 box. The envelope of the optical-PP1 volume is approximately (in mm units) 1000x160x80 (length x height x width) and the patch-panel design includes storage of excess lengths of ribbon-cable as well as strain relief elements. Prototypes have been produced and tested in the lab and one optical-PP1 is currently being used in the CMS magnet-test/cosmic challenge (MTCC). The production of the final cassettes will be done in Q2 of 2006.

Concerning the other components of the optical links, all the optical link front-end parts have been produced and are now being integrated into the Tracker front-end detector systems. All the back-end optical receiver and transceiver modules have been produced and integrated onto VME cards or their mezzanine boards. There has been very good quality of integration and system performance with few breakages or failures. The quality control tests of link performance after integration into the Tracker sub-detectors will be described and a summary of the results given, focusing on the analogue optical link gain and dynamic range.

Preparations are beginning for the final optical cabling of the Tracker in CMS at LHC Point 5, which will occur over several months in early 2007. A cabling procedure has been developed and is being practiced in the MTCC and TIF. The final trunk cabling will involve laying and fixing of 560 multi-ribbon cables onto the CMS detector from the in-line patch panel (PP1) out to the balcony on the cavern wall, followed by pulling and routing through the passage into the counting room cavern and onto the final destination rack and back-end patch panel. There will be about 5m slack per cable that will be stored beneath the racks in the false-floor in the couting room. After the Tracker is installed in the cavern, the remaining cabling can be made from the Tracker to the inline-patch panel, involving approximately 4000 12-way fibre ribbons.

Extensive QC (acceptance) tests of the cabling and connections are foreseen and these will be presented. The tests include visual inspection of the cabling, connections, barcode controls, plus measurement of the optical performance in terms of light-loss in the cables and connectors. Time-pressure is expected and these tests of the cables and connectors will be done in parallel with the installation. Either a simple light-source/receiver (for a basic test of the trunk cables only) or a specialized instrument such as an optical time domain reflectometer (OTDR) will be used. The OTDR can be used for testing either the trunk cables alone or for testing the full optical link system. As well as detecting broken optical fibre channels or poorly mated optical connections, the OTDR provides also a precise measurement of the cable lengths in the system which are needed for synchronization of the Tracker.

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The high voltage distribution system for the RICH photon detectors at LHCb

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We present the High Voltage, HV, distribution system for the Hybrid Photon Detectors (HPDs) of RICH1 and RICH2, at LHCb (484 HPDs in total). The HVs (-20 kV, -19.7 kV and -16.4 kV) are supplied by printed circuit boards specially developed to prevent electrostatic discharges and/or corona effects using the limited available volume of the HPD arrays. The circuits that will be presented allow for the splitting, distribution, protection and monitoring of the high voltages. Each board is covered with silicone rubber, which prevents electrostatic breakdown. The complete characterization of the boards will be shown against the main important parameters.

Summary:

Particle identification in the LHCb experiment will be performed by two Ring Imaging Cherenkov Detectors, RICH1 and RICH2, where two arrays of Hybrid Photon Detectors (HPDs) will be allocated. The HPDs will be mounted on column structures. RICH1 will have 196 HPDs, arranged in 2 arrays, each with 7 columns of 14 HPDs per column. RICH2 will have 288 HPDs, also arranged in 2 arrays, each with 9 columns of 16 HPDs per column. The area covered by both arrays of HPDs is about 2.6 m2; the active diameter of a single HPD photocathode is 72 mm.
The photoelectrons produced by incident photons in the HPD photocathode are accelerated and focused by a cross focusing electrostatic field onto a silicon pixel array anode. Three high voltages (HVs) are required for the electron optics: -20 kV, -19.7 kV and -16.4 kV. At the silicon anode, the electrons are detected and read out with CMOS pixel readout chip, each channel containing an amplifier discriminator network. A binary readout of the signals from each pixel is then performed and the data are transmitted via optical fibre to the control room. The front end readout, its voltage biasing and the HPD HV distribution are located on the columns supporting the HPDs.
At this conference we will describe the distribution scheme which delivers the HVs to the HPDs of both RICH detectors. This distribution consists of a series of HV circuit boards specifically designed to provide the three bias voltages, including protective networks. An accurate test system has been developed to fully characterize the boards. The layout includes an "analogue boundary scan"to perform accurate characterization and testing. Results will be presented on the behaviour of the leakage current from the silicone rubber that covers the boards when operated in a humidity-controlled environment.
The maximum radiation levels across the HPD regions are expected to be about 30 kRad (Total Ionizing Dose –TID) and 3×1012 n/cm2 (1MeV equivalent Non-Ionizing Energy Loss –NIEL) over the ten years of running. These values include a safety factor of 2. We have therefore tested the radiation-hardness properties of most of the components used and some prototype boards covered with the insulator.

Parallel Session B3-Trigger session 3 / 95

Setup, tests and results for the ATLAS TileCal Read Out Driver production

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The setup used in the production of the 38 TileCal Read Out Drivers (RODs) and the results are described. Firstly we will explain all the hardware and firmware changes done to the RODs in order to adapt them to the TileCal requirements. Then, we will describe the procedure to test the RODs and the obtained results.

Summary:

The Hadronic Tile Calorimeter (TileCal) for the ATLAS experiment at LHC will send data from 9856 channels by optical fiber links. These channels have to be read out and processed every 10 μs by 32 Read Out Drivers (RODs) with 8 optical inputs each, which will be placed in 4 crates, one per each calorimeter partition. With the aim of using a common ROD motherboard in the ATLAS calorimeters, both LAr and TileCal use the same design for their RODs. This means that the bare boards have to be adapted for the TileCal front end electronics and dataflow requirements. In order to adapt the boards some modifications have been done to the common design. Firstly, hardware modifications have been done, related mainly with the reception circuit due to the different clock frequency used in the data transmission in TileCal and LAr. Firmware modifications have been done in the Processing Units and the Staging FPGAs. This firmware is still being upgraded, but the versions used at the time of production had all the functionalities needed to fully validate the boards.
Once the RODs were adapted for TileCal, we started their validation. The test bench mounted in TileCal laboratory at IFIC-Valencia for these tests will be described. In this test bench we have emulated the detector front end data with the Optical Multiplexer Board (OMB), which is able to generate events at a programmable rate and send them to the ROD. As this board has only 2 optical outputs, an Optical Buffer board was designed by our group in order to replicate each of these optical fibers coming from the OMB up to 16 optical inputs to the ROD. Thus, using one OMB and 2 Optical Buffers, it was possible to test 4 RODs at a time, which represents half a crate.
Following, the test procedure used in order to validate each of the 38 boards (32 required units and 6 spares) will be described. The ROD production tests were completed successfully with excellent results. At a quantitative level, more than 1.3x109 events have been processed and checked without errors, which represents a bit error rate better than 10-14. We will present also the results obtained in G-Link temperature monitoring studies. These components reach high temperatures while they are powered and need continuous cooling in order to guarantee not to overheat above the threshold recommended by the manufacturer. At a qualitative level, we will present the results obtained regarding the reconstruction of energy, time and $\chi 2$ in the DSPs, as well as the upgrades done at the firmware level in order to reach a more optimized system. Once the RODs were validated in the test bench, they were installed in the ATLAS electronics cavern (USA15), their final placement, to read out and process data coming from the TileCal detector and participate in the TileCal commissioning.

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Signal Integrity Studies at Optical Multiplexer Board for TileCal System

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The Optical Multiplexer Board is a card included in the TileCal Data Acquisition System; it is designed to receive two optical fibers with same data from front-end boards and decided which has correct data.
Inside this card we have different transmission lines that need to be studied; signal integrity problems such as signal delay, reflection, distortion and coupling should be analyzed.
This paper presents the results of the signal integrity studies at the Optical Multiplexer Board for TileCal System.

Summary:

TileCal is the hadronic calorimeter of the ATLAS experiments. It consists, electronically speaking, of 10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system (DAQ) following the assertions of a three level trigger system.
In the acquisition chain, place is left for a system which has to perform pre-processing and gathering on data coming out after a good first level trigger before sending them to the second level. This system is called the Read Out Module (ROD). Before the ROD we have a pre-ROD card, called Optical Multiplexed Board (OMB), able to analyze two fibbers, both of then carrying the same data, to provide the correct one to the ROD input.
The interest of this project was justified in February 2003, when a preliminary study appeared. This proposal shown a solution for OMB based on exhaustive on-line analysis of the data carried by both of the fibbers, using FPGAs for implementation.
Universidad de Valencia –IFIC (Spain) team showed the greater interest to deal with this project, to make a first prototype to study technical viability. In particular, the main goals are:
• Fibber optic switching to take advantage of redundancy
• Obtain real (production) costs
• Have a development platform (hw - sw)
• Try different alternatives for data error analysis (CRC, etc.)
In this paper we want to show the Signal Integrity Studies made to this card; OMB is a high-speed digital design and Signal Integrity has become a critical issue.
The term Signal Integrity addresses two concerns in the electrical design aspects, the timing and the quality of the signal. The goal of this Signal Integrity analysis is to ensure reliable high-speed data transmission.
We can divide the studies in two parts, the pre-layout (without which prototypes may never leave the bench) and the post-layout (without which products may fail in the field).
In the pre-layout stage, Signal Integrity analysis they were used to select technology for I/Os, clock distributions, chip package types, component types, board stackups, pin assignments, net topologies, and termination strategies.
With an initial physical layout, post-layout Signal Integrity analysis verified reflection noise, ringing, crosstalk and ground bounce.
The results were correct and allowed the accomplishment of the card that at the present time is in operation at CERN.

Parallel Session B2-Trigger session 2 / 97

Installation and Test of the ATLAS Muon Endcap Trigger Chamber Electronics

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For the detector commissioning planned in 2007, a sector assembly of the ATLAS muon endcap trigger chambers
is progressed in CERN intensively. Final technical test for the electronics mounted on a sector must be
accomplished at this stage. For systematic test of the electronics, we have developed a DAQ system on top of the
ATLAS online software framework. The system is not dedicated only for this test, but can be used also as the
front-end detector part of the overall ATLAS DAQ system. We presume the extension to the ATLAS final one
from the presently developed DAQ system must not be hard if it is built up in the common software framework.
In this presentation, we report installation of the electronics on the sector, development of the DAQ system and
its validity check performed through the electronics test at the chamber assembly stage.

Summary:

For the detector commissioning at LHC planned in 2007, a sector assembly of the ATLAS muon-endcap chambers is progressed intensively in CERN. The thin gap chamber (TGC) is used for the muon-endcap trigger
system. The muon endcap system covers the both endcaps of the detector (1.1<abs(eta)<2.4) to detect isolated muons and give the level-1 muon trigger signal with two ranges of the transverse momentum (pt) of
low-pt > 6 GeV/c and high-pt > 20 GeV/c.
As at least three measurement points per track is necessary to identify a muon with even such coarse momentum estimation, there are three TGC discs per endcap (one has three layers with triplet chambers, and
the other two discs have two layers each with doublet chambers). Every disc has commonly twelve sectors.
This 1/12 sector is a construction unit for the trigger muon endcap system for both the chambers and electronics. The sector is also the unit for the trigger and readout system.
The electronics systems mounted on a sector are the front-end ASD (Amplifier-Shaper-Discriminator), readout chain (pipeline buffers, derandomizers and parallel/serial converter), trigger decision logic for the
level-1 low-pt muon candidate signals, miscellaneous control and test circuits and Detector Control System
(DCS). We also mount modules for high-pt decision logic as well as readout data concentrator nearby the
sector, but these are not directly mounted on it.
Once the sector is installed in the whole ATLAS detector system in the cavern, one cannot access easily its
electronics as well as cables. We have to test the electronics system after completion of the sector and fix or

repair quickly if we find incomplete connection of cables or damage of electronics components. Furthermore
since the system involves the level-1 trigger generation logic, timing adjustment of the electronics at this
assembly stage is also the key issue from the signal synchronization point of view.
In order to check all the functionalities and adjust timing of the electronics system, it is necessary to do almost full DAQ operation to the sector. We have made a lot of DAQ systems so far for the standalone electronics consistency check or the integrated beam test with TGCs using the high energy muon beam. These
DAQ systems constructed have been dedicated for specific purposes, but none of them can be used in the
actual ATLAS online system, although various software codes in particular for individual module controls are
re-usable with minor modification. For the present electronics test of the sector assembly, we have reformed
the DAQ system once more. We made it with being fully complied with the ATLAS online software framework.
In this presentation we will describe the installation and mass-test procedure of electronics using this DAQ
system in detail and some experience to fix problems encountered actually in the sector assembly. We would
like to discuss the timing adjustment procedure in detail. If the adjustment in the sector level is done well,
then the timing signals in larger parts (disc, side or overall muon endcap) will be smoothly synchronized. We
discuss finally the front-end DAQ system itself and how we have evolved the system through the verification
process of the electronics installation.

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Commissioning and calibration of the CMS micro-strip tracker

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The CMS micro-strip tracker data acquisition system is based on an analogue front-end ASIC, optical readout
and an off-detector VME board that performs digitization, zero-suppression and data formatting before
forwarding event fragments to the online event-building farm. Sophisticated “commissioning”procedures are
required to optimally configure, calibrate and synchronize the 10M readout channels. The procedures are
defined by data acquisition loops that configure and control the readout and local trigger systems, perform
event building and data analysis. We present an overview of the commissioning procedures and results from
the CMS Cosmic Challenge and large-scale system tests at the Tracker Integration Facility.

Summary:

The micro-strip tracker for the CMS experiment, comprising a sensitive area of over 200m2 and 10M readout
channels, is unprecedented in terms of size and complexity. The readout system is based on a 128-channel

analogue front-end ASIC, optical readout and an off-detector VME board that uses FPGA technology to perform digitization, zero suppression and data formatting before forwarding event fragments to the CMS
online computing farm.

Commissioning such a large-scale readout system requires sophisticated procedures to bring the detector
into an operational state that is suitable for physics data-taking. These procedures comprise several independent tasks that fall into one of the following categories: automated detection of the readout system
partitioning and cabling; optimization of hardware configurations; synchronization of the front-end system,
both internally and to LHC collisions; and determination of calibration constants that are used by the hardware
and, in some cases, the CMS reconstruction software. These procedures will be used to validate the operational functionality and performance of the detector during the start-up phase of the experiment and
will also be performed between fills to guarantee optimum detector performance during the subsequent period of data taking.

The software implementation for the commissioning procedures is divided between the CMS online and offline
software frameworks, known as XDAQ and CMSSW, respectively. XDAQ provides a core set of services and
tools, including: a fast communication protocol for peer-to-peer messaging between processes registered
with the framework; a finite-state machine schema and a slower communication protocol for configuration of
the framework processes; and standard event builder and memory management tools. CMSSW is the offline
software project comprising physics simulation, reconstruction, analysis and High-Level Trigger software, and
provides services such as a conditions database and a Data Quality Monitoring framework.

The commissioning procedures are defined by data acquisition loops that configure and control the readout
and local trigger systems, perform event building and data analysis. Communication between the various,
distributed "hardware supervisor"processes is achieved using the XDAQ framework, which allows to automate
the data acquisition loops, so removing the need for repetitive run control sequences and complex bookkeeping. Consequently, this accelerates detector commissioning and start-up. Data analysis is performed
within CMSSW, which determines optimized hardware configuration parameters and calibration constants from
reconstructed calibration pulses, timing delay curves, dynamic range curves and other features of the front-
end ASIC data stream. These optimized configurations and calibrations are then stored in a "hardware configuration and calibration"database and provide the basis for subsequent commissioning tasks or physics
runs.

The software design ensures that both the local computing resources allocated to the tracker sub-detector and the global resources provided by the online computing farm can be used transparently. The former option
will be the default configuration used during the start-up phase. The latter offers significant improvements in
detector readout speeds and CPU processing power, thus providing the possibility to reduce turn-around times between physics runs.

The software is to be used for the final, complete micro-strip tracker, as well as during the CMS Cosmic Challenge and large-scale system tests at the CERN Tracker Integration Facility.

Poster sessions / 99

The CDF Run II Silicon Detector

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The CDF Run II Silicon detector is one of the largest operating Silicon detectors in high energy physics. It has 6m2 of Silicon sensors with 722,432 channels read out by 5456 chips. The Silicon detector allows precision tracking, vertexing and is used in the hardware displaced vertex trigger.

The CDF silicon detector had a very challenging commissioning period of 18 months. However the detector has been operating reliably over the last 3 years and it has recorded more than 1fb-1 of data. There will be a brief review of detector commissioning, the effects of radiation damage and its impact on the CDF physics programme.

Summary:

The Run-II CDF Silicon detector is one of the largest operating Silicon detectors. The total surface area covered by the Silicon sensors is ˜6m2. The complete system totals 722,432 channels read out by 5456 chips. The detector is subdivided into three sub-detectors: L00, SVX and ISL.

SVX is the core of the CDF silicon detector. It consists of 5 concentric layers of Silicon arranged as twelve 30o wedges in r. SVX is used by the hardware displaced vertex trigger allowing it to participate in the Level-2 trigger decision making. This allows CDF to trigger directly on B hadrons and other long lived particles.

L00 is a single layer of single sided silicon attached directly to the beam-pipe. This allows precision position measurements before multiple-scattering by inactive material. Due to its proximity to the beam, radiation hard LHC sensors were used which can be depleted to 500V.

The Intermediate Silicon Layer (ISL) was added to extend the forward acceptance of the Silicon tracker to |=2 and to link tracks from SVX to the Central Outer Tracker (COT); the CDF wire chamber. The sub-detector is arranged as two forward layers and one central layer.

The commissioning of the CDF Silicon detector took considerable effort. It took almost 18 months before the detector was considered as operational. This was due to the large number of problems encountered which included blocked cooling lines, noise on L00 and the wirebond resonance problems. Despite these initial problems, the detector has now been running stably over the last 3 years. 92% of the detector is powered with almost 85% returning data with a digital error rate < 1%.

The Silicon detector has been exposed to 1.5fb-1 of proton-anti proton collisions. Evidence of radiation damage of the sensors has been observed with increases in the bias currents and the evolution of the depletion voltage. There will be a presentation of these results and a discussion on the implications upon detector performance and lifetime.

A highlight of the CDF physics programme has been the measurement of the Bs mixing. This single measurement now defines the world average and the Silicon detector played a critical role in this measurement.

Parallel Session A3-Readout, commissioning and integration 3 / 100

Recent Results on the Performance of the CMS Tracker Readout System

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The CMS Silicon Tracker is comprised of a complicated set of hardware and software components that have been thoroughly tested at CERN before final integration of the Tracker. A vertical slice of the full readout chain has been operated under near-final conditions. In the absence of the tracker front-end modules, simulated events have been created within the FED and used to test the readout reliability and efficiency of the final DAQ. The data are sent over the final SLink 64 bit links to the final FRL modules at rates in excess of 200 MBytes/s per FED depending on setup and conditions. The current tracker DAQ is fully based on the CMS communication and acquisition tool called XDAQ. This paper discusses setup and results of a vertical slice of the full Tracker final readout system. Simulated data is created with varying hit occupancy (1-20%) and trigger rates (<200KHz) and the resulting behaviour of the system is recorded. Data illustrating the performance of the system and data readout is presented.

Summary:

The CMS Silicon Tracker will produce large amounts of data, which must be read out by the Front End Drivers (FEDs), which are 9U 400mm VME64x cards that process the raw data from a subset of 192 APV25 silicon readout ASICs, equivalent to 0.2% of the tracker. After multiplexing and streaming, the data from the tracker are routed via analogue optical links to the FEDs. 96 optical channels are then digitised to 10bit precision at 40MHz and processed in large FPGAs, before being collated into events and sent to the CMS DAQ via either VME or the SLINK-64 protocol.

Under final running conditions the SLINK-64 protocol must be used to enable a data throughput of up to 200 Mbytes/s per FED. It is clear therefore that such a system must be well tested before the final system is assembled at Point 5 on the LHC ring, so that the final operation of the system is certified. However, during the testing and assembly stages in 2006 there are not enough Tracker front-end modules available in order to drive a large enough number of FEDS to make a true vertical slice test. Nominally a vertical slice would consist of 1 whole crate of FRLs, which corresponds to two whole crates of FEDs ˜ 32 in total. Therefore another method of testing the readout system without the need for the detector modules is required. This is achieved by creating Pseudo-Random fake events within the front-end modules of the FEDs themselves, which are injected directly into the FED exactly where the optical data samples would arrive from the final system.

In order to qualify the hardware readout system and operation of the DAQ, this system was set up in building 904 on the CERN Prevessin site. This system is capable of creating variable event occupancies in the front end of the FED, without the need for the actual detector modules to create the event frames from the APV25 front-end readout chips. The “fake events”which are created in the FED have the capability to be set to operate at any occupancy between 0 and 100% and also include a pseudo random adjustment to the pedestals of the fake APV frames, in order to simulate the random nature of the hits in the front-end silicon detector modules.

The main purpose of this test is to qualify the functionality of the entire trigger and readout chain from the LTC –TTCci –TTCex –TTCoc –APVE –FMM –FRL –FED – Transition Card - Slink Sender Card and DAQ software. Operating the system under various conditions by varying the trigger rate and data throughput (occupancy). In

doing so one can investigate the limiting factors of the system to gain a better understanding of how the final tracker will perform.

The results of this test have shown that the system is stable for periods of time over many hours when running at 150KHz Poisson distributed triggers, the back pressure from the APVE and FED, via the FMM, works perfectly to throttle the trigger rate down to a sustained rate of 72Khz when operating the FED at 5% occupancy. At lower occupancies, 2-3%, more representative of nominal data taking conditions in the final Tracker, the system runs without interruption at trigger rates around 100 KHz sustained. A number of other scenarios have also been tested and will be presented in the paper, and if time permits, some nominal testing of the same system with real detector modules will also be included.

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Ideas on DC-DC Converters for Delivery of Low Voltage and High Currents for the SLHC / ILC Detector Electronics in Magnetic field and Radiation environments.

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We are exploring various way of employing 48 volt DC-DC converters capable of running in high magnetic fields and /or radiation environments of the SLHC and ILC detectors. Tradeoffs with respect to voltage conversion ratios, currents deliverable, radiation, and magnetic field are explored.

Summary:

We have been thinking about DC-DC voltage regulators capable of running in up to 5T field and LHC upgrade radiation environment.

Yale University was responsible for the design of the 2.5 V power distribution of the CMS ECAL detector in which the front end electronics requires 50,000 amps. The 750 odd power leads from the power supplies to the 36 super modules dissipate 100 Kilo Watts. The efficiency of the power delivery form the output of the power supplies is less then 40%.

So we ask ourselves "Is there a better way to deliver power to the front end electronics". There may be techniques available in different fields to need our requirements of radiation environment, high power density and magnetic fields.

Hera is a few different new ideas.

1. Last year Intel Corporation gave a demonstration of a 100 MHz Dc-DC converters built in 90 nm technologies. For several years, their Circuit research laboratory has explored air and ferrite coils with frequencies of up to 480 MHz. They have showed the feasibility of building air coils in 90 nm silicon die. See Ref.1
2. VICOR Power Corporation, a maker of DC-DC converters, has 200 watt power density in a small package of the size of a matchbox with half the thickness. Their simulations show that for a Sine Amplitude Converter Voltage Transformation Module designed to convert 48V to 2V at up to 80A in 1/2 cubic inch using a shielded air core transformer and achieve a full load efficiency exceeding 90%. See Ref.2

3. Many semiconductor companies have ICs with complete DC-DC regulators with output currents of a few amps. The market for these is driven by battery operated handheld gadgets like cell phones, Ipods, blackberries etc.
4. In the past 15 years, there has been a great deal on interest in the power distribution driven mainly by the PC industry. There are books and publication on new topologies that can be used.

The silicon trackers for the SLHC needs a few amperes for the strip hybrids and the Staves/ladder mat take 35 amps. The total tracker current may be about 30 Kamps.

The applications shall be common to all the LHC upgrade detector systems and applicable to ILC. The ILC detectors power can be pulsed to keep the average power low but the electronics need the voltage and peak current to operate.

This development is being pursued with some involvements of the companies like VICOR, Intel Corporation's research laboratory, Wiener, CAEN etc.

We shall discuss the tradeoffs with the magnetic filed, high radiation environment and current that can be delivered in a single unit.

Ref. 1: Proceedings of the 2004 International Symposium on Low Power Electronics and Design (ISLPED'04) 1-58113-929-2/04 $20.00 ACM
Ref. 1: http://www.vicorpower.com/products/vichip/vtm/index.php

Parallel Session B4-Trigger & DAQ session 1 / 102

Recent developments on th ALICE central Trigger processor

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The ALICE Central Trigger Processor is designed to process signals
from triggering detectors and send appropriate trigger signals and
data to participating detectors. The ALICE system allows dynamic
partitioning of the detector, past-future protection appropriate to
each detector's electronics, and a number of different monitoring
and diagnostic functions. The system has now been built, and
consists of 6 6U VME boards with logic implemented on ALTERA CYCLONE
FPGAs. In this paper the characteristics of the system are described
and its performance in tests described. Tests related to the system
integration will also be presented.

Summary:

The primary purpose of the ALICE experiment is to study heavy ion
collisions. Under these conditions the luminosity will be far lower
than in proton proton collisions (L = 10^27 cm-2 s-1 in Pb-Pb

collisions). The ALICE experiment programme will include runs with
several different ion species, and also both proton nucleus and pp
runs. Note that several of the detector subsystems would not be able
to follow the high luminosity pp running conditions, and for this
reason ALICE receives a lower pp luminosity of around 10^30 cm-2
s-1.

The ALICE trigger system operates with interaction rates between
about 8 kHz and 300kHz. It must provide a number of different
services. There are three different trigger levels (L0, L1 and L2)
with latencies from 1.2 microseconds to 88 microseconds. The system
allows dynamic partitioning in order to make optimum use of detector
readout. The system has a flexible provision for past-future
protection. The system also allows for special provision for high
priority (”rare”) triggers. These features have been described in
detail at previous workshops.

The trigger system was built in 2005 and has been tested in
considerable detail. There are six different types of 6U VME board
in the CTP system, and two further boards required for fan-in and
trigger distribution. Apart from the fan-in board, which is passive,
these share a common architecture base on ALTERA CYCLONE FPGAs.
These FPGAs are loaded from a flash memory, which is loaded via VME.
This feature makes it easy to distribute firmware upgrades, as has
been done in the case of the Local Trigger Unit (LTU), where units
are in use at ALICE institutes around the world.

The three trigger levels involve several signal types from the CTP.
The L0 trigger is sent as an LVDS signal; the L1 signal is sent on
channel A of the TTC system; trigger data associated with level 1 is
sent as a message on channel B of the TTC system; the L2 trigger is
sent as a message on the TTC system after a delay, currently 88
microseconds, to allow for the longest required past-future
protection interval. Additional possibilities exist in the case of
calibration triggers. Examples of these sequences from CTP
measurements will be shown, and in addition a measurement of the CTP

internal decision time.

In order to control the CTP an extensive software development was required. The ALICE CTP is in the experiment cavern, and therefore is inaccessible during running time. For this reason particular attention has been paid to monitoring and debugging facilities. Configuration of the system is possible in a two-tier system, with experts able to change all parameters while normal users select already prepared configurations from a database. Trigger data is sent to dedicated monitoring processors, to the data acquisition and to the detector control system. A protocol based on SMI++ is being developed to make an interface to the experiment control system (ECS). All these systems will be reviewed. A more detailed description of the CTP software is the subject of a separate contribution to this conference.

Parallel Session B4-Trigger & DAQ session 1 / **103**

Timing in the ALICE trigger system

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In this paper we discuss trigger signals synchronisation and trigger input alignment in the ALICE trigger system.

The synchronisation procedure adjusts the phase of the input signals with respect to the local Bunch Crossing (BC) clock and, indirectly, with respect to the LHC bunch crossing time.

Alignment assures that the trigger signals originating from the same bunch crossing reach the processor logic in the same clock cycle. It is achieved by delaying signals by an appropriate number of full clock periods.

We discuss the procedure which will allow us to find alignment delays during the system configuration, and to monitor them during the data taking.

Summary:

This presentation will deal with the synchronisation and alignment of the trigger signals in the ALICE trigger system.

Synchronisation adjusts the phase of the input signals with respect to the local Bunch Crossing (BC) clock and, indirectly, with respect to the LHC bunch crossing time. (The synchronisation delays are within one clock period: 0-25 ns.)

Synchronisation is necessary at two points of the Alice trigger system. The phases of trigger inputs relative to the Central Trigger Processor

(CTP) BC clock and the Local Trigger Unit (LTU) inputs relative to
the LTU BC clock are to be adjusted.
The system provides for an automatic measurement of
the phase shift of all trigger inputs relative to the CTP clock
and the phase of the LTU inputs relative to the local LTU clock.
In both cases, following the measurement, a programmable hardware option
is used to adjust the phase of the signals appropriately.

Alignment assures that trigger signals originating from the same bunch
crossing reach the processor logic in the same clock cycle. It is achieved by
delaying signals by an appropriate number of full clock periods.

Two ways of automatic alignment are discussed.
The first is based on the activity plot of the LHC beam structure
for different trigger inputs;
the other procedure is based on a correlation analysis of
different trigger inputs.

While the synchronisation is a fully internal procedure of the trigger system,
alignment relies on the presence of external physics signals.
The feasibility of the method is evaluated in three different cases:
- without a beam (cosmic trigger),
- with one beam (beam gas interaction)
- and with both beams.
The efficiency of these procedures depends on the amount of data collected
for the analysis.
There are two different ways of collecting the data for the alignment
analysis:
- the data recorded through the ALICE data acquisition system
(DAQ alignment data),
- the data recorded directly in the CTP (CTP alignment data).
The CTP alignment data can be collected by the CTP alone; independently of
the data acquisition system, because of the presence of a local memory
(snapshot memory) on each CTP board.

We shall present an estimate of
the time necessary to produce reliable alignment delays in different
circumstances (cosmic trigger, beam gas interaction and beam-beam interaction)
and using different collecting methods (DAQ or CTP data).

Finally a procedure for setting the synchronisation parameters
and the alignment delays will be proposed.
In addition a possible strategy for monitoring the synchronisation and
alignment will be presented.

Plenary Session P7-Beam, SLHC & closeout / 105

Stacked Tracking for CMS at Super-LHC

Author: John Jones[1]

Co-authors: Andrew Rose [1]; Benjamin Constance [1]; Costas Foudas [1]; Geoffrey Hall [1]; Keija Zhu [1]; Mark Raymond [1]

[1] *Imperial College London*

We report on recent work on the design of a pixel detector for CMS at the Super-LHC.
This work builds on previous studies on a tracking detector capable of providing
track stubs to be used in the Level-1. We now focus on the use of two layers of

tracking, each comprising stacks of pixel sensors with 20x50x10μm3 pitch (θxφxr) and separated by a few millimetres. Preliminary work on track reconstruction in Field Programmable Gate Arrays (FPGAs) is also presented.

Summary:

Currently groups of researchers are actively discussing possible scenarios of upgrades of the LHC machine. According to the most financially realistic scenario the LHC will be upgraded to provide proton beams of an order of magnitude larger intensity (1035 cm-2 sec-1) colliding at twice the frequency (80 MHz) of the present design but have the same centre of mass energy. This machine design is commonly referred as the Super-LHC and it is expected to be operational after 2015. A consequence of this design is that the backgrounds due to minimum bias events will increase by at least a factor of 5. It is anticipated that CMS will require tracking information in order for the trigger to be operated efficiently in this environment.

The performance of a single stack has been discussed in LECC 2005. In this paper we review this approach, using a PYTHIA-based Monte Carlo as a reference. We then expand the approach to cover the use of multiple stacks (in particular the double-stack method), showing potential improvements in reconstructed resolution (both momentum and position) as well as reconstruction purity. It has been found that the reconstruction method can be implemented in the current generation of FPGAs, on a comparable scale to the other trigger systems currently in CMS, and within the current time budget of the Level-1 trigger.

Poster sessions / **106**

Radiation Testing of electronic components and systems for the LHC experiments and machine : summary and future

Authors: Federico Faccio[1]; Thijs Wijnands[1]

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A statistical summary on 6 years radiation testing for the LHC machine and
experiments will be presented. The data shows that radiation tolerance assurance to
cumulative damage effects was taken into account as an engineering constraint in a
rather early stage in the project. The issue of Single Event Errors was only
recognized as major issue at a much later stage in the project and this resulted in
a sharp increase in proton beam testing in dedicated facilities at Université
Catholique de Louvain and the Paul Scherrer Institute. Presently, the requests for dedicated radiation testing are reducing because series
produced electronic equipment is being installed in the LHC. However, the requests
may well rise again when the R&D for radiation hard semiconductor devices for the
LHC upgrade gets to full swing. The suitability of the presently used radiation
facilities for this task will be assessed.

Plenary Session P6- LHC Machine / 107

An on line radiation monitoring system for the LHC machine and experimental caverns

Authors: Christian Pignard[1]; Thijs Wijnands[1]

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With an unprecedented amount of electronic systems exposed to radiation in the LHC, reduced operational efficiency due to radiation induced failures in electronic equipment has become an issue for both the machine and the experiments. The RADMON radiation monitoring system presented here has been designed to measure radiation at the location of electronic equipment in the LHC tunnel and in the experimental caverns. On line measurements of the dose, dose rate, hadron flux and hadron fluence will be used to separate and identify radiation induced failures, to evaluate the performance of electronic equipment under irradiation, to provide insight into the way the machine is operating and to measure the efficiency of the shielding structures. The radiation sensors consist of 4 Mbit of commercial SRAM (0.5 ⊠m), 2 Radiation sensitive Mosfets with different gate oxides thicknesses and 3 PIN Photodiodes in series. A detailed description of the radiation tolerance readout board design will be given.

Parallel Session A5-DAQ and Optical technology / 108

PCI Express Over Optical Links for Data Acquisition and Control

Author: Marco Bellato[1]

Co-authors: Andrea Triossi [1]; Guang Meng [1]; Marina Passaseo [1]; Roberto Isocrate [1]; Sandro Ventura [1]

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PCI Express is a new I/O technology for desktop, mobile, server and communications platforms designed to allow
increasing levels of computer system performance. The serial nature of its links and the packet based protocols allows an easy geographical decoupling of a peripheral device. We have investigated the possibility of using an optical
physical layer for the PCI Express, and we have built a bus adapter which can bridge, through such a link, remote
busses (> 100m) to a single host computer without even the need of a specialized driver, given the legacy PCI
compatibility of the PCI Express hardware. This adapter has been made tolerant to harsh environmental conditions,
like strong magnetic fields or radiation fluxes, as the data acquisition needs of high energy physics experiments
often require.

Summary:

PCI Express represents a radical move from traditional I/O architectures in that it replaces parallel multi-drop busses with serial multi lane switched point-to-point links. Being each lane bi-directionally driven at 2.5 Gbit/s, the capacity of the channel after 8b/10b encoding is fixed at 250 MByte/s times the number of lanes. While this bandwidth outperforms the capacity of former standards, the points worth considering for our goal are not only concerned with speed. The new serial technology adopts a “communication centric”approach: the load-store operations between two nodes are performed exchanging framed packets in accordance to a suite of stacked protocol layers taking care of the physical, link and transaction issues of the channel. In case of PCI Express all these activities are carried out at the hardware level, with no software intervention. Clearly this load-store model logically matches the model of field bus control in which a host and a networked peer node exchange software arranged packets to access memory and registers of the field bus for I/O operation. To investigate and further extend this parallelism to its practical consequences we have addressed a number of activities in the context of the INFN Gr. V funded project LINCO.

LINCO project was involved in research and design for the development of an optical adapter that translates PCI express signals to/from the optical physical layer and which, using commercial bridges, could be fitted into legacy bus standards (PCI, CompactPci, VME).

First of all we had to investigate a non standardized physical medium for the PCI Express protocol, namely running on an optical fiber link. The figure of total jitter reserved for the interconnection by the specifications deserves careful attention, so strict measurements of jitter and data signal integrity were done to characterize the link.

Then LINCO project resolved to develop a Printed Circuit Board able to translate the PCI to PCIe protocol and then to convert the PCIe electrical signals to optical signals. We chose the PCI Mezzanine Card (PMC) standard in order to meet different standards of field bus like VME or Compact PCI. Two prototypes have been assembled and configured for reverse and forward operation. The reverse type has been accommodated in a PMC to PCI adapter to fit into a host PC, while the forward type has been tested with a passive adapter in a CompactPCI crate and with an active adapter (hosting a Tundra UniverseII PCI to VME bridge) in a VME environment. The two boards were linked by a 100m multimode fiber with Intel SFP optical transceivers for data and clock paths. In the CompactPCI case we could trasfer data at the full legacy PCI throughput (132 MB/s) to a remote device, while in the VME case transfers were achieved on a VME slave the with a 2 to 3 μs single access latency.

To qualify our design for LHC use we have setup a radiation test with protons of 63 MeV energy. The fluence measured on the board was 5·1010 p/cm2 corresponding to a total ionizing dose of less than 7 Krad. During the test, the boards were active and a certain number of VME registers were continuously written with random patterns, read back and compared for SEU checking and logging. We could observe only a negligible total dose effect on the board itself but a consistent dose effect on the SFP transceivers. To ease operation at LHC, a watchdog-type mechanism for automatic reset has been put in place using the Altera programmable logic device

on the board. The watchdog drives the gate of the high current MOS switch in series with the main power supply of the board and is continuously reset through the GPIO bus of the bridge.

Poster sessions / 109

CMS ECAL Low Voltage system

Author: Alexander Singovski[1]

[1] *University of Minnesota & CERN*

The final design of the low voltage power system of the CMS ECAL detector will be presented. The particular requirements of the ECAL on-detector electronics powering will be discussed and details of the W-IE-NE-R MARATON system design related to these features will be pointed out. All tests performed with the ECAL-specific version of the MARATON power supply units will be summarized. The units acceptance and burning-in procedure will be presented.

Poster sessions / 110

CMS ECAL optical cables testing

Author: Alexander Singovski[1]

[1] *University of Minnesota & CERN*

CMS ECAL detector will require more than 400 dense multi-ribbon optical cables, made of single mode 9 micron quartz fibers, for the data, control and trigger data transfer between on-detector and off-detector electronics.
Although all cables will be tested before installation, one cannot guarantee no single fiber damage during the mass cable pooling campaign at the underground area. Hence, all optical lines have to be tested after installation.
The available industrial test systems will be reviewed and motivation for the special system design will be discussed. The two portable optical components testers designed for the CMS ECAL application will be presented.

Plenary session P1-Opening plenary / 111

Introduction by the Director of IFIC

Author: Juan Antonio Fuster Verdú[None]

Plenary session P1-Opening plenary / 112

Particle and Astroparticle Physics in Spain

Author: Antonio FERRER[None]

Plenary session P1-Opening plenary / **113**

The LHC machine status, calibration run and commissioning plans

Author: Mike LAMONT[None]

The status of the ongoing LHC installation is described with attention given to the long straight sections around the experiments.
An overview of the proposed commissioning schedule for 2007 and 2008 presented. This schedule includes a calibration run at the end of 2007 which aims to deliver collisions at 450 GeV beam energy. The details of this run and planned beam conditions are summarised.

The full commissioning to 7 TeV will be a challenging exerecise and an overview of the plans for 2008 is also given.

Finally, the beam related issues associated with the LHC upgrade are introduced.

Plenary session P1-Opening plenary / **114**

CMOS directions in industry

Author: Ernesto PEREA[None]

The seminar addresses recent advances in CMOS technologies. Technological limits, device-related limits and fundamental physical limits linked to the diminished feature sizes and their impact on analog performance and digital integration potential are discussed. Progress is made in new semiconductor/dielectric materials and in band-gap engineering to overcome some of the unfavorable effects at the microscopic/quantum level. Overall system cost pressures call for improved fabrication yields, forcing new tightly-coupled system-architecture-circuit-device design techniques in a context of ever increasing parameter variability. A detailed account of current device architectures beyond 45nm including performance boosters will be presented together with their associated advantages and risk factors. New paradigms will be necessary to reduce the analog-digital divide. One possible approach is the use of long-time known sampling techniques for Analog and RF circuits, opening the way to fully integrated reconfigurable systems, a concept that has been around for many years, but that is regaining interest.

Plenary session P1-Opening plenary / **115**

3D electronics

Author: Vyshnavi SUNTHARALINGAM[None]

Traditional integrated circuits consist of a single layer of transistors interconnected with multiple layers of metal wiring.
Three-dimensional integrated circuits (3D-ICs) consist of two or more active circuit layers that are vertically stacked and interconnected at high density. In addition to reducing the wire length, 3-D interconnection of active devices offers the potential for radically new computer architectures, extremely dense memories, and advanced focal planes that utilize the inherent parallelism inherent in the 3D technology. In this talk we will present work at MIT Lincoln Laboratory over the last several years which targets new classes of focal planes which exploit the parallelism of dense vertical interconnection reaching to small pixel sizes.

Plenary session P2-Plenary ILC & high reliability / **116**

Detector and readout systems for the ILC

Author: Tim Greenshaw[1]

[1] *Liverpool*

The challenges of experimentation at the International Linear Collider are discussed and the different detector concepts designed to cope with those challenges presented. The differing concepts lead to various alternative technologies for the major ILC detector components. These are briefly presented and discussed.

Plenary session P2-Plenary ILC & high reliability / **117**

High Availability Electronics standards

Author: RAY LARSEN[1]

[1] *Stanford Linear Accelerator Center For the ILC High Availability Electronics R&D Effort*

Availability modeling of the proposed International Linear Collider predicts unacceptably low uptime with current electronics systems designs. High Availability (HA) analysis is being used as a guideline for all major machine systems including sources, utilities, cryogenics, magnets, power supplies, instrumentation and controls. R&D teams are seeking to achieve total machine high availability with nominal impact on system cost. The focus of this paper is the investigation of commercial standard HA architectures and packaging for Accelerator Controls and Instrumentation. Application of HA design principles to power systems and detector instrumentation will also be discussed.

Plenary Session P3-Optoelectronics / **118**

Optoelectronic developments for remote-handled maintenance tasks in ITER

Author: Marco VAN UFFELEN[1]

Co-authors: F. Berghmans ; P. Leroux

[1] *SCK*

Periodic maintenance operations during shut down of the future International Thermonuclear Experimental Reactor (ITER) will have to be performed in a severe nuclear environment, exposing operating tools inside the reactor vessel to temperatures ranging from 50°C to 200°C, with total doses that can reach MGy levels. Radiation tolerant remote-handling technology will therefore play a major role during these maintenance tasks. Connecting remotely operated actuators and sensors with the control room requires bulky and shielded umbilicals. Their management could be eased by applying radiation tolerant communication links with multiplexing capabilities, for which fibre-optic technology is considered as a potential EMI-free solution.
We present the main results obtained at SCK•CEN over the past years towards the development of radiation tolerant fibre-optic communication links, including the individual optical components such as optical fibres and power couplers, laser diodes and photodetectors, as well as their associated electronic driver circuits.

Plenary Session P4-HEP electronic and ASIC trends / 119

3D Circuit Integration for High Energy Physics

Author: Ray YAREMA[None]

Industry is pursuing 3D integrated circuits to enhance circuit performance. The techniques and technologies being employed can be of benefit to the High Energy Physics community. There are two general approaches that can be followed: die to wafer bonding, and wafer to wafer bonding. Each has its own benefits. Both of these approaches are being investigated at Fermilab. The die to wafer bonding approach is being studied through the services of two different vendors using devices produced at Fermilab for a previous experiment. The wafer to wafer bonding approach is being pursued with one vendor using their 0.18 um SOI process. The capabilities of these two different approaches are presented through a brief description of devices that have been fabricated. Critical processes for 3D integration are described. Design of a 3D circuit in an SOI process for High Energy Physics is presented

Plenary Session P4-HEP electronic and ASIC trends / 120

Technology Scaling and CMOS Analog Design

Author: Franco Maloberti[1]

Co-author: Franco MALOBERTI [1]

[1] *University of Pavia*

Modern and future ultra-deep-submicron technologies make challenging the analog design especially when power consumption must match digital counterparts. The decrease of the supply voltage reduces the voltage headroom in analog circuits, the gate leakage current increases, the voltage gain decreases in planar bulk transistors, 1/f noise deteriorate when using new high-k gate dielectrics. The transistor and passive components mismatches give rise to large inaccuracies. Only some of these problems can be solved at the technology level; others require new circuit topologies and design techniques. The increased digital processing capability not only pushes the analog-digital interface toward more and more digital, thus limiting the analog design to very first interfaces and data converters, but also enables to use digital methods for the correction and digital assisted analog design. Several of the solutions currently proposed for analog pre-processing and data converter design are discussed in this paper.

Plenary Session P6- LHC Machine / 121

LHC machine RF issues and developments

Author: Andy BUTTERWORTH[None]

The main RF system of the LHC, which uses 400MHz superconducting cavities, will be used to capture, accelerate and store the injected beam. A separate transverse damper system using electrostatic deflectors will be used to damp transverse oscillations. The associated low-level RF (LLRF) equipment is responsible for fast control of the accelerating voltage and phase in the cavities, the phase and radial position of the beam, and the synchronization of beam transfers between SPS and LHC. The LLRF system combines high-frequency analogue components with digital signal processing using FPGAs and DSPs. The extensive use of digital technology allows not only to achieve the required performance and stability but also to provide full remote control and diagnostics facilities needed in a machine where most of the RF system is inaccessible during operation.

Plenary Session P5-LHC experiment electronic upgrades / 122

Upgrades introduction

Author: Geoff HALL[1]

[1] *Imperial College of London*

Plenary Session P5-LHC experiment electronic upgrades / **123**

TTC upgrade questions and discussion

Plenary Session P5-LHC experiment electronic upgrades / **124**

Optical links questions and discussion

Plenary Session P5-LHC experiment electronic upgrades / **125**

Power issues questions and discussion

Plenary Session P7-Beam, SLHC & closeout / **126**

Close OUT

Plenary Session P5-LHC experiment electronic upgrades / **127**

Informal comments on SLHC machine issues

Author: Andy BUTTERWORTH[None]

Plenary Session P5-LHC experiment electronic upgrades / **128**

The GBT Bi-directional Link and Data system

Author: Paulo MOREIRA[None]

Plenary Session P5-LHC experiment electronic upgrades / **129**

Future options for optical links

Author: Francois VASEY[1]

[1] *CERN*

Poster sessions / **130**

High-density backplanes –problems and solutions

Author: Sam Silverstein[1]

Co-author: C. Bohm [1]

[1] *Stockholm University*

The challenges of producing high-performance and low-latency realtime systems for LHC have led many groups to design systems with higher channel density and greater interconnectivity between modules. Custom backplanes with 2mm Hard Metric connectors provide the high pin counts necessary for these systems, but also present new problems, including increased insertion and extraction forces, vulnerable and easily damaged pins, and other long-term maintenance issues.

The ATLAS Level-1 calorimeter trigger processor presents a near "worst-case"example of such a system. The Jet/Et and em/hadron subsystems use a full-custom 21-slot 9U backplane fully populated with 2mm HM connectors with a total of 1148 signal and ground pins per module. In this paper we present our solutions for reducing insertion/extraction force, providing strain relief for hundreds of connected cables while maintaining accessibility, and maintaining and repairing the backplane over the lifetime of LHC.

Parallel Session A6-Optoelectronics Working Group / 131

SLHC Working Group

Author: Francois Vasey[1]

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