Low-noise Design Issues for Analog Front-end Electronics in 130 nm and 90 nm CMOS Technologies

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Abstract

Deep sub-micron CMOS technologies provide well-established solutions to the implementation of low-noise front-end electronics in various detector applications. The IC designers' effort is presently shifting to 130 nm CMOS technologies, or even to the next technology node, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. In this work the results of noise measurements carried out on CMOS devices in 130 nm and 90 nm commercial processes are presented. The behavior of the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width. The study is focused on low current density applications where devices are biased in weak or moderate inversion. Data obtained from the measurements provide a powerful tool to establish design criteria in nanoscale CMOS processes for detector front-ends in LHC upgrades.

I. Introduction

Deep sub-micron CMOS technology has met the challenging design requirements for front-end electronics in various High Energy Physics (HEP) detector applications. For instance, CMOS commercial technologies of the quarter micron node have been extensively used for the implementation of radiation tolerant, low noise, low power readout circuits with very high channel density for analog and digital processing in pixel and microstrip detectors at the Large Hadron Collider (LHC) experiments under construction at CERN [1-4]. The increased luminosity and track densities expected in the experiments at the next generation colliders (LHC upgrades, International Linear Collider, Super B-Factory) set the demand for moving to more scaled CMOS technologies [5-7]. Nowadays, CMOS processes with 130 nm minimum feature size are widely available for Application Specific Integrated Circuits (ASICs) design, and 90 nm processes are coming on-line as the next industrial generation; therefore, the IC designers' effort is presently shifting to these technology nodes to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. At nanoscale geometries, below 100 nm feature sizes, modeling the behavior of the analog parameters of these devices is a tricky problem, since some effects which can deeply affect short channel MOSFET performance, become more difficult to foresee. This work presents the results relevant to the noise characterization of single CMOS devices belonging to two commercial CMOS processes with minimum feature size of 130 nm and 90 nm manufactured by STMicroelectronics. The devices were characterized at drain currents from several tens of μA to 1 mA, that is, the usual operating currents of input devices in integrated charge-sensitive amplifiers. In these conditions, deep sub-micron devices are biased in weak or moderate inversion. The behavior of the main noise parameters modelling the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width to account for different detector requirements. The wide set of measurements provides a powerful tool to establish design criteria in 130 nm and 90 nm CMOS processes. The analysis of the experimental results also includes the comparison of noise parameters obtained from the two technology generations. This is expected to provide useful hints for the choice of the proper CMOS node to be used for detector front-end electronics in view of future applications in the field of HEP electronic instrumentation such as LHC upgrades.

II. Experimental Details

A. Investigated Devices

The MOSFETs studied in this paper belong to two commercial CMOS processes with 130 nm and 90 nm minimum feature size manufactured by STMicroelectronics. The maximum allowed supply voltage V_{DD} is +1.2 V for devices in the 130 nm process and +1.0 V for devices in the 90 nm process. The physical thickness of the gate oxide t_{OX} is 2.0 nm, and 1.6 nm respectively; for devices in inversion the electrical gate oxide thickness can be estimated to be 2.4 nm and 2.0 nm [8], therefore, the corresponding effective gate capacitance per unit area C_{OX}, is about 15 fF/μm^2 and 18 fF/μm^2. In the 130 nm process PMOS and NMOS devices with gate length L of 0.13, 0.2, 0.35, 0.5, 0.7 and 1 μm, and gate width W of 200, 600 and 1000 μm were investigated. In the 90 nm process we studied devices of both polarities with gate length of 0.1, 0.13, 0.2, 0.35, 0.5 and 0.7 μm, and gate width of 200 and 600 μm. Devices with such a large W are commonly used as front-end elements in readout systems for particle detectors, in order to achieve the best noise performances [9]. In both processes all NMOS devices were laid out using a standard open structure, interdigitated configuration.

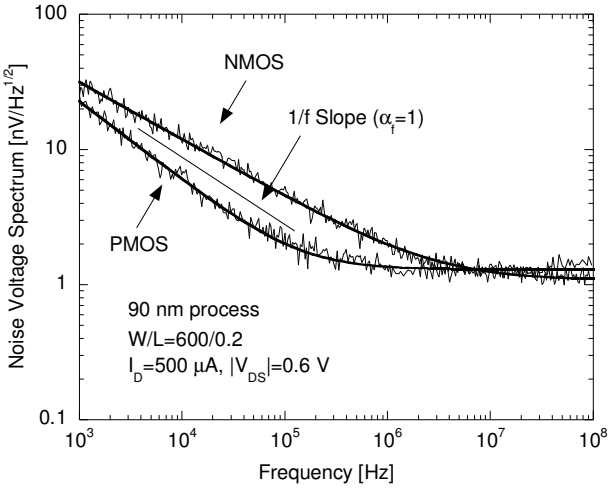

Figure 1: Gate referred noise voltage spectra for NMOS and PMOS devices with *W/L*=600/0.2 belonging to the 90 nm process (I_D=500 µA, $|V_{DS}|$=0.6 V).

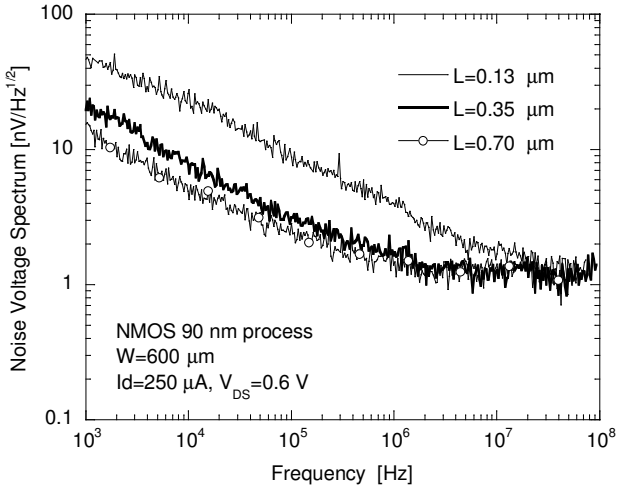

Figure 2: Noise voltage spectra of NMOS with gate width *W*=600 µm and different gate length *L* belonging to the 90 nm process (I_D=250 µA, V_{DS}=0.6 V).

B. Measurement setup

Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. The spectral density of the noise in the channel current of the examined devices was measured using instrumentation purposely developed at the Electronic Instrumentation Laboratory, University of Pavia. The noise of the DUT is amplified by a wideband interface circuit and detected by a Network/Spectrum Analyzer HP4195A [10]. This system allows for noise measurements in the 100 Hz–100 MHz range.

III. NOISE MODEL AND PARAMETERS

In a MOSFET, the noise in the channel current can be expressed by an equivalent noise voltage generator referred to the gate of the device. A rather general expression for the power spectral density of the voltage noise is expressed by means of equation (1) where the first term is determined by channel thermal noise and noise contributions from parasitic source/drain, gate and bulk resistors while the second term is given by 1/f noise in the channel current [11].

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f) \tag{1}$$

In the low current density operating region, the white noise voltage spectrum S_w^2 is dominated by channel thermal noise and can be expressed by means of its equivalent noise resistance:

$$R_{eq} = \frac{S_W^2}{4k_B T} = \alpha_W \frac{n\gamma}{g_m} \tag{2}$$

were k_B is the Boltzmann's constant, T is the absolute temperature, g_m is the device transconductance, n is a coefficient proportional to the inverse of the subthreshold slope of I_D as a function of V_{GS}, γ is a coefficient ranging from 1/2 in weak inversion to 2/3 in strong inversion and $\alpha_W \geq 1$ is an excess noise factor [12]. The 1/f noise in the channel current can be modeled by the relationship:

$$S_{1/f}^2(f) = \frac{K_f}{C_i} \frac{1}{f^{\alpha_f}}. \tag{3}$$

K_f is an intrinsic process parameter for 1/f noise and $C_i = C_{OX}WL$ is the gate oxide capacitance, whose value depends on the size of the MOSFET. The exponent α_f determines the slope of this low frequency noise term and its value is usually between 0.8 and 1.2. According to equations (2) and (3) the noise parameters α_W, γ, K_f and α_f, together with static and signal parameters n and g_m, fully characterize the noise performance of MOS transistors.

IV. NOISE MEASUREMENT RESULTS

Noise voltage spectra were measured for PMOS and NMOS with different gate widths and lengths belonging to both the investigated technologies. Fig. 1 to Fig. 5 are a typical set of experimental results concerning devices in the 90 nm process. For the devices in the 130 nm process, noise measurement results can be found in [13], while the effects of ionizing radiation on the noise properties are studied in [14]. The device parameters were characterized at drain currents I_D below 1 mA, as dictated by power dissipation constraints in high density monolithic front-end systems. In these conditions nanoscale devices are biased in weak or moderate inversion. Fig. 1 compares the noise voltage spectra of a PMOS and an NMOS with the same gate dimensions. The devices are biased at I_D=1 mA, that is in the moderate inversion region, where the NMOS has a larger transconductance with respect to the PMOS. This results in a smaller channel thermal noise for the NMOS, as it appears in the high frequency part of the spectra. The PMOS retains an advantage on the NMOS in terms of 1/f noise, which dominates the low frequency portion of the spectra. Figs. 2 and 3 show noise voltage spectra relevant to NMOS and PMOS devices with *W*=600 µm and different gate lengths *L*, biased at the same drain current. The devices are close to weak inversion, therefore, white noise should not be sizably affected by *L* variations. At low frequencies, 1/f noise

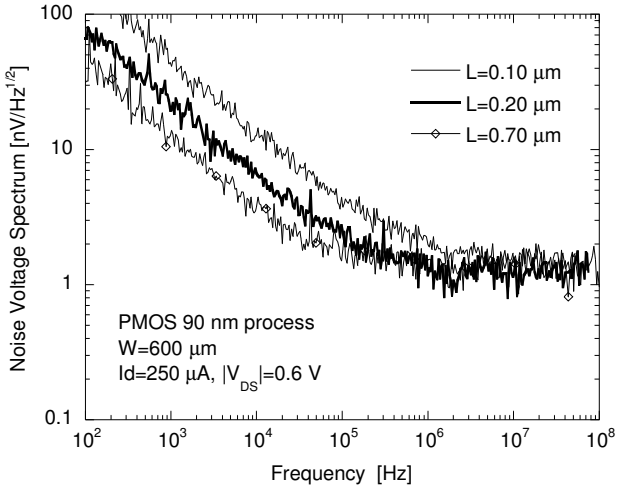

Figure 3: Noise voltage spectra of PMOS with gate width W=600 µm and different gate length L belonging to the 90 nm process (I_D=250 µA, $|V_{DS}|$=0.6 V).

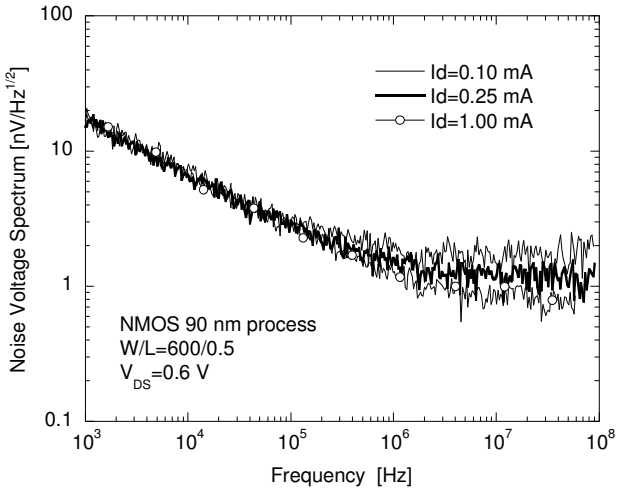

Figure 4: Noise voltage spectra of an NMOS with W/L=600/0.5 belonging to the 90 nm process at different values of drain current I_D (V_{DS}=0.6 V).

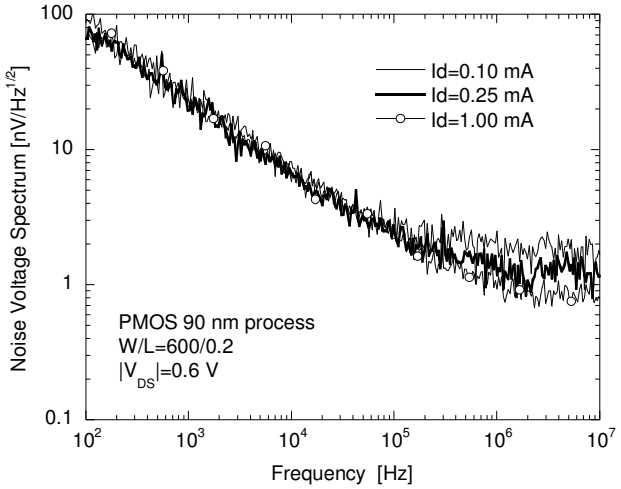

Figure 5: Noise voltage spectra of a PMOS with W/L=600/0.2 belonging to the 90 nm process at different values of drain current I_D ($|V_{DS}|$=0.6 V).

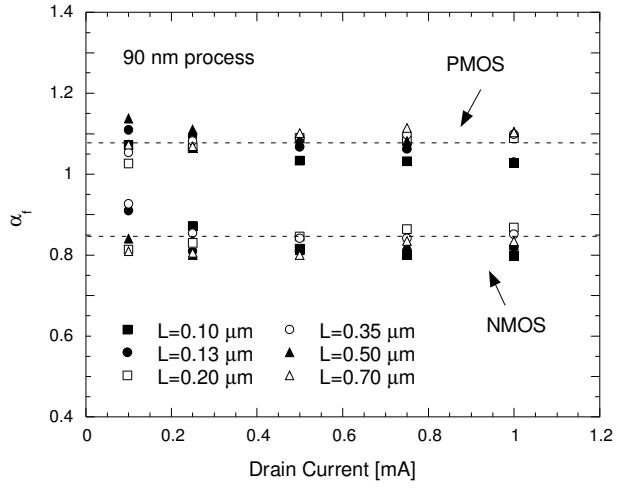

Figure 6: Slope of the 1/f noise term as a function of the drain current I_D for NMOS and PMOS devices with W=600 µm belonging to the 90 nm process ($|V_{DS}|$=0.6 V).

increases with decreasing L. According to (3), this is due to the reduction in the input capacitance C_i. Figs. 4 and 5 show the effect of the drain current I_D on the noise voltage of an NMOS and a PMOS. Channel thermal noise is reduced by increasing I_D in agreement with (2), since the transconductance correspondingly increases. As far as the 1/f noise component is concerned, it is not affected by I_D variations for NMOS devices while a slight increase with the drain current is detected for PMOS devices. In the following the behavior of the 1/f and white noise parameters is studied as a function of the device polarity and of the gate length and width to account for different detector requirements at different drain currents. A comparison of parameters concerning the two investigated technologies is also shown.

A. 1/f noise parameters K_f *and* α_f

In Fig. 1 it can be observed that the slope of the 1/f noise component of the spectrum α_f is not equal to 1. The analysis of the experimental results shows that α_f is consistently smaller than 1 in NMOSFETs and larger than 1 in PMOSFETs. This behavior was detected in other deep submicron processes [15,16] and could be related to a different profile of oxide traps interacting with carriers of different polarity. Typical values of α_f obtained for devices of both polarities in the two investigated processes are reported in table 1 together with the spread across samples with different gate dimensions and tested in different bias conditions. From the measured noise voltage spectra it has been found that 1/f noise parameter α_f does not exhibit any clear dependence on the channel length L nor on the drain current I_D as shown in Fig. 6. Fig. 7 shows the behavior of the

Table 1: Slope coefficient of the low frequency noise term.

	α_f	
Process	130 nm	90 nm
NMOS	0.85±0.05	0.85±0.05
PMOS	1.19±0.05	1.09±0.05

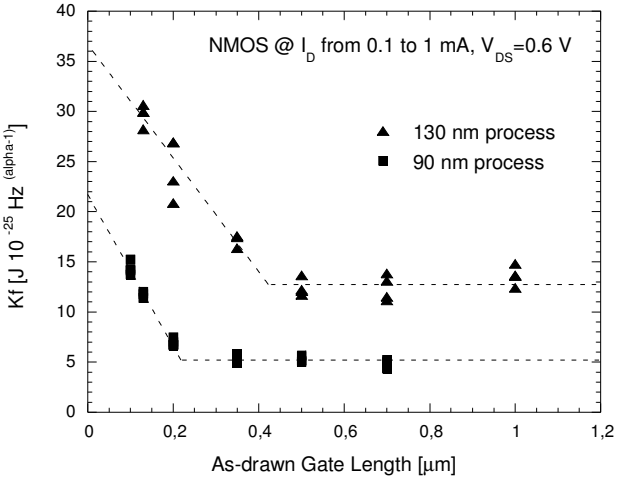

Figure 7: 1/f noise coefficient K_f as a function of the gate length L for NMOS belonging to the 130 nm and 90 nm processes (V_{DS}=0.6 V).

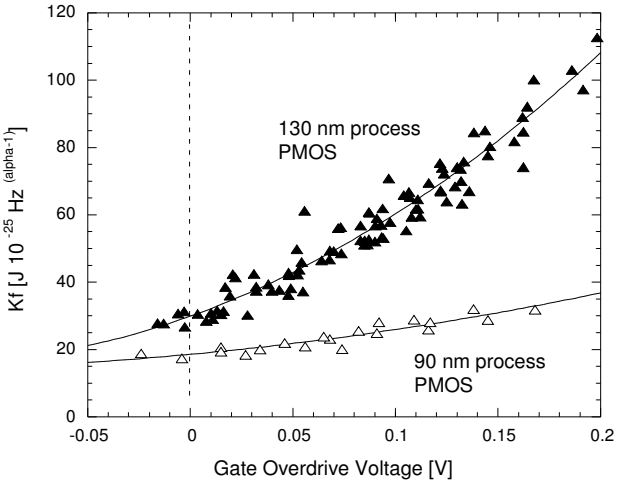

Figure 8: 1/f noise coefficient K_f as a function of the overdrive voltage for PMOS belonging to the 130 nm and 90 nm processes ($|V_{DS}|$=0.6 V).

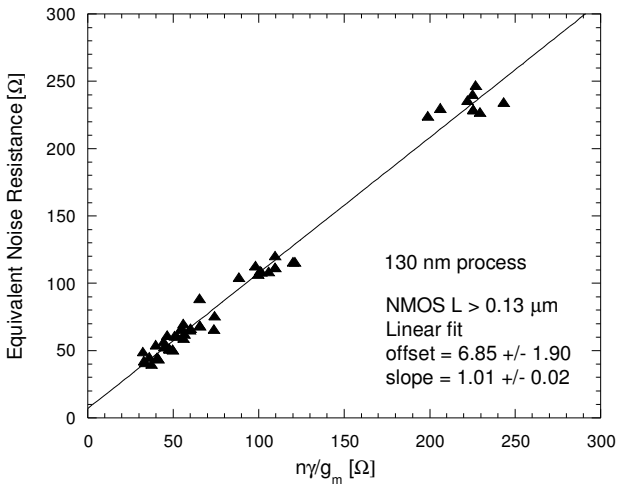

Figure 9: Equivalent channel thermal noise resistance R_{eq} for NMOS devices belonging to the 130 nm process (V_{DS}=0.6 V).

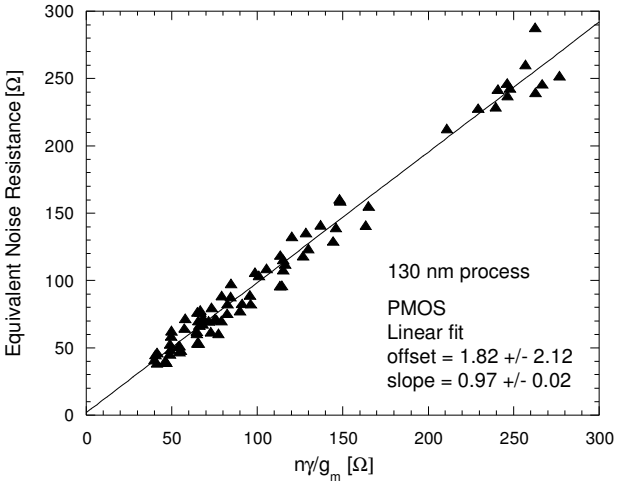

Figure 10: Equivalent channel thermal noise resistance R_{eq} for PMOS devices belonging to the 130 nm process ($|V_{DS}|$=0.6 V).

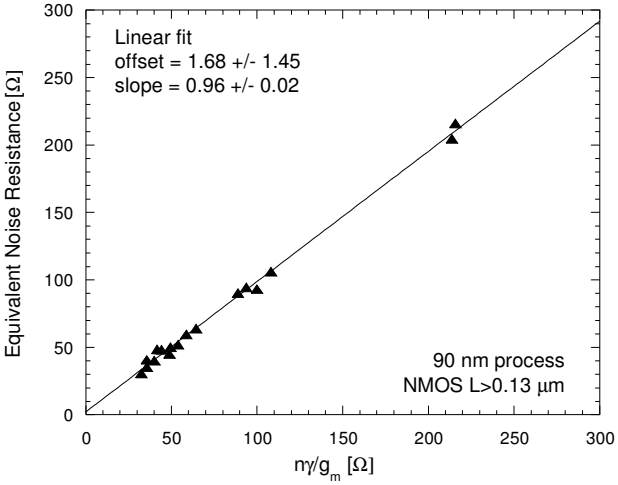

Figure 11: Equivalent channel thermal noise resistance R_{eq} for NMOS devices belonging to the 90 nm process (V_{DS}=0.6 V).

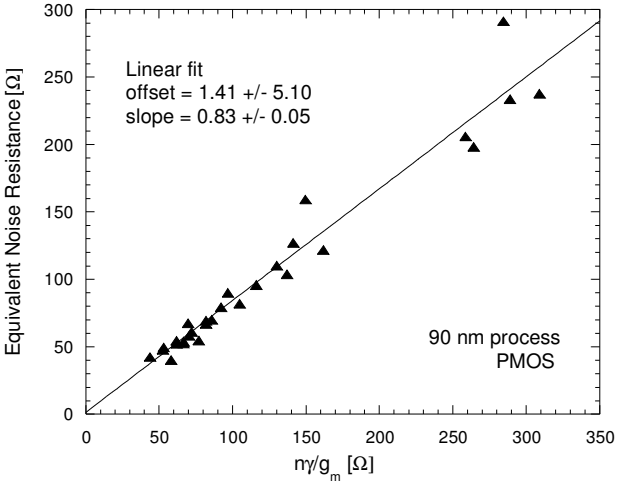

Figure 12: Equivalent channel thermal noise resistance R_{eq} for PMOS devices belonging to the 90 nm process ($|V_{DS}|$=0.6 V).

1/f noise coefficient K_f for NMOS devices as a function of the channel length. In both processes the 1/f noise coefficient K_f is larger for devices with channel length close to the minimum allowed by the technology and is lower in the 90 nm process with respect to 130 nm process. Moreover it is independent of the drain current in the NMOS. Measurements on PMOS devices show an increase of K_f both with the channel length L and the drain current I_D. According to [16,17] this behavior is due to the origin of flicker noise that, in p-channel devices, is often attributed to mobility fluctuations, and shows an increase of K_f with the overdrive voltage. In Fig. 8 values of K_f obtained for devices with different gate geometry and bias condition are reported as a function of $(V_{GS}-V_T)$. According to this plot K_f is larger for devices in the 130 nm process and its bias dependence is weaker in 90 nm technology.

B. White noise parameters α_W and γ

White noise is evaluated in terms of the equivalent channel thermal noise resistance R_{eq}. Figs. 9 and 10 show values of R_{eq} as a function of $n\gamma/g_m$ obtained for NMOS and PMOS devices belonging to the 130 nm process. According to equation (2) the slope of the linear fit is determined by the coefficient α_W while the offset is due to contributions from parasitic resistance. Values of α_W close to unity were found for all devices except for NMOS with the minimum feature size allowed by the technology. This means that there are no sizeable short channel effects in the considered operating regions. Negligible contributions were found from parasitic resistance. Same results were obtained for 90 nm process devices as shown in Figs. 11 and 12. In this case no data are available for channel thermal noise in NMOS devices with $L \leq 0.13$ μm.

V. CONCLUSIONS

The paper presents noise measurement results concerning devices belonging to two different CMOS technology nodes, namely the 130 nm and the 90 nm STM processes. The analysis of the experimental results show that channel thermal noise equations developed to describe the device behavior in the considered operating regions provide a reliable model, with short channel effect playing a minor role in both the considered processes. 1/f noise results confirm the behavior detected in previous submicron processes as far as the dependence on device polarity and bias and gate geometry is concerned. Extracted noise parameters show that using the 90 nm process may ensure an improvement in the noise performances in applications where large signal dynamic range is not needed while miniaturization can be an asset.

VI. REFERENCES

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