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Low-noise design issues for analog front-end electronics in 130 nm and 90 nm CMOS technologies

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Deep sub-micron CMOS technologies are widely used for the implementation of front-end electronics in various detector applications. The IC designers'effort is presently shifting to 130 nm CMOS technologies, or even to the next technology node, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. In this work the results of signal and noise measurements carried out on CMOS devices in 130 nm and 90 nm commercial processes are presented. Data obtained from the measurements provide a powerful tool to establish design criteria in nanoscale CMOS processes for detector front-ends in LHC upgrades.

Summary

Deep sub-micron CMOS technology has met the challenging design requirements for front-end electronics in various High Energy Physics (HEP) detector applications. For instance, CMOS commercial technologies of the quarter micron node have been extensively used for the implementation of radiation tolerant, low noise, low power readout circuits with very high channel density for analog and digital processing in pixel and microstrip detectors at the Large Hadron Collider (LHC) experiments under construction at CERN. The increased luminosity and track densities expected in the experiments at the next generation colliders (LHC upgrades, International Linear Collider, Super B-Factory) set the demand for moving to more scaled CMOS technologies. Nowadays, CMOS processes with 130 nm minimum feature size are widely available for Application Specific Integrated Circuits (ASICs) design, and 90 nm processes are coming on-line as the next industrial generation; therefore, the IC designers'effort is presently shifting to these technology nodes to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. At nanoscale geometries, below 100 nm feature sizes, modeling the behavior of analog parameters of these devices is a tricky problem, since some effects which can deeply affect the MOSFET performance, such as short channel effects, already observed in previous generations of technology, become more difficult to overcome; therefore, these advanced processes require a thorough evaluation of the impact of technology scaling on the main device analog parameters. This work presents the results relevant to the signal and noise characterization of single CMOS devices belonging to two commercial CMOS processes with minimum feature size of 130 nm and 90 nm manufactured by STMicroelectronics. The devices were characterized at drain currents from several tens of uA to 1 mA, that is, the usual operating currents of input devices in integrated charge-sensitive preamplifiers. In these conditions, deep sub-micron devices are biased in weak or moderate inversion. The behavior of the main signal parameters and of the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width to account for different detector requirements. The wide set of measurements provide a powerful tool to establish design criteria in 130 nm and 90 nm CMOS process. The analysis of the experimental results also includes the comparison of signal and noise parameters obtained from the two technology nodes in order to convey useful hints for the choice of the proper technology node to be used for detector front-end electronics in view of future applications in the field of HEP electronics instrumentation such as LHC upgrades.

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