Design and test of the final ALICE SDD CARLOS end ladder board

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Abstract

The paper presents the design and test of the final prototype of the CARLOS (Compression And Run Length Encoding Subsystem) end ladder board that is going to be used in the ALICE experiment at CERN. This board is able to compress data coming from one Silicon Drift Detector (SDD) front-end electronics and to send them towards the data concentrator card CARLOSrx in counting room via a 800 Mb/s optical link. The board design faces several constraints, mainly size (54x49 mm) and radiation tolerance: for this reason the board contains several CERN developed ASICs. A test setup has been realized for selecting the good devices among the 500 cards already produced.

I. Introduction

The Inner Tracking System (ITS) [1] of the ALICE experiment contains six coaxial cylindrical layers. Layers 3 contains 14 ladders each one hosting 6 SDDs, while layer 4 contains 22 ladders each one hosting 8 SDDs. The CARLOS end ladder board is placed on both sides of each ladder with the purpose of acquiring and compressing data coming from each SDD before sending them towards the data concentrator card CARLOSrx in counting room through optical fibers. The board contains the compression chip CARLOS [2] that performs a bi-dimensional compression of the data coming from the SDD front-end electronics. CARLOS 16-bit output bus is encoded with 8B/10B Ethernet protocol and sent to a single mode optical fiber using a 1310 nm optical laser with a total data throughput of 800 Mb/s.

II. Final CARLOS End Ladder Board

Figure 1a and Figure 1b show the layout of the components' positions on the final CARLOS end ladder card. Looking at Figure 1a from the top-right corner the 1310 nm edge-emitting laser diode is shown. This component transmits the compressed and packed dataset to the CARLOSrx board, at a rate of 800 Mb/s. Below the laser, two pin-diodes (FT1 and FT2) receive the clock and the serial signals. The latter signal provides the system configuration at start-up and may stop the acquisition in event of channel congestion. The 2 pin-diodes and the laser are single-mode 1310 nm (wavelength) pig-tailed modules. These modules are interfaced with the commercial transceivers (Optoway SPS-7110) on the CARLOSrx card via optical adaptors. In more detail, the

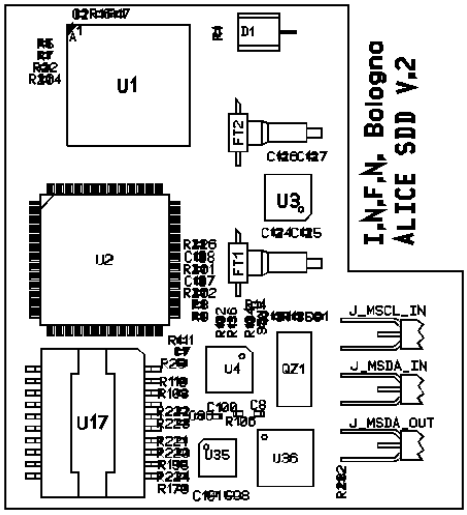

Figure 1a: CARLOS end ladder card layout top view.

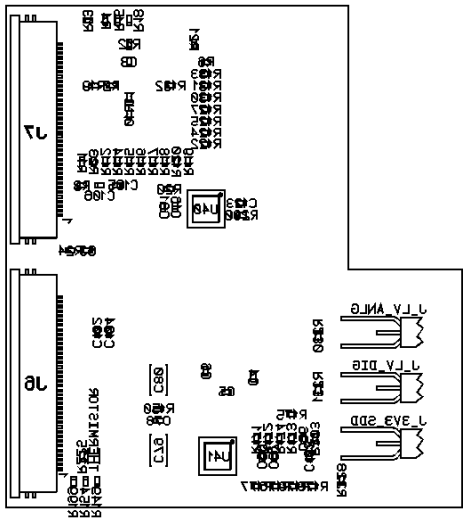

Figure 1b: CARLOS end ladder card layout bottom view.

signals received on the pin-diode interface with the other components through the 2-channel receiver chip RX40.

Let us now describe the system data-flow. The dataset that originates from the Front End Electronics (FEE) enters the

card through the Molex connectors and is read by the CARLOS chip. This performs basically a bi-dimensional compression [3], [4] during the normal DAQ mode and works as a system JTAG switch during the FEE configuration. CARLOS reduces and packs the dataset and its outputs are serialized via the Gigabit Optical Link (GOL) serializer chip that interfaces, by means of an 800Mb/s link [5], with the laser diode. Finally, the GOL chip serializes the dataset that is reconstructed within the Counting Room Emulator by a mirroring de-serializer device that outputs the data to the state analyzer instruments. As the GOL chip requires a low-jitter clock signal, as low as 50 ps peak-to-peak, the QPLL clock filter chip has been applied. This locks the 40.08 MHz clock signal, derived from one of the two pin-diodes, on a very-low-jitter 160.3 MHz crystal (QZ1). Then this frequency is divided by 4 and passed to the GOL and CARLOS chips. The low-right corner of the Figure 1a shows the layout for the 3 twisted pairs of the I2C bus that it is used for monitoring some embedded parameters, such as supply voltage, temperature and current on the front-end and CARLOS end ladder boards. The bus is remotely controlled by the Detector Control System (DCS) card that interfaces the DILBERT and DCU chips on the CARLOS end ladder board. This control bus (I2C) allows to reset the DCU, to inhibit the power-supply for FEE and to power-cycle the GOL chip. The power-cycle feature is achieved by using the CRT4T [6] [7], a CMOS power switching chip developed by the CERN Microelectronics Group.

Three twisted pairs (in the bottom side of the card, see Figure 1b) are used for implementing the fine voltage regulation for the FEE and CARLOS end ladder. The chips are powered with a 2.5 V low voltage regulator (LHC4913) that is configured for an overall current of 1 A. All the components embedded into the final CARLOS end ladder board are Application Specific Integrated Circuits (ASICs) designed to be radiation-tolerant to the total ionizing dose that is estimated (nearly 30 krads) for a 10-years of data-taking within the ALICE ITS environment

III. CARLOS End Ladder System Test

The CARLOS end ladder board as a whole is qualified using two different test setups. The first setup is used to verify the behaviour of the CARLOS end ladder board together with the electronics developed for the ALICE-SDD experiments.

The second is a Bit Error Rate Test (BERT) system, which is used to measure an upper limit on the BER, when the CARLOS end ladder board is operated under ideal laboratory conditions.

A. Experimental Results

The card was tested using the test setup shown in Figure 2. The SDD module contains the FEE that generate the 16 bit data streams at 40 MHz to be fed to the CARLOS end ladder board.

The data are processed by the card and sent via optical link to the receiver board that interfaces the ALICE Detector Data Link (DDL) [8]. In this way it is possible to

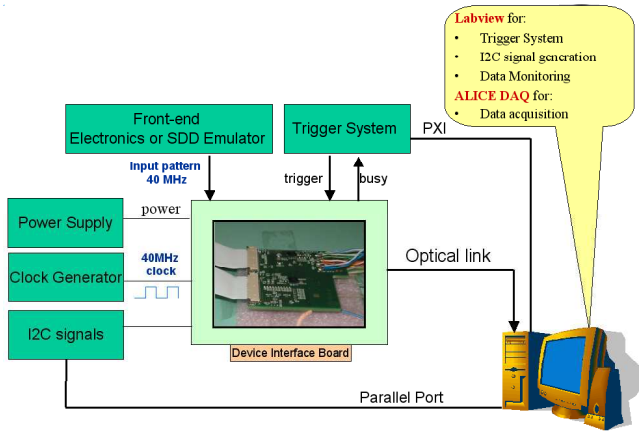

Figure 2: Test setup for CARLOS end ladder board.

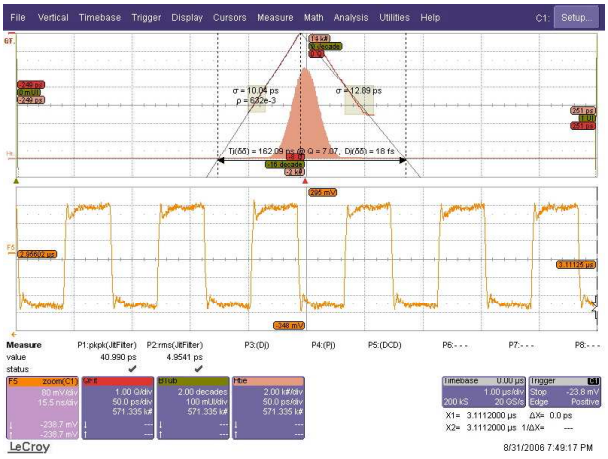

Figure 3: QPLL jitter filtering results.

store and monitor the data processed by the CARLOS end ladder card looking for errors in the structure of the data. A Labview program controls the instrumentation used to generate the trigger and I2C signals that are used to start the acquisition and monitoring of the control parameters (i.e. temperature, voltage and current) and digital lines (i.e. power to GOL) for the CARLOS end ladder board and the FEE. This setup has confirmed the validity of the architecture implemented in the CARLOS end ladder board.

Figure 3 shows the measurements for the CARLOS end ladder board hosting the QPLL circuit. Since the output clock jitter is less than 50 ps peak-to-peak and is less than 10 ps RMS when the input jitter less than 120 ps RMS, this confirms the achievements of the design goals.

The CARLOS end ladder board delivers a clean eye diagram when driven with a bias current of 16 mA at 800 Mb/s, as shown in Figure 4. At this current, the optical power output from the MU connector is approximately –5 dBm.

Figure 5 shows the bathtub plot for the transmission of data via optical link, the horizontal axis is the unit interval (UI) of 1.25 ns and the logarithmic vertical axis is BER. The estimated BER from the signal-to-noise ratio of the eye diagram is less 10^{-16} with a 70% open eye. This diagram

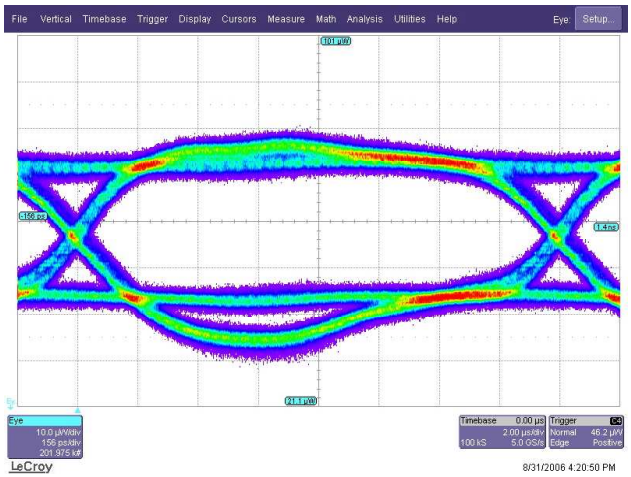

Figure 4: Eye diagram at 800 Mbits/s.

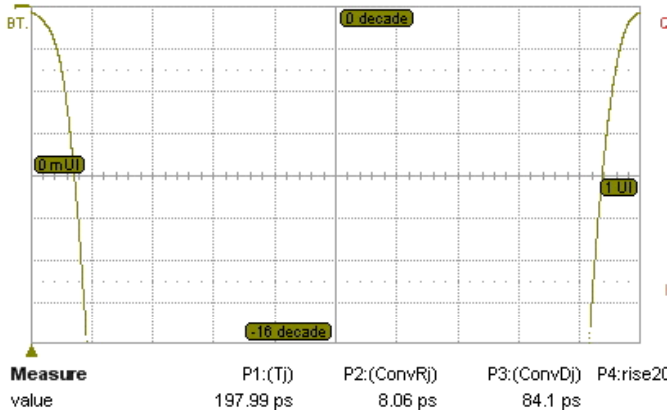

Figure 5: Bathtub curve.

shows the quality of the optical link and the quality of the filtered clock.

B. BERT System

The BERT is a custom-built system based on a SDD emulator FPGA board, CARLOS end ladder board and BERT card. It is illustrated in Figure 6. The SDD emulator is a special card developed by Bologna group that emulates the signals coming from the FEE, with the difference that it is possible to send a specific data pattern to the CARLOS end ladder board. Xilinx FPGA's on the SDD emulator (XC2V1000) and BERT (XC2VP7) cards generate data input to the CARLOS end ladder board and read output form the deserializer (TLK1501), respectively.

The firmware implemented in the BERT card compares bit-by-bit the expected data with the acquired data and if a mismatch is found the firmware increases the error count and the position in the pattern for future analysis. In this way the BERT card compares the bits at the same speed of the acquisition (640 Mb/s).

Using the BERT system the bit error rate has been measured to be less than 10^{-14}, comparable to the estimated BER from the signal-to-noise ratio of the eye diagram.

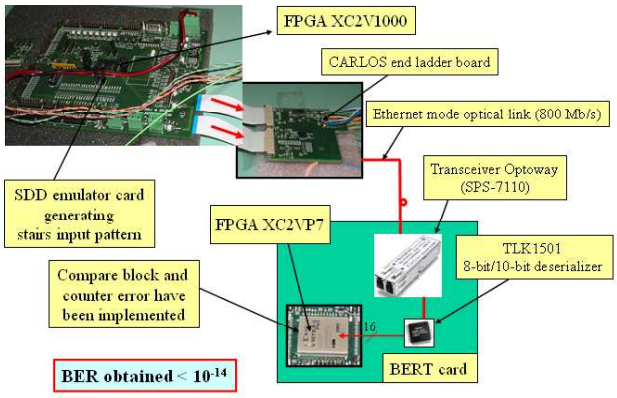

Figure 6: Bit Error Rate Test (BERT) system setup.

IV. Integration With The FEE

The CARLOS end ladder board has been tested and assembled in the ladder structure with the final FEE, readout and power supply electronics. In Figure 7 the CARLOS end ladder boards placed on the end side of the ladder are shown. No errors were attributed to the CARLOS end ladder board during these tests.

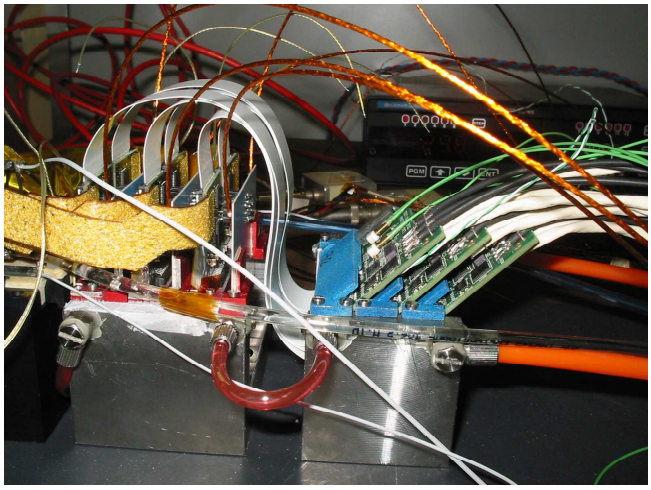

Figure 7: CARLOS end ladder boards assembled in the ladder structure.

V. Conclusions

The CARLOS end ladder board fulfils the requirements on space (54x49 mm with a maximum thickness of 16 mm) and on construction materials for its final use in the ALICE experiment. The board has been tested using the complete setup from the front-end electronics to the data concentrator card CARLOSrx: the test of the board was successful both for what concerns data transmission and DCS features. Beside that an FPGA based board has been developed as an emulator of the front-end boards with the purpose of generating known patterns after receiving a trigger signal: this allowed us to obtain the measure of the optical link Bit Error Rate (BER) lower than 10^{-14}. It has clean eye diagram, low bit error rate

and low clock jitter. Up to now 500 boards have been produced and the test of the production is being carried out.

Beside that, the installation of 260 CARLOS end ladder board has started.

VI. Reference

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