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Design and test of the final ALICE SDD CARLOS end ladder board

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The paper presents the design and test of the final prototype of the CARLOS end ladder board. This board is able to compress data coming from one Silicon Drift Detector (SDD) front-end electronics and to send them towards the data concentrator card CARLOSrx in counting room via a 800 MBit/s optical link. The board design faces several constraints, mainly size (54x49 mm) and radiation tolerance: for this reason the board contains several CERN developed ASICs. A test setup has been realized for selecting the good devices among the 500 cards already produced.

Summary

The Inner Tracking System (ITS) of the ALICE experiment contains six coaxial cylindrical layers. Layers 3 contains 14 ladders each one hosting 6 SDDs (Silicon Drift Detectors), while layer 4 contains 22 ladders each one hosting 8 SDDs. The CARLOS end ladder board is placed on both sides of each ladder with the purpose of acquiring and compressing data coming from each SDD before sending them towards the data concentrator card CARLOSrx in counting room through optical fibers. The board contains the compression chip CARLOS that performs a bi-dimensional compression of the data coming from the SDD front-end electronics. CARLOS 16-bit output bus is encoded with 8B/10B Ethernet protocol and sent to a 800 MBit/s single mode optical fiber using a 1310 nm optical laser.
The CARLOS end ladder board receives the trigger signals and the configuration parameters through a 40 MBit/s serial signal coming from CARLOSrx through an optical fiber and converted using a photodiode.
An other photodiode is used for receiving the 40.08 MHz clock coming from the TTC system. The QPLL ASIC on the end ladder board allows to obtain a clock with a peak-to-peak jitter lower than 50 ps that is used both for the serializer (ASIC GOL) of the board and for the front-end electronics.
A special control unit has been developed with the purpose of monitoring parameters such as voltage, current and temperature related to the whole readout chain. The control unit is remotely controlled from the DCS (Detector Control System) board through the I2C bus. The CARLOS end ladder board also provides power for the analog and digital voltages of the front-end boards under the control of the DCS system.
The board has been tested using the complete setup from the front-end electronics to the data concentrator card CARLOSrx: the test of the board was successful both for what concerns data transmission and DCS features. Beside that an FPGA based board has been developed as an emulator of the front-end boards with the purpose of generating known patterns after receiving a trigger signal: this allowed us to obtain an estimation of the optical link Bit Error Rate (BER) lower than 10-16.
The CARLOS end ladder board fulfils the requirements on space (54x49 mm with a maximum thickness of 16 mm) and on construction materials for its final use in the ALICE experiment. Up to now 500 boards have been produced and the test of the production is being carried out.

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