The Hardware of the ATLAS Pixel Detector Control System

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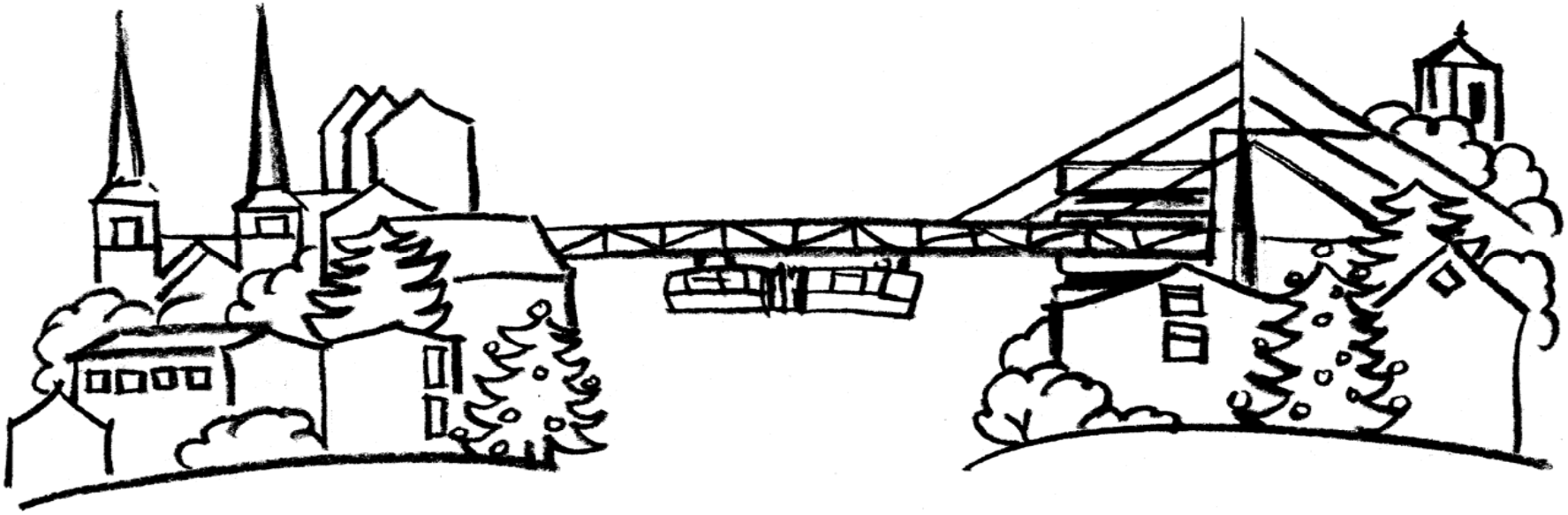

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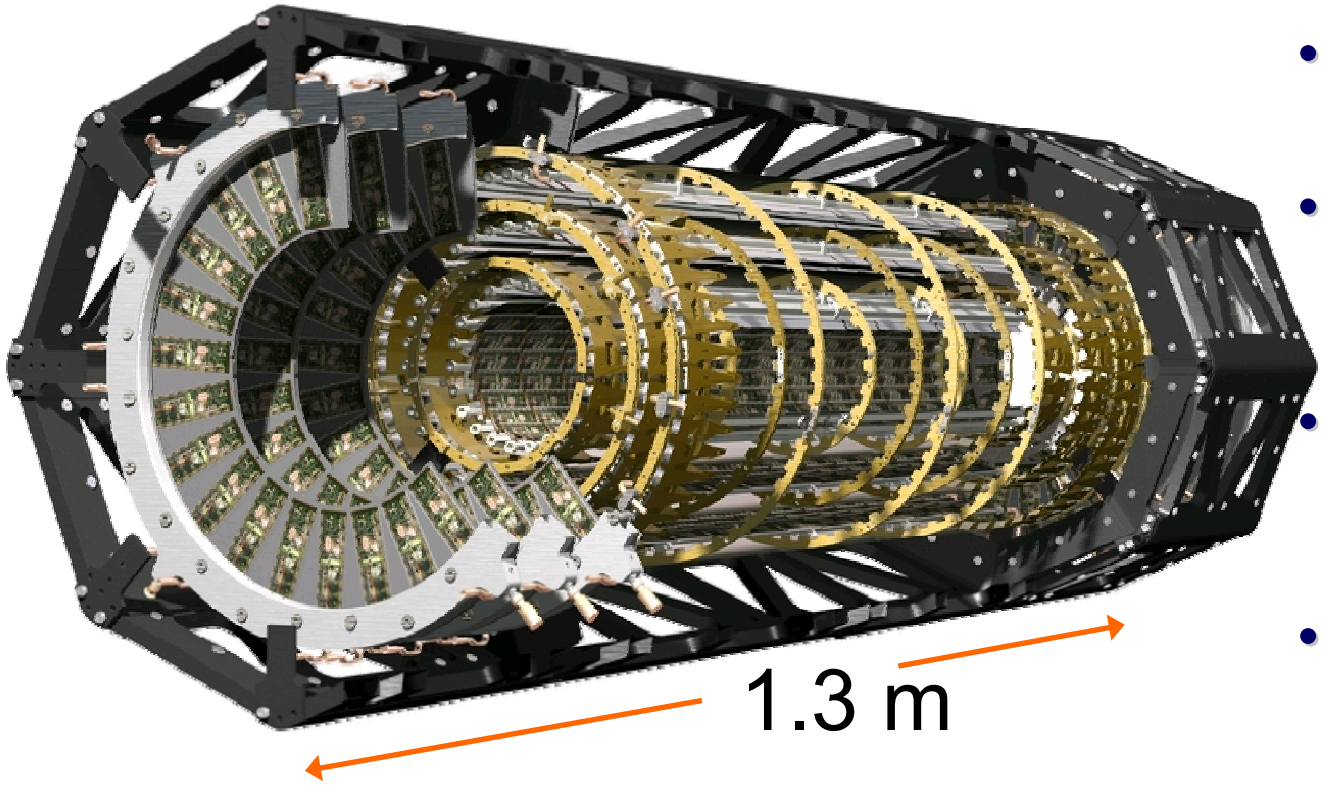
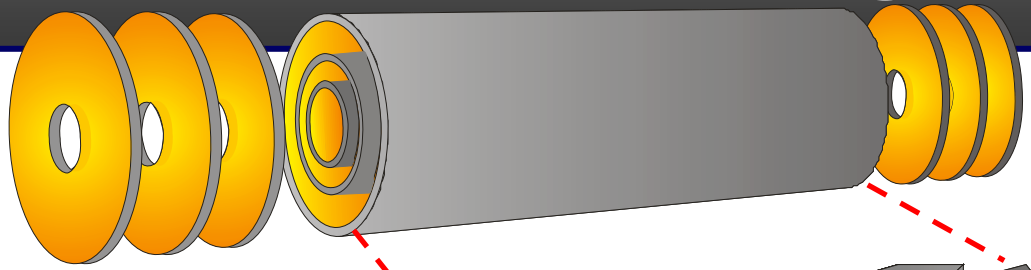
The Pixel Detector



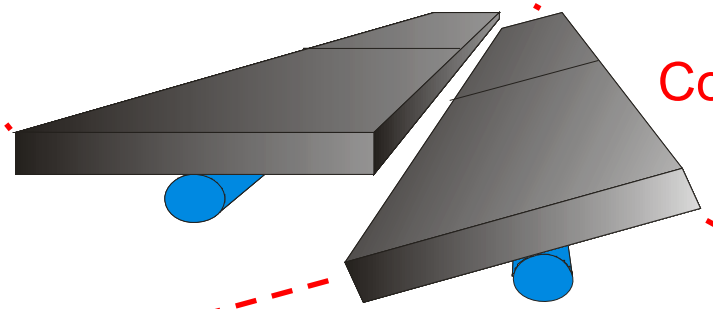
- 1744 modules
- 3 layers with r = 5, 9, 12 cm
- 3 space points for |η|<2.5
- 80 million Pixels (~90% ATLAS)
- main task: vertex-reconstruction

- ~6,5 kW
- -7°C operation temperature
- evaporative C_3F_8 cooling system

Pixel Detector Geography



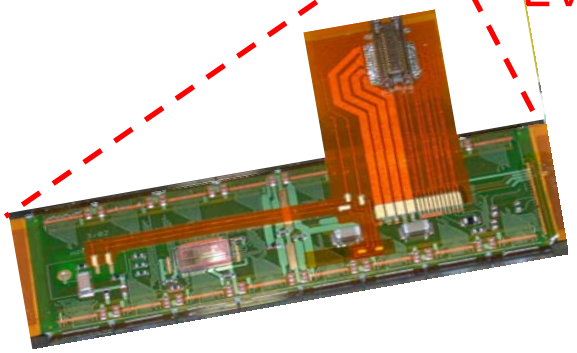
- Disc
- BLayer
- Layer1
- Layer2
  - max. 26 parallel cooling circuits (PCCs) per layer



Cooling (-7 °C)

LV (< 12 V), SC-OLink

- 4 half-staves / 2 sectors per PCC



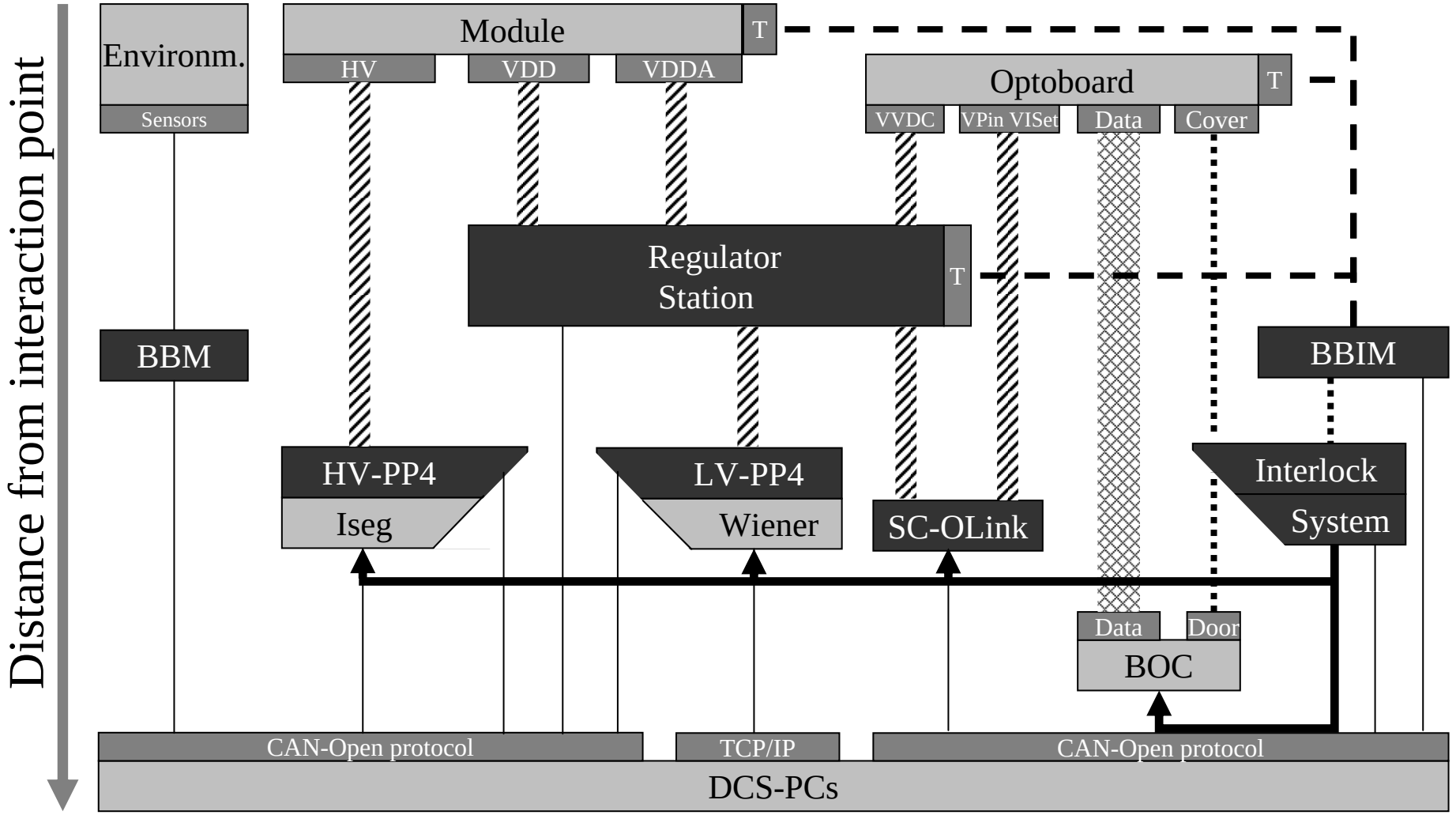
HV (< 700 V)
VDD (~1.7 V)
VDDA (~2.1 V)
Temperature

- 6 / 7 modules per half-stave

Hardware Requirements

- high power density (~6.5 kW)
  - thermal interlock
- radiation
  - radiation hard / tolerant devices
  - enable for long distance powering (LV -> regulators)
- granularity
  - costs for power supplies
  - high availability
- optical link
  - laser interlock
  - supply and control
- low cost / manpower
  - common parts (ATLAS ELMB)
  - common interfaces (CAN, TCP/IP)
- grounding sceme
  - floating
  - prevention of transients
  - use of opto-couplers or transformers

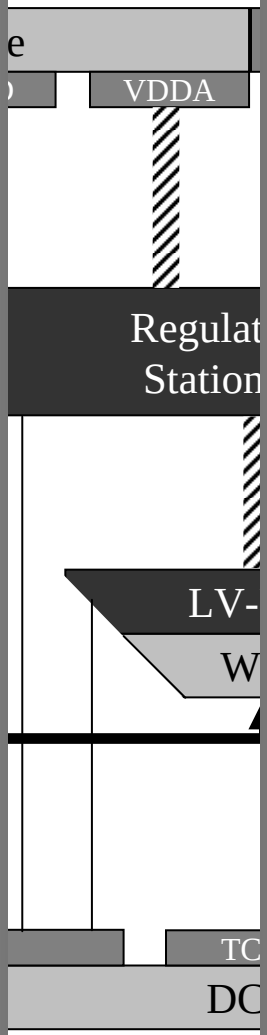
The DCS Hardware



Low Voltage

LV-PP4:

- mapping of regulator boards to PS channels
- uses ELMB
- current measurement of plus lines:
  - 2- 10 mA tested precision
  - 0 V to 2 V range
  - opto-decoupled
- current measurement on return lines can be added for selected boards



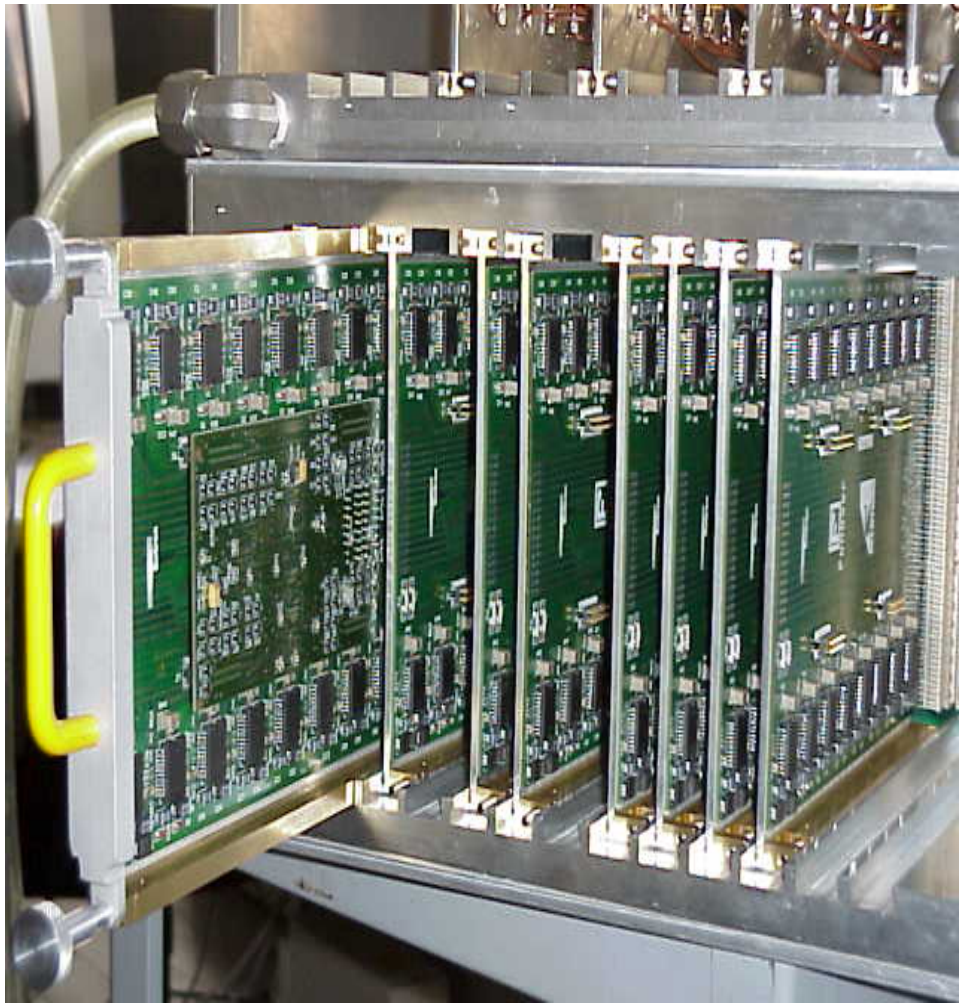
Wiener LV supply:

- LV for the modules VDD and VDDA
- 12 channel power supply
- max 12 V / 11.5 A
- floating
- protections:
  - over-voltage, over-current

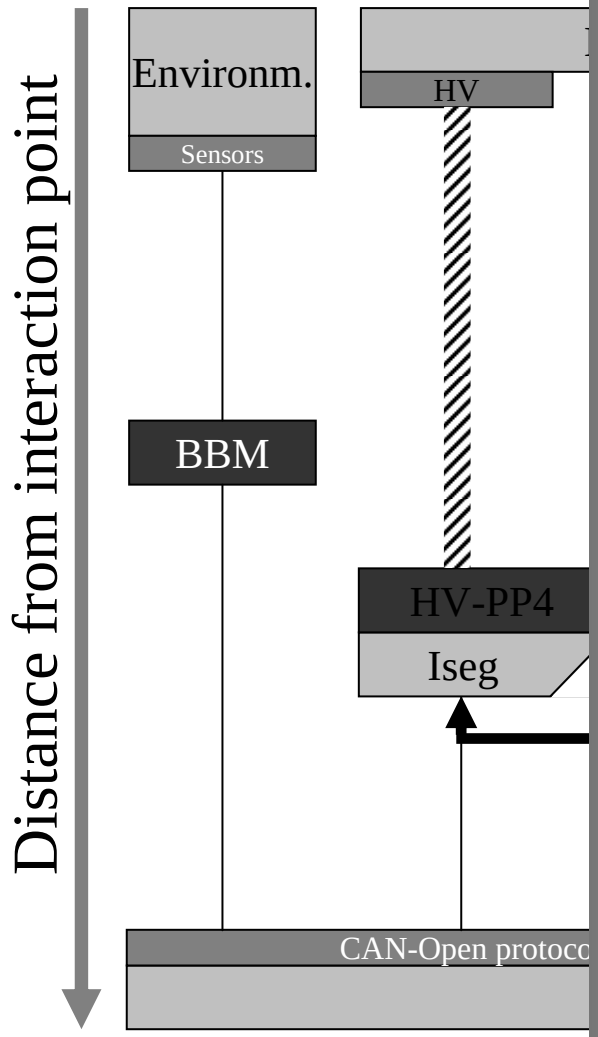
next slide

Regulator Station

- protects sensitive front end chips against transients
- 12 regulator boards/station
- 1 controller board per station (FPGA Actel APA075 internal control, ELMB communication to outer world
- reg. board houses 16 regulator circuits (all you need for one half stave)
- key component: ST LHC4913
- adjustable output voltage 0 to 12 V via digital trimmers
- external on/off control



High Voltage



Iseg HV supply:

- module depletion HV
- 16 channel power supply
- max 700 V / 4 mA
- floating
- protections:
  - over-voltage, over-current

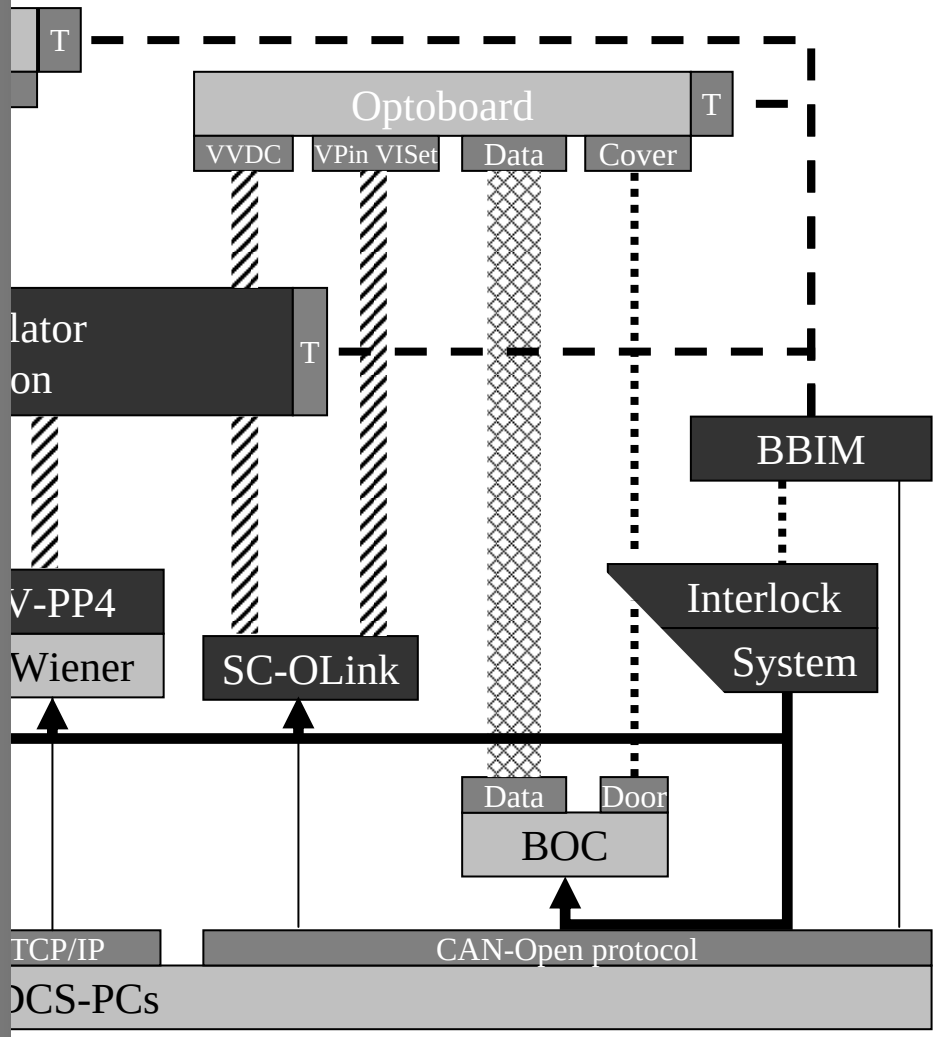
HV-PP4:

- mapping of modules to PS channels (modularity 6/7 or 2)
- uses ELMB
- objective of current measurement (to be implemented):
  - 5% precision
  - 0.4 µA to 4 mA range
  - opto-decoupled

SC-OLink

Supply and Control for the Opto Link (SC-OLink):

- floating outputs between 5-20 V and 20-800 mA
- controlled and monitored by an ELMB
- decoupled via opto-couplers / transformers
- 12 bit DAC with SPI interface
- hardware current limitation



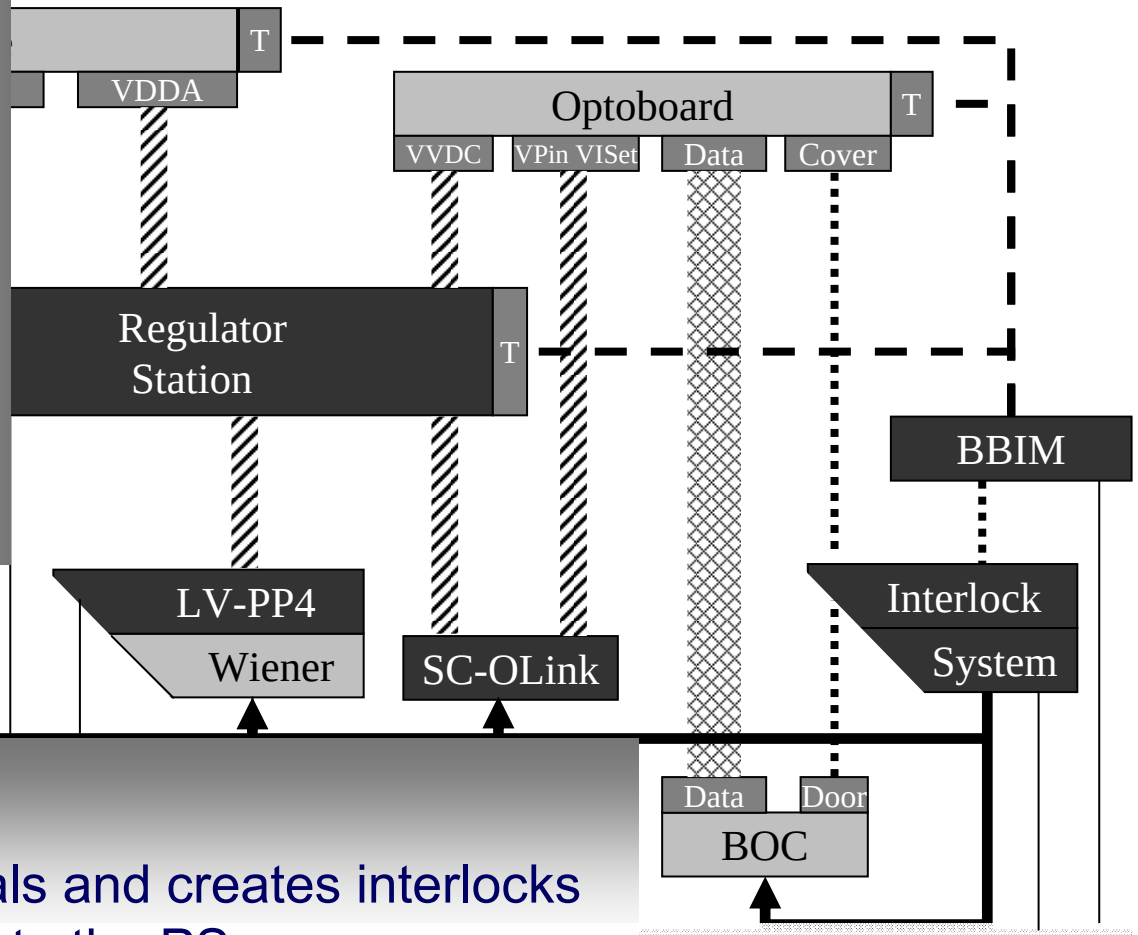
Interlock System Requirements

- prevention of human injuries (lasers)
- prevention of detector damage (temperature)
- fast reaction time
- hardware based
- self-certifying (by monitoring)
- radiation tolerant
- flexible logic (changing modularities)
- fine granularity

Interlock System

BBIM:

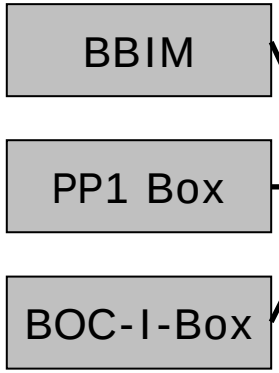
- digitization / discrimination of analog temperature values
- uses ELMB for monitoring



Interlock System:

- receives digital signals and creates interlocks
- distributes interlocks to the PS
- uses ELMBs for monitoring

The Interlock System



Incoming Signals:

2150

Logic Units

Interlock Distribution Boxes

Interlock controlled Devices:

1100

	action on individual channels or small group of channels				action on all channels			
	HV	**LV**	**SC-OLink**	**BOC**	**HV**	**LV**	**SC-OLink**	**BOC**
T_{Module}	X	X						
$T_{Regulator}$	X	X	X					
$T_{Optoboard}$			X					
$I_{BocDoor}$			X	X				
$I_{OptoboardCover}$							X	X
I_{DSS}					X	X	X	

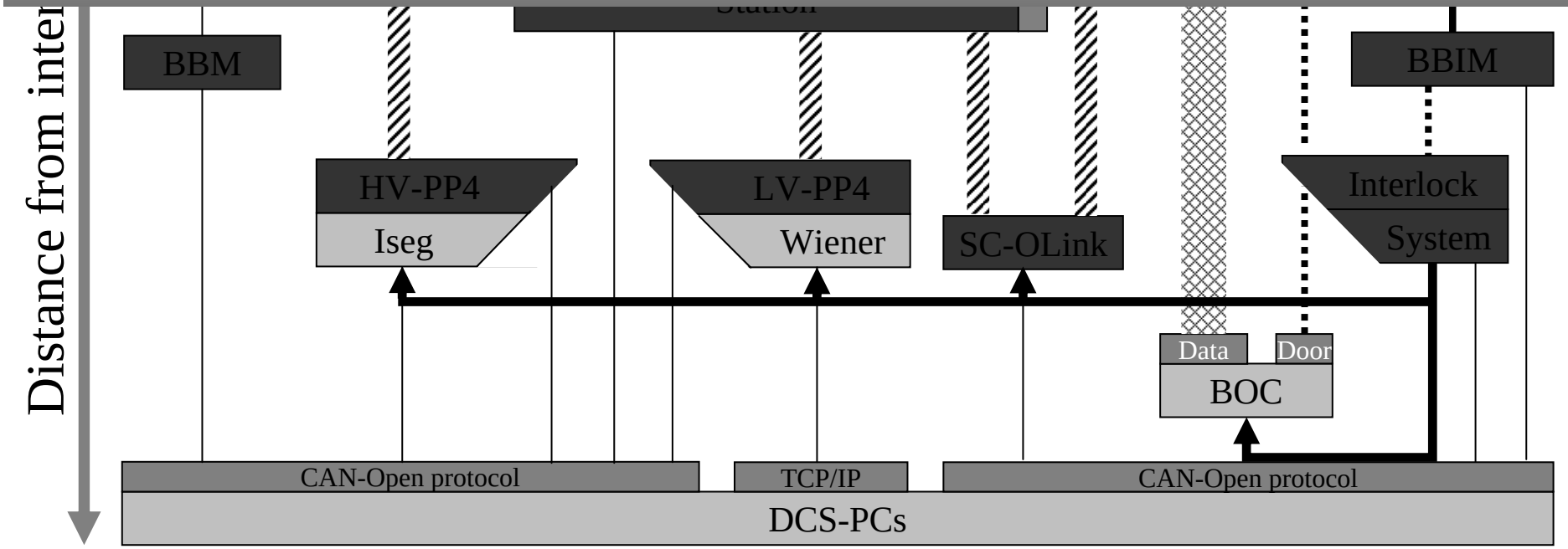
Connection to Control PCs

CAN:

- > 500 nodes
- all but Iseg ELMB-type
- ~5 s update time

TCP/IP:

- only Wiener
- private network



Summary

The DCS is responsible for:

- control of all power supplies
- monitoring of all process parameters
- the interlock safety system

It makes use of:

- a variety of sensors
- many custom made components that all use the ELMB:

  – Building Block Monitoring (BBM)
  – Building Block Interlock Monitoring (BBIM)
  – High-Voltage Patch Panel 4 (HV-PP4)
  – Low-Voltage Patch Panel 4 (LV-PP4)
  – Supply and Control for the Opto Link (SC-OLink)
  – Regulator Station
  – Logic Unit (LU)
  – Interlock Distribution Box (IDB)

DCS design parameters

- # power supplies: ~ 120
- # PS channels: > 5.000
- # parameters: > 30.000

- # operator: 1
- # PCs: ~ 10
- # CAN-nodes: > 500
- reaction speed SW: ~ 5 s
- automatic operation (via FSM / DAQ is Master)

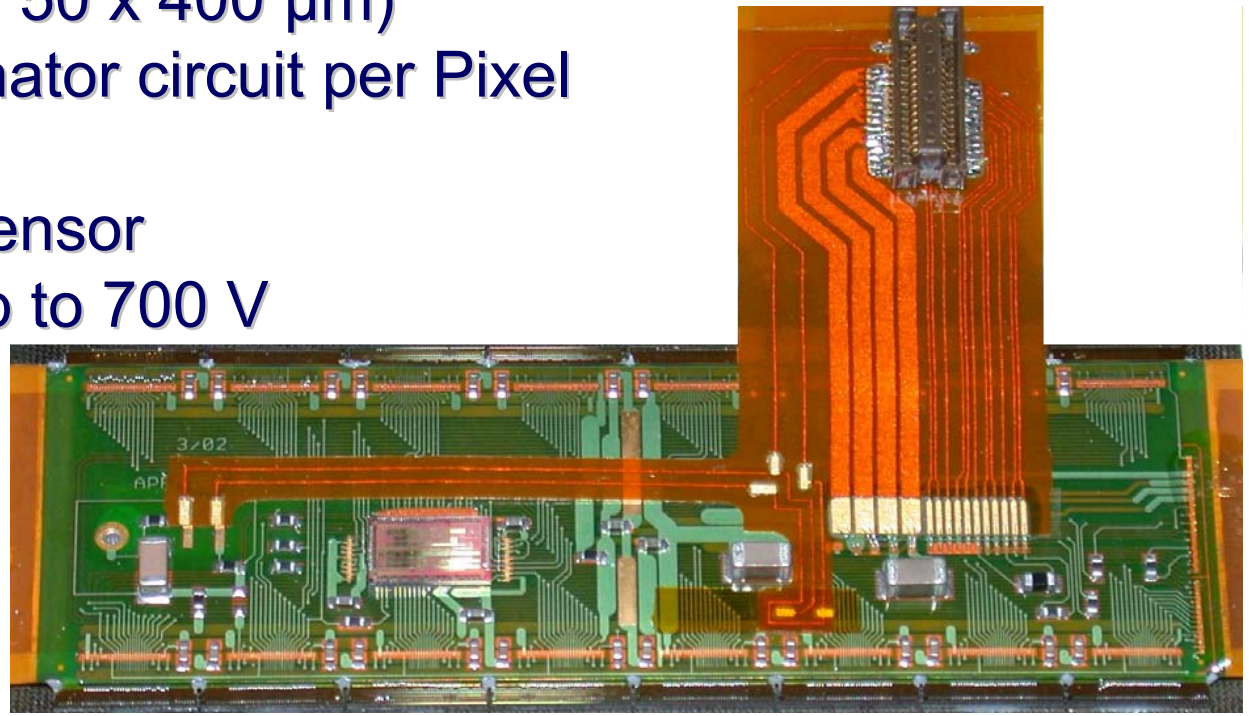
- HW-bases emergency system (interlock system)
- reaction speed PS (interlock): < 250 ms
- veto on ALL power supplies (not nec. at the same time)

The Pixel Module

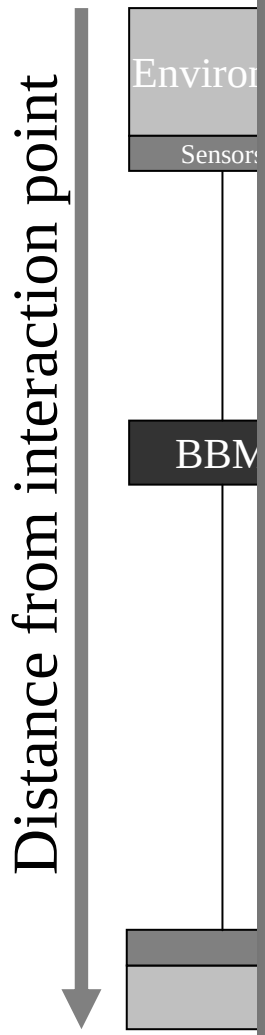
- 2 cm x 6 cm x 250 µm silicon sensor
- 16 front-end chips
- module contol chip (communication, control)

- 46.080 Pixels (each 50 x 400 µm)
- amplifier- / discriminator circuit per Pixel

- NTC temperature sensor
- depletion voltage up to 700 V
- VDD ~1.7 V
- VDDA ~ 2.1 V



Environmental Sensors



NTC temperature sensors:

- additional temperature sensors within the pixel volume

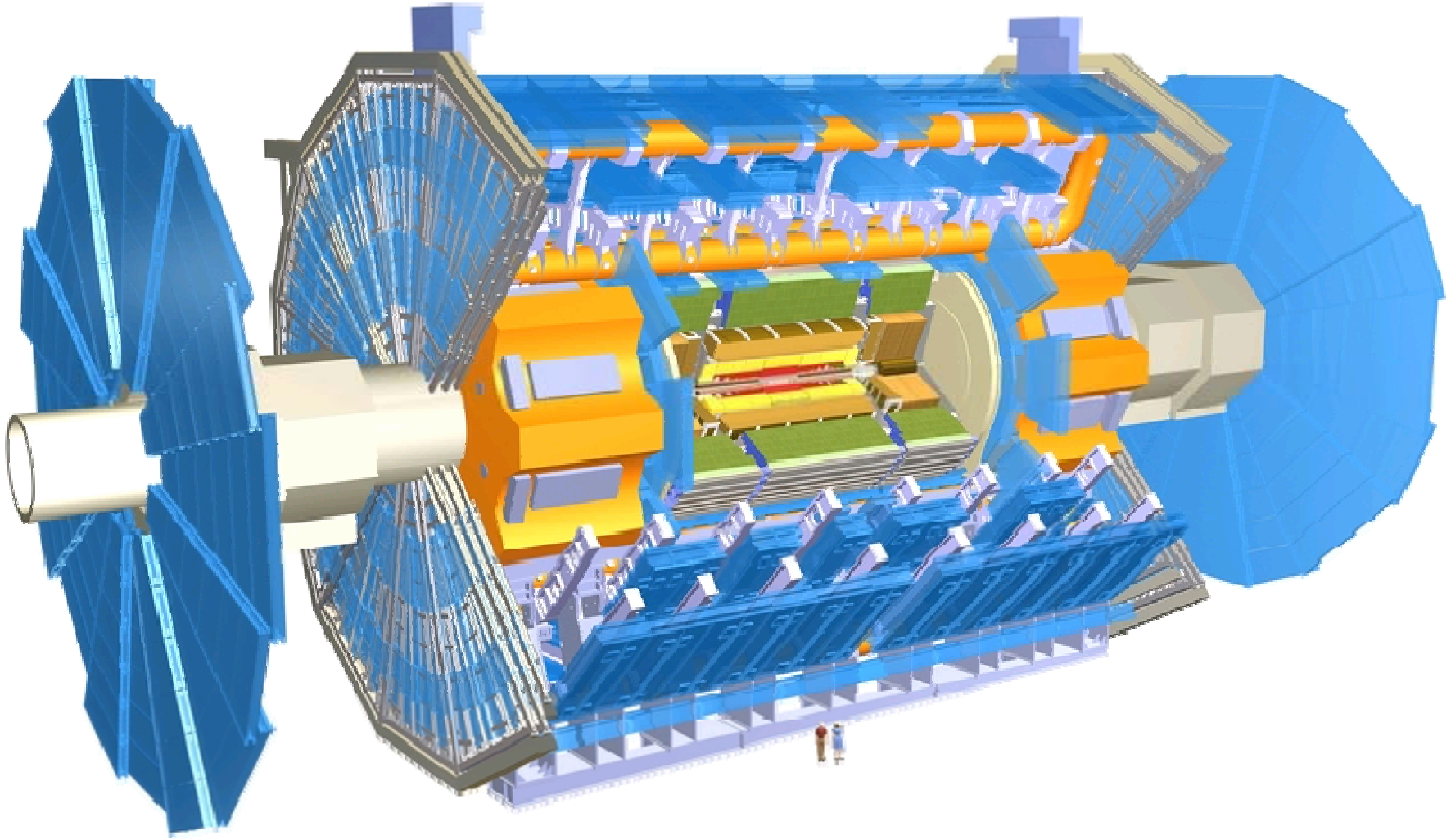
Xeritron humidity sensors:

- radiation hard sensors
- slow settling time (> 30 min)

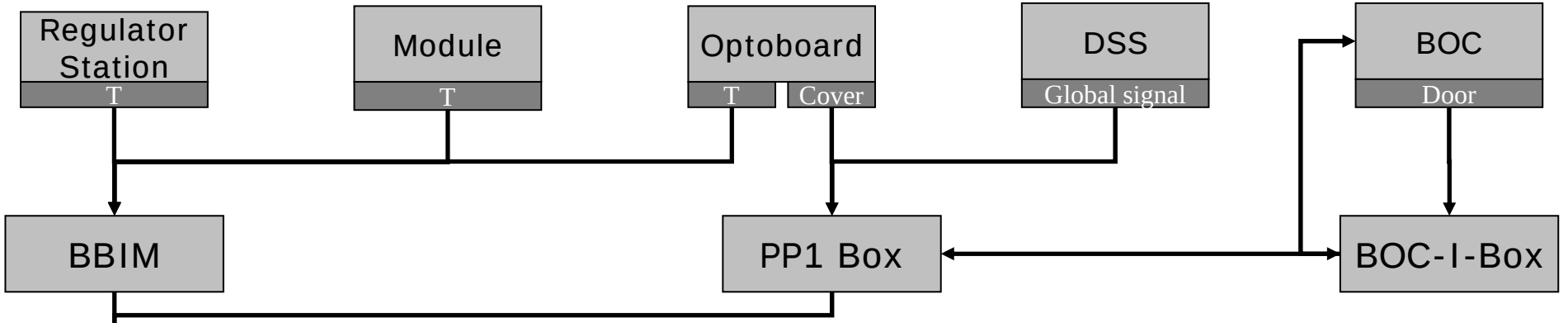
BBM:

- responsible for the read-out of the above sensors
- uses ELMB
- important for dew point measurement
- not used for the interlock system

The ATLAS Experiment



The Interlock System



	action on individual channels or small group of channels				action on all channels			
	HV	**LV**	**SC-OLink**	**BOC**	**HV**	**LV**	**SC-OLink**	**BOC**
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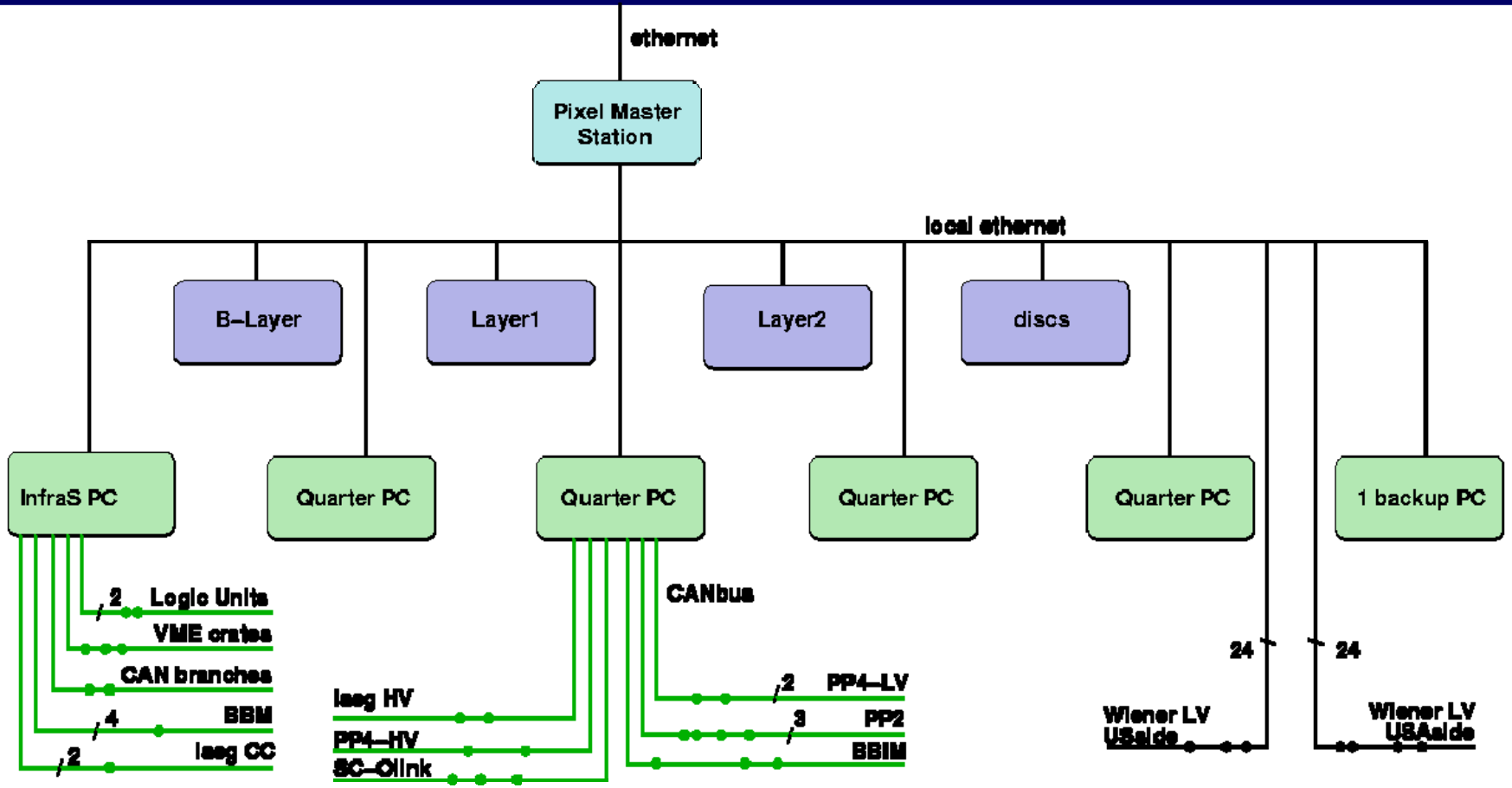
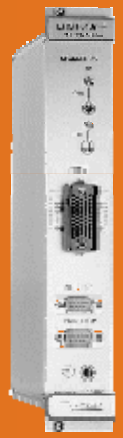
DCS-Net



- 100 CAN-nodes / Quarter PC
- 135 CAN-nodes on InfraS PC
- total of 535 CAN-nodes
- 9 to 10 CAN-busses / PC

V. Backup



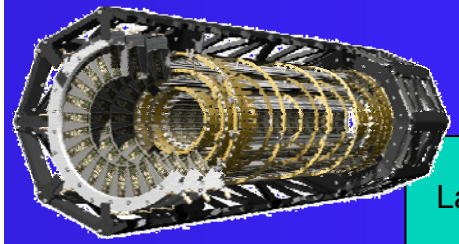
Temperature monitoring

High voltage

Low voltage

FIT: Functional part

SIT: Geographical part

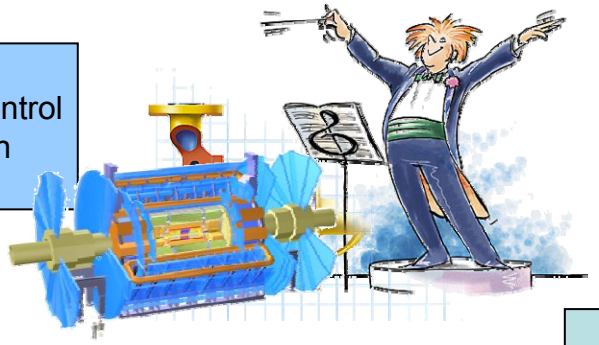


Layers

Bi-staves or Bi-sectors

Detector modules

Global control station



Graphical user interface

Finite state machine (FSM)

Front end integration tool (FIT)

Detector control stations

JCOP tool

System integration tool (SIT)

DAQ-DCS-communication (DDC)

Data Acquisition (DAQ)

Data bases

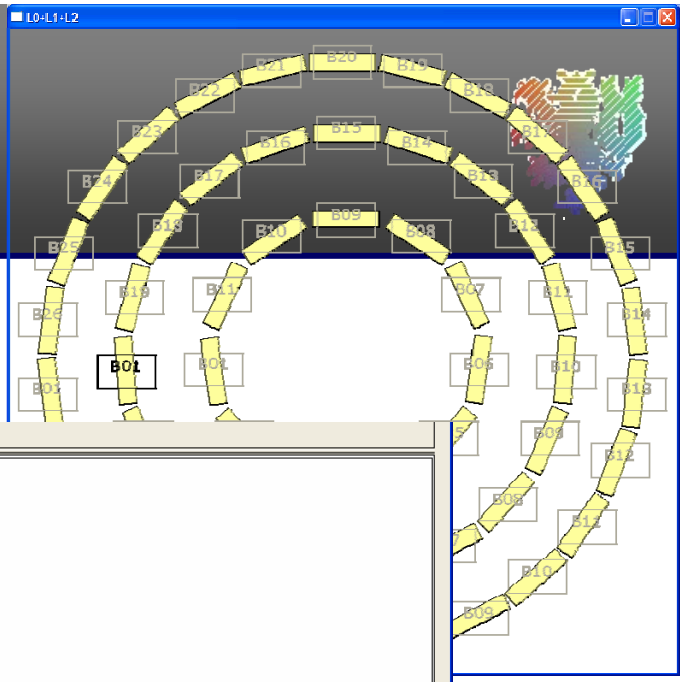
mapping set values

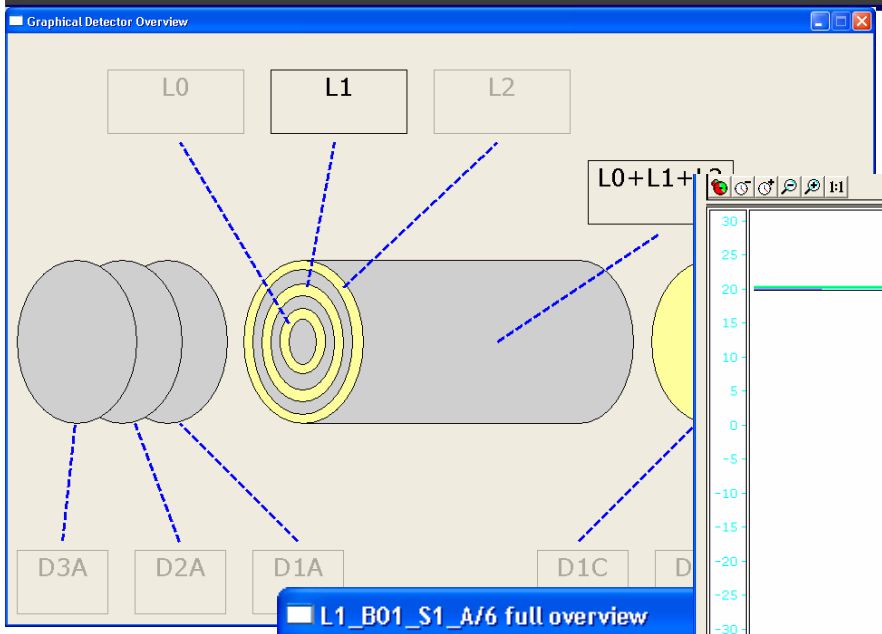
Configuration data base

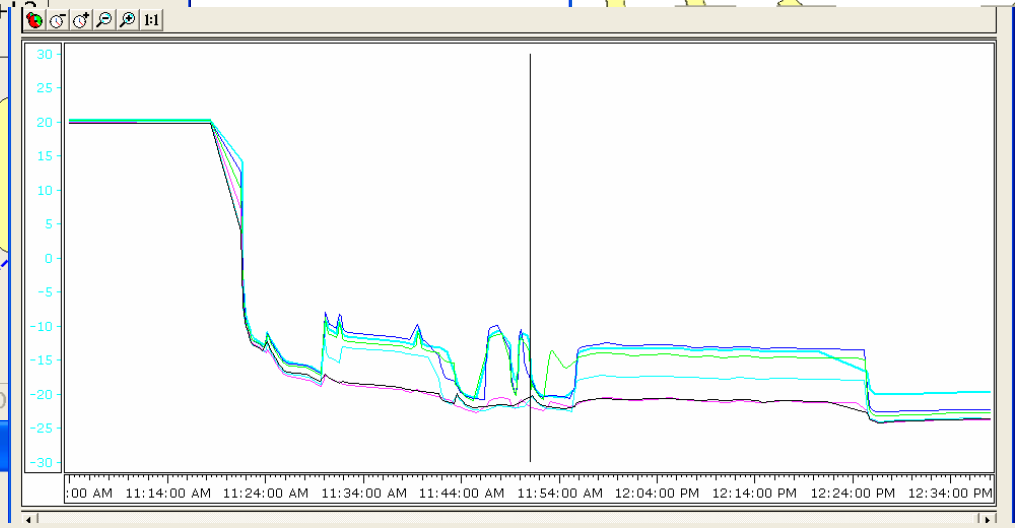
store data

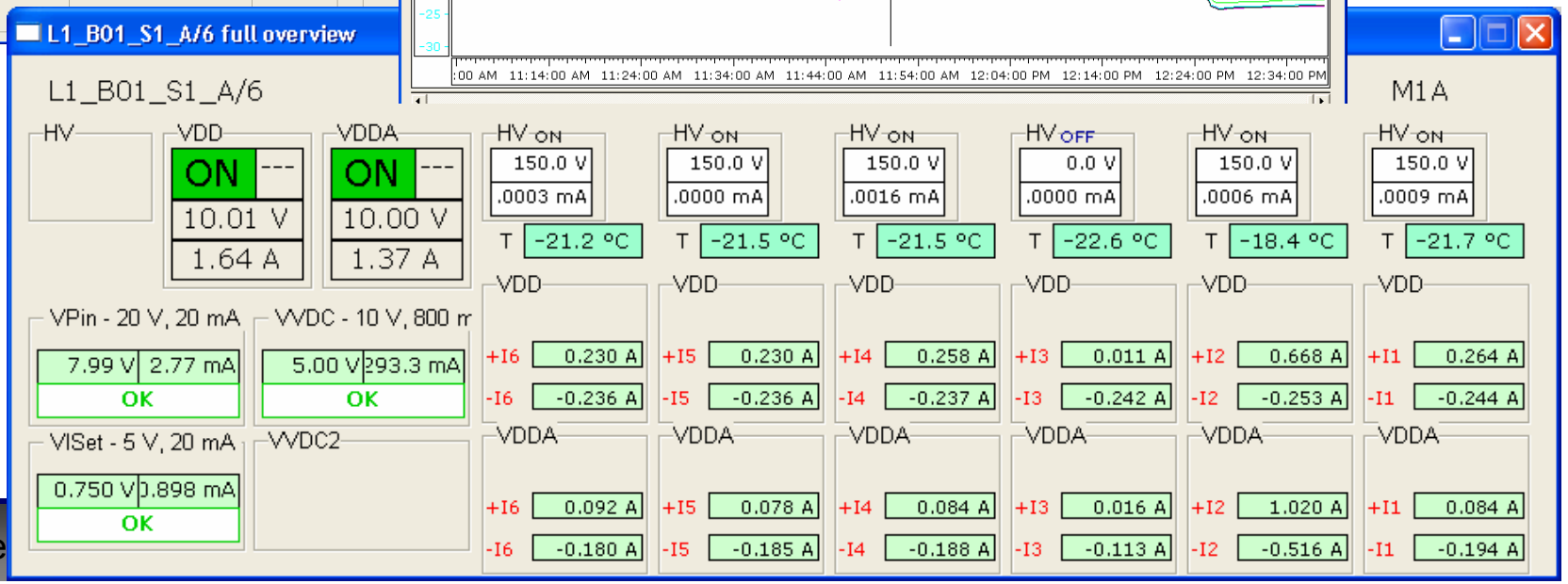
Conditions data base

User Interface







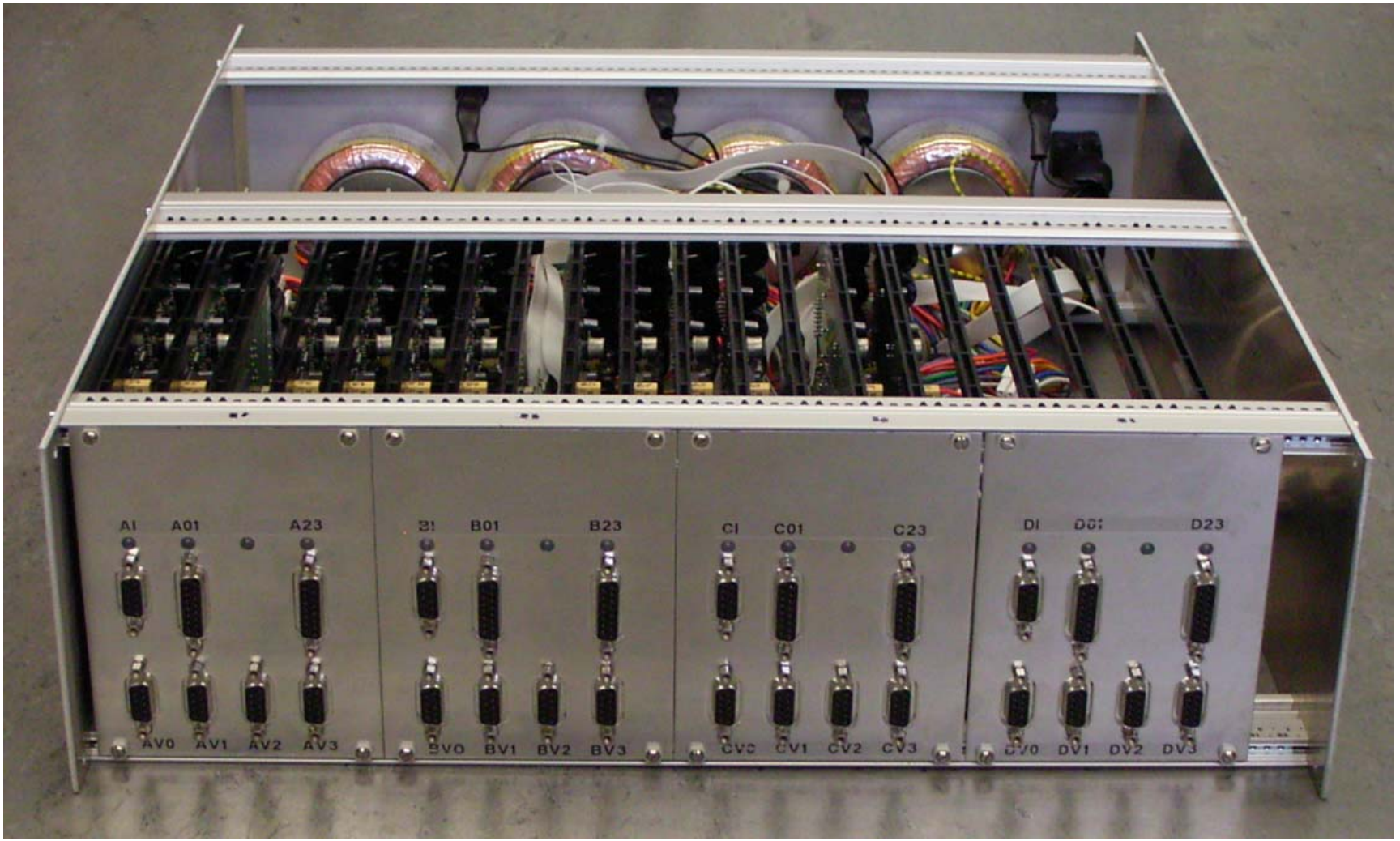


„The Hardware

Iseg


EHQ 8007n-F
CHANNEL OK
Imax
Vmax
HV-OUT
INHIBIT 0-7
SL
iseg
iseg
EHQ-
RESET
BANK
SELECT
STATUS
STDBY
POWER
ON
CAN-HV
SL1
SL2
POWER 230 V AC / 6,3 A

SC-OLink


A0
A01
A23
B0
B01
B23
C0
C01
C23
D0
D01
D23
AV0
AV1
AV2
AV3
BV0
BV1
BV2
BV3
CV0
CV1
CV2
CV3
DV0
DV1
DV2
DV3