DC to DC Power Conversion

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LECC2006

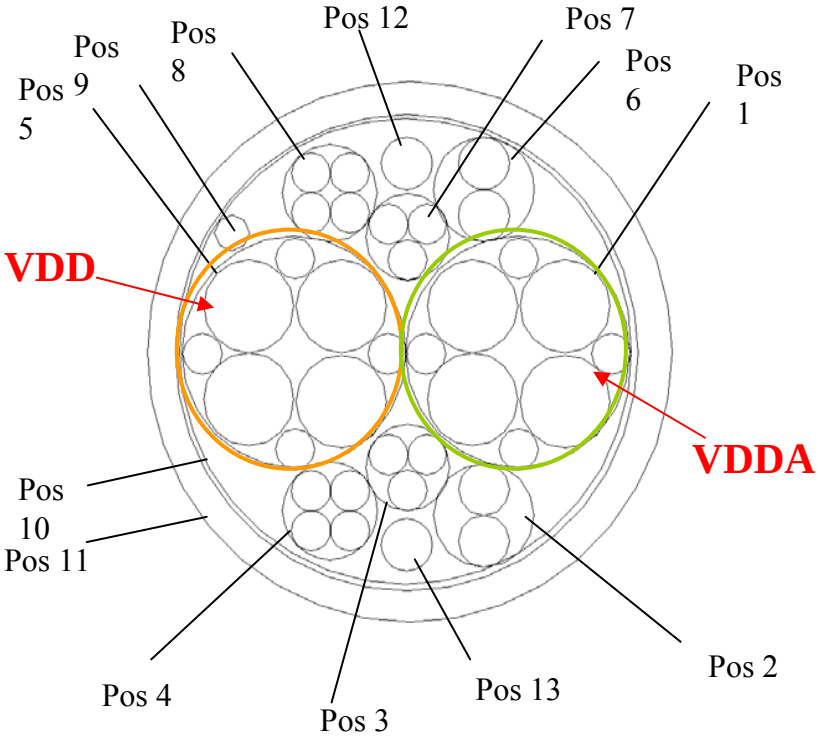
Valencia – Sept 25-29, 2006

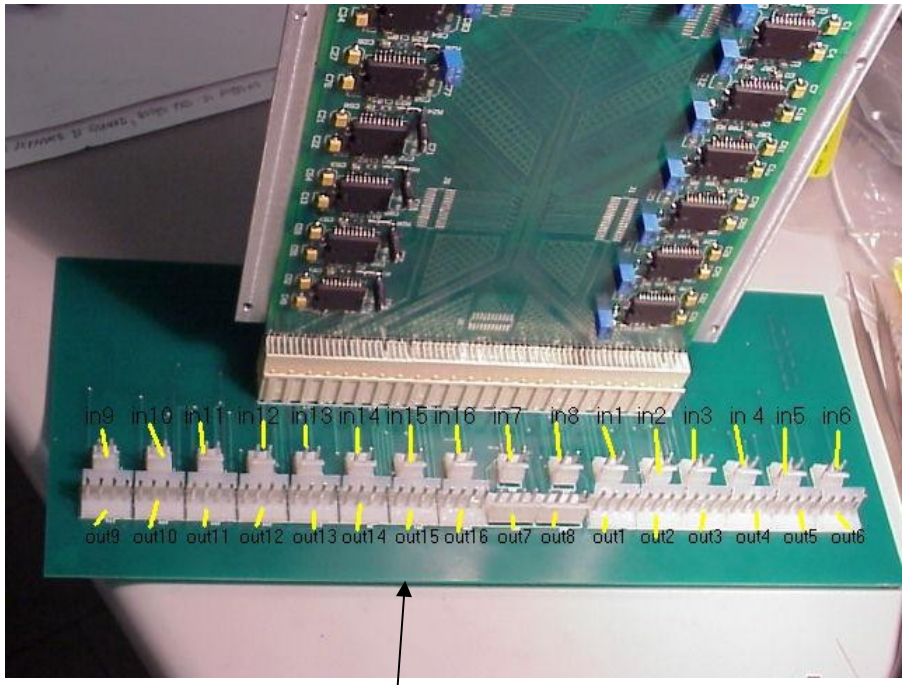
- Introduction
- Series Scheme
- Charge Pumps
- Tests on DC2DC_0 chip
- Plans

From the Power Board to the outside world

Atlas pixel cable

70% Power



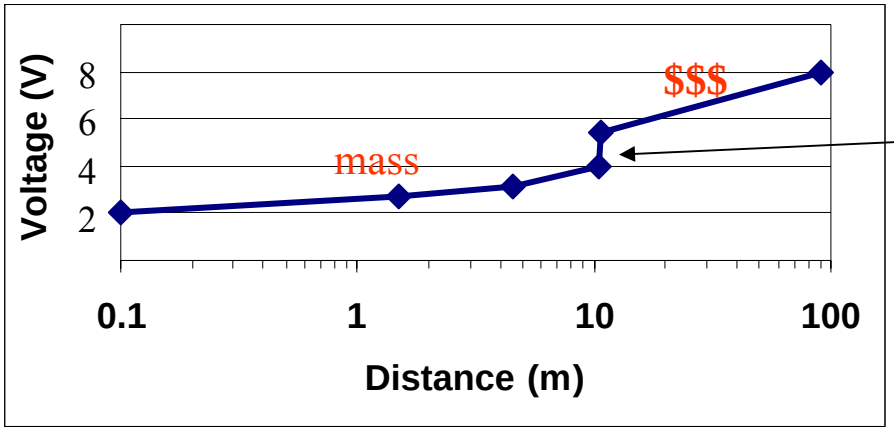


Adapter board … instead of the “bus board”.

The SCT cable is also made by Raydex !

High Power + Low Voltage = MASS + $$$

- Pixel Electronics operate at ~2V => large current
- ~2A low voltage per module (1744 modules) -3488A!



Remote sensing rad.-hard **linear** regulators necessary for safe operation

Voltage between +ve and ground leads vs. distance from module

Next time, deliver power at higher voltage

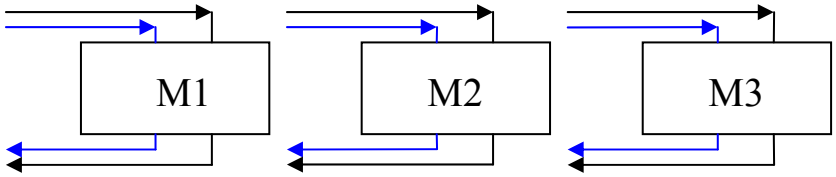
- Migration to smaller feature size in IC design means lower voltage. The .13u process that is considered for a new pixel front end will be either 1.2 or 1.5 vt.
- Need scheme to reduce voltage at the detector

Two Options

- Serial Power
  - Work started with Pixels. Demonstrated with present modules by Bonn group
  - Picked up for SCT modules by Marc Weber at RAL
  - Incorporated into stave prototypes by RAL and LBNL
- DC-DC converters
  - Proposed by LBNL
  - Initial simulations shown at Genova (details later)
  - Prototype switches fabricated and tested

Alternatives to IP

IP

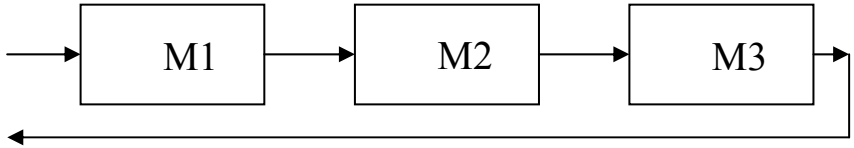


Analog and digital voltage

Serial powering or **parallel power bus with DC-DC conversion**

SP

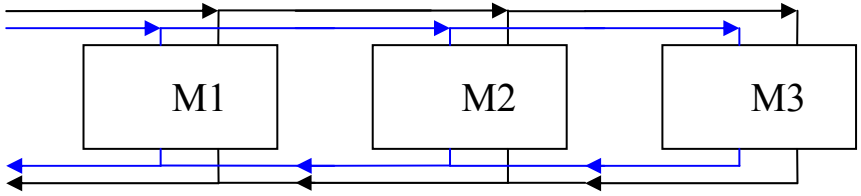
(RAL, lbl)



Constant current for both analog and digital power

PP with DC-DC conversion

(LBL)

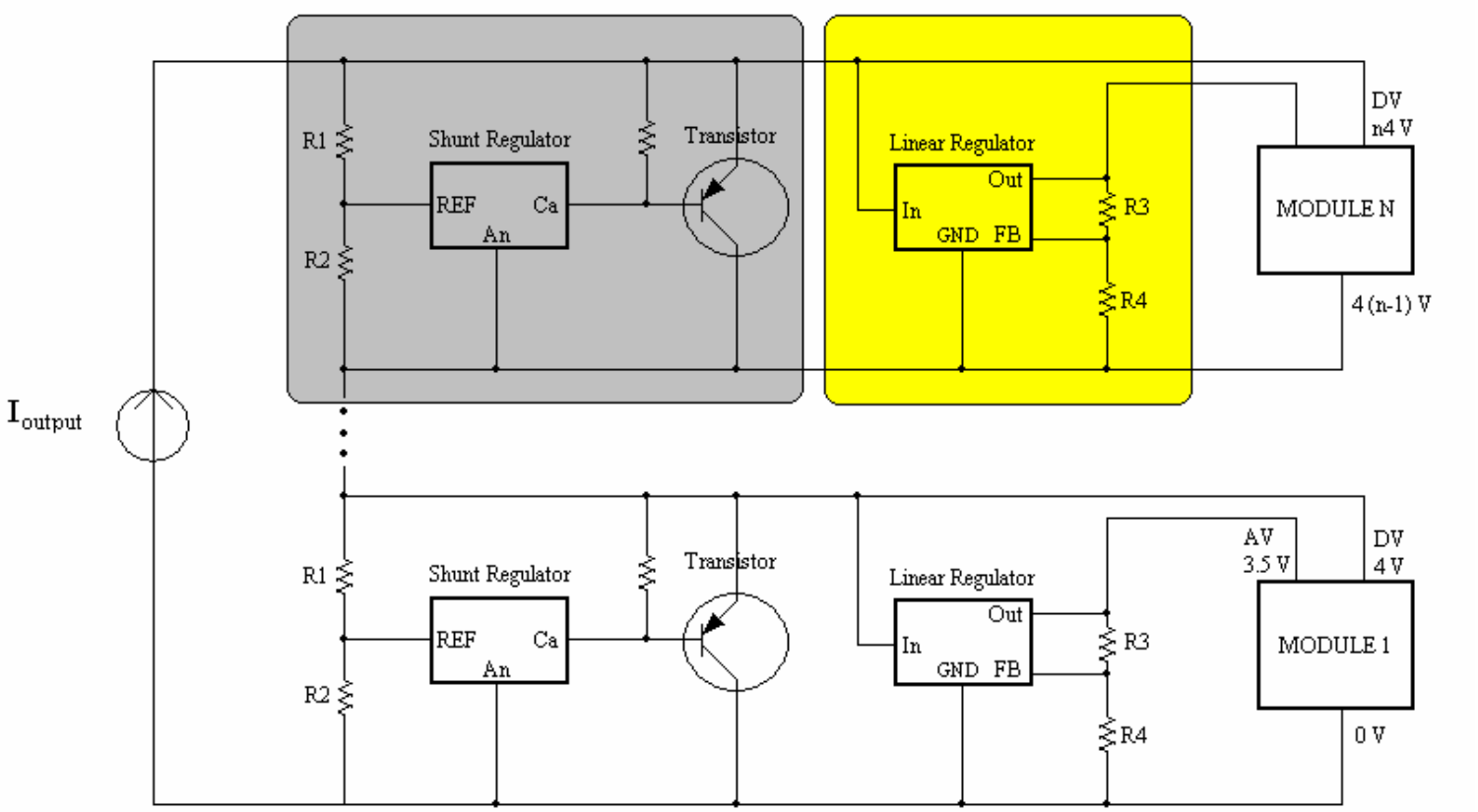


How does SP work?

Four elements

- Current source
- Shunt regulator and power device (digital power)
- Linear regulator (analog power)
- AC or opto-coupling of signals

Regulators

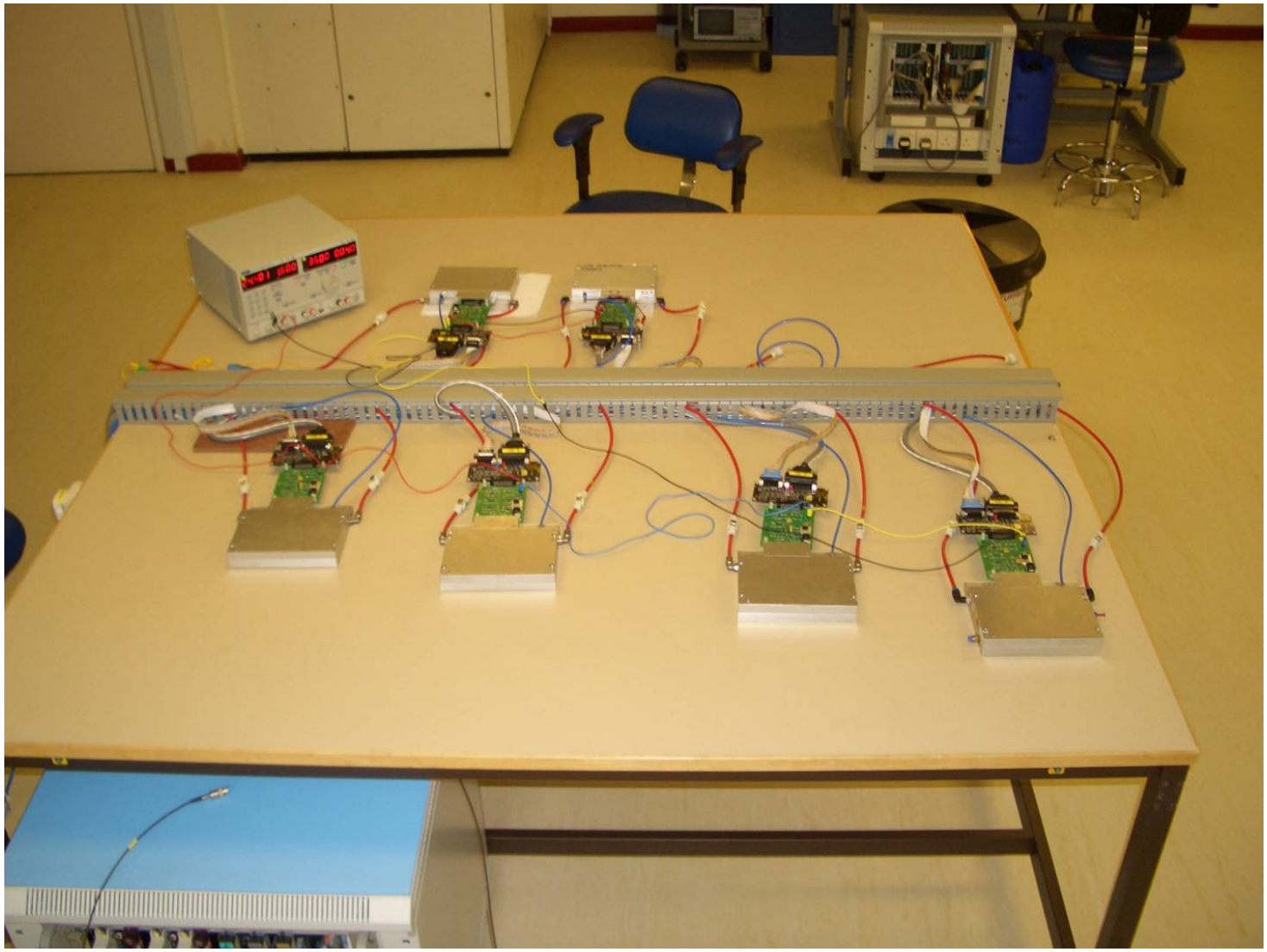


Chain of modules at different voltages

Chips on a module are connected in parallel (as usual)

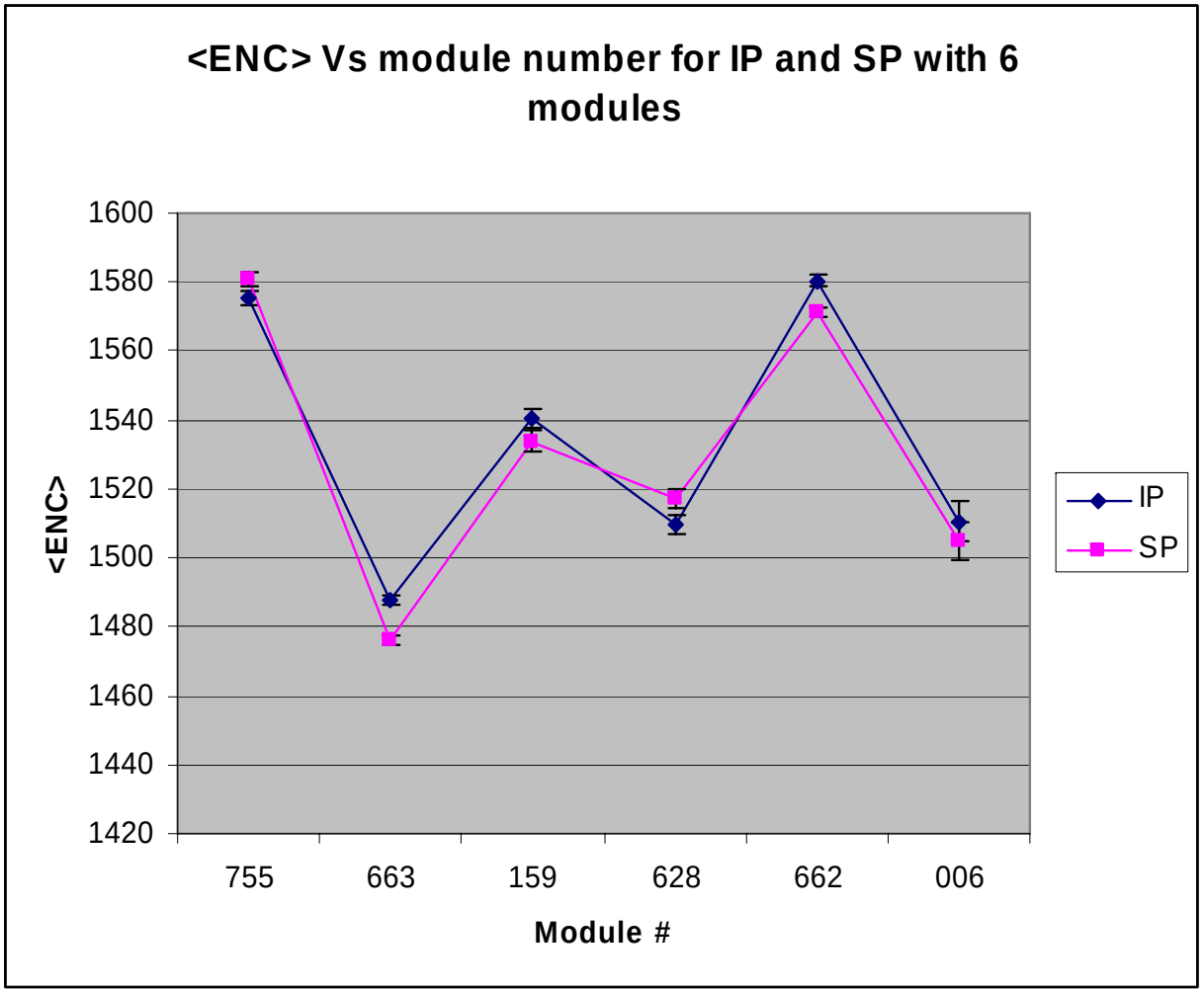
analog ground, digital ground and HV ground are tight together for each module (as usual) ⇔ floating HV supplies

Serial powering of six ATLAS SCT modules



RAL clean room. This was also used for QA of ~800 SCT modules

Noise performance of 6 SCT modules



Precise measurements; noise performance of SP is excellent

Future R&D program on powering schemes

Goal: be ready for implementation of advanced SP and DC-DC conversion PP systems in a realistic module assembly in ~ 3 years

Can distinguish three phases:

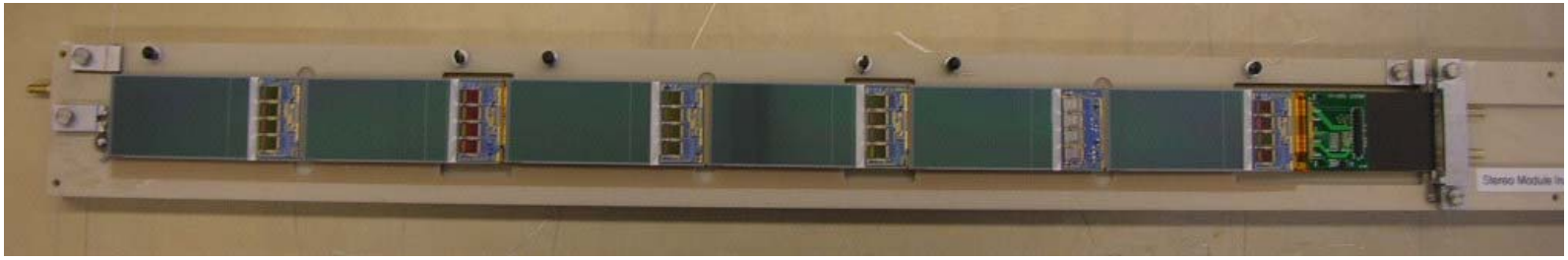
Generic studies (as presented here and in Carl's talk) to identify crucial features and challenges ⇔ "easy", affordable, "fun"

Develop radiation-hard *custom electronics (ABC_Next chip)*; build and test systems with *large number of modules* ⇔ significant effort, serious engineering

Implementation of power distribution schemes on *advanced supermodule prototypes* ⇔ "service", crucial to establish supermodule electrical performance

Prototyping: Phase 1 Test-bed

- Based on existing ATLAS ABCD chip and Run2b R&D*
- Develop ATLAS hybrid specific for multi-module
- 1 sensor + hybrid = 1 module (hybrid glued to Si)
- 6 modules per side + interface card
- Modules linked by **embedded bus cable**
- Total length 66 cm, 6144 channels
- Built around carbon fiber/foam laminate



- Measure multi-module performance with ATLAS electronics
- Explore assembly and mechanical aspects

*T.Akimoto et al, NIM A 556 (2006) 459-481

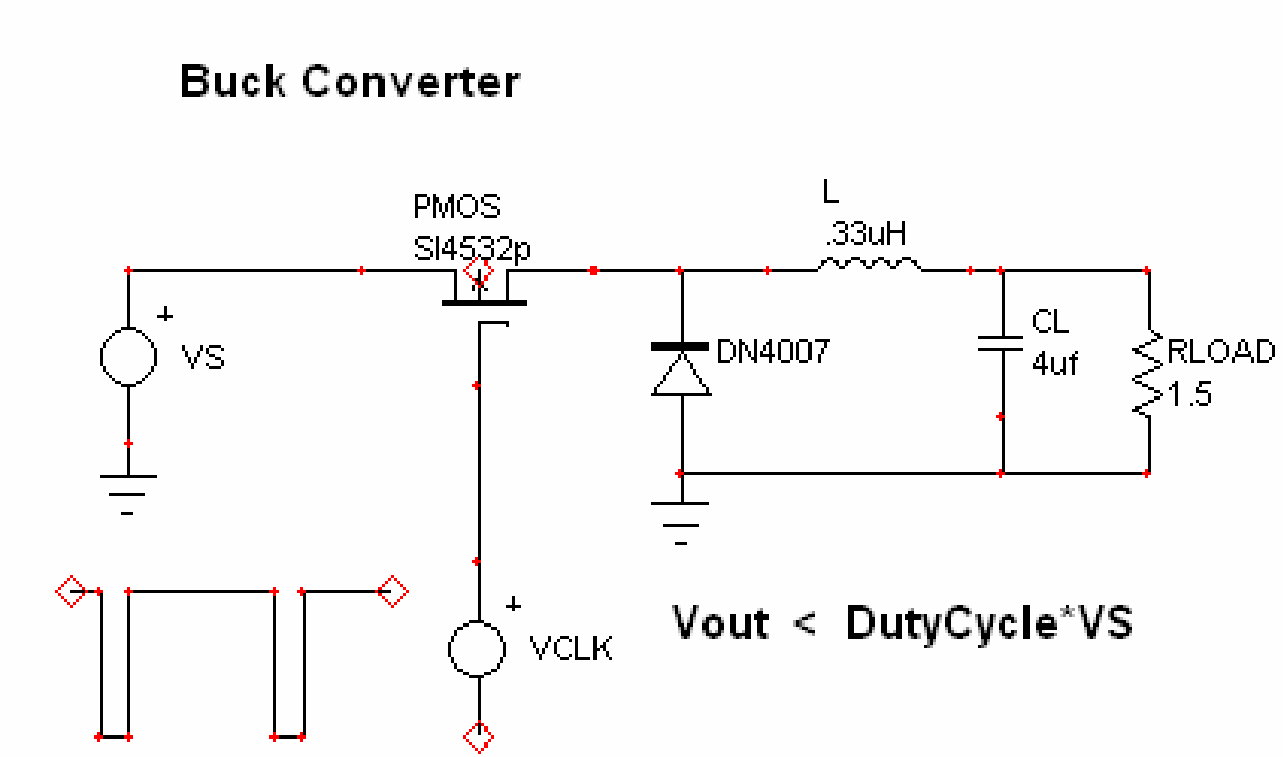
Plans

- Further study of serial powering…
- Develop a DC-DC test stave
- Preparation for an ATLAS SLHC 1 meter stave
  - Aim for construction and test in early 2007
  - Mechanical design and assembly fixtures (Miller)
  - 3 cm ATLAS detectors (BNL)
  - New bus cables and hybrid (with serial power)
  - ABCD-Next chip? (Dabrowski et al)

DC-DC Converter options

- Inductor Buck converter
  - typical in industry
  - We would have to worry about magnetic field, EMI from fringe fields, and would have to make our own air-core inductors.
- Switched Capacitor array
  - not common in industry except for divide by 2
  - Seems natural choice for us- fewer worries (see below).

Buck Converter



DC-DC Converters for Delivery of Low Voltage and High Currents for use in Magnetic field and Radiation environments.

S. Dhawan, D. Lynn b, H. Neal a, R. Sumner c, M. Weber d and R. Weber

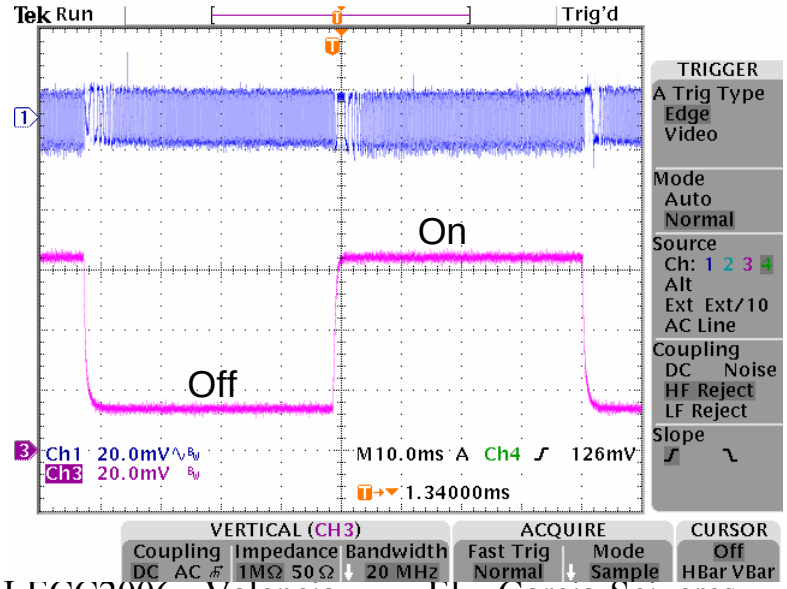
Buck Regulator

Micrel 2285 with

538 nH Air Coil

Output Ripple: 20 mV 8 MHz

0. 5 amp Load



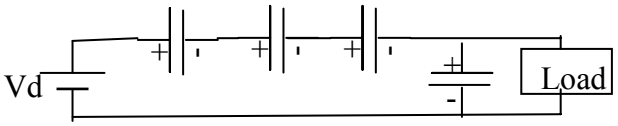
Switched Capacitor Options

- Most commercial applications multiply low supply voltage to drive a display. They require low current – switch resistance is not a problem
- We wish to reduce voltage and supply large currents – switch resistance is important
- There are many circuits – M. Makowski and D. Maksimovic' have shown that with n capacitors the highest voltage ratio which can be achieved is given by the nth Fibonacci number. We have simulated one.

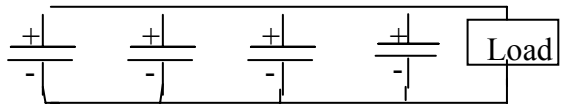
Divide by 4 Stack

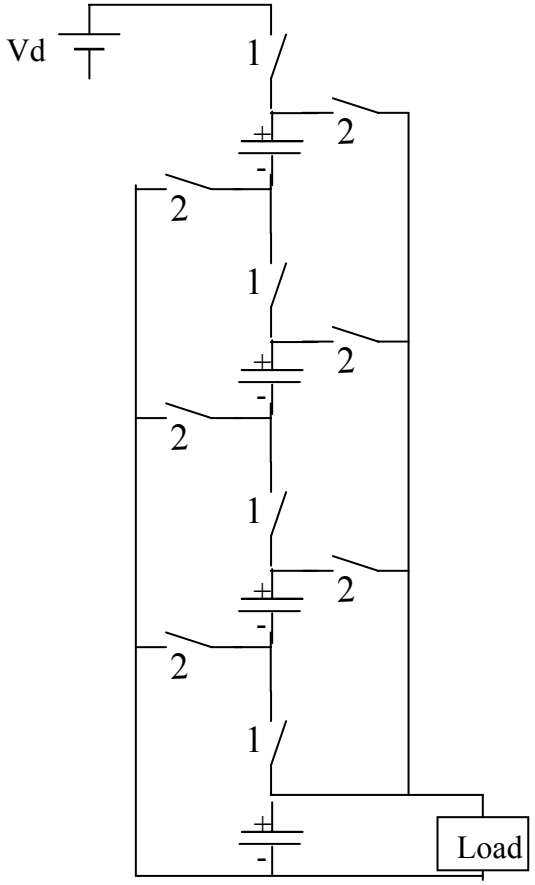
4 capacitors – 10 switches

- Phase 1 - Charge



- Phase 2 - Discharge





CMOS Transistor Switches

- Austria Microsystems H35 Process
  - Feature size 0.35μ
  - 3 gate oxides
  - Vds up to 50 vts
  - Bulk isolation
  - Gate oxide breakdown vt > 8vts

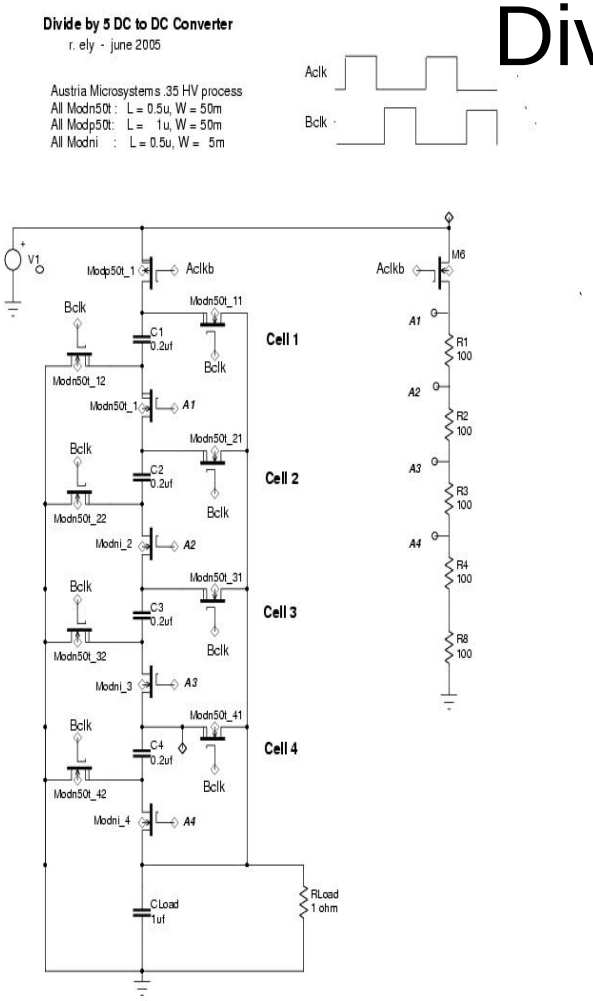
AMS H35 Transistors

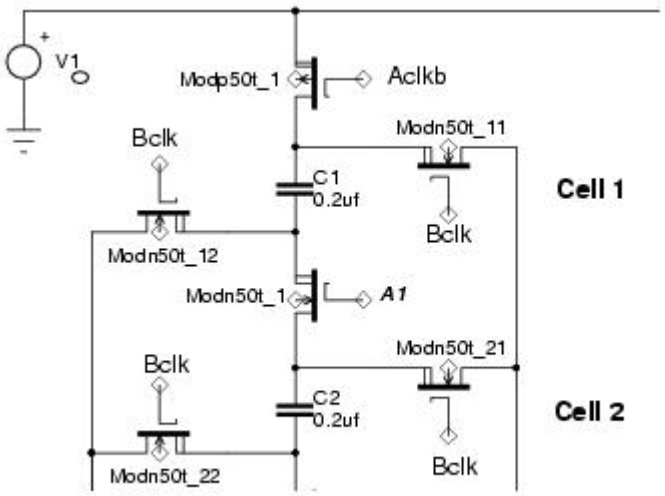
Device Name	Min. L (μ)	Max. Vgs(vt)	Max Vds(vt)	On Res. L = min W= 50m	C_g (pf)
NMOSI	0.5	3.6	3.6	0.06	125
NMOS50T	0.5	3.6	50	0.54	364
PMOS50T	1.0	3.6	50	0.73	369

Figures of Merit
(for divide by n)

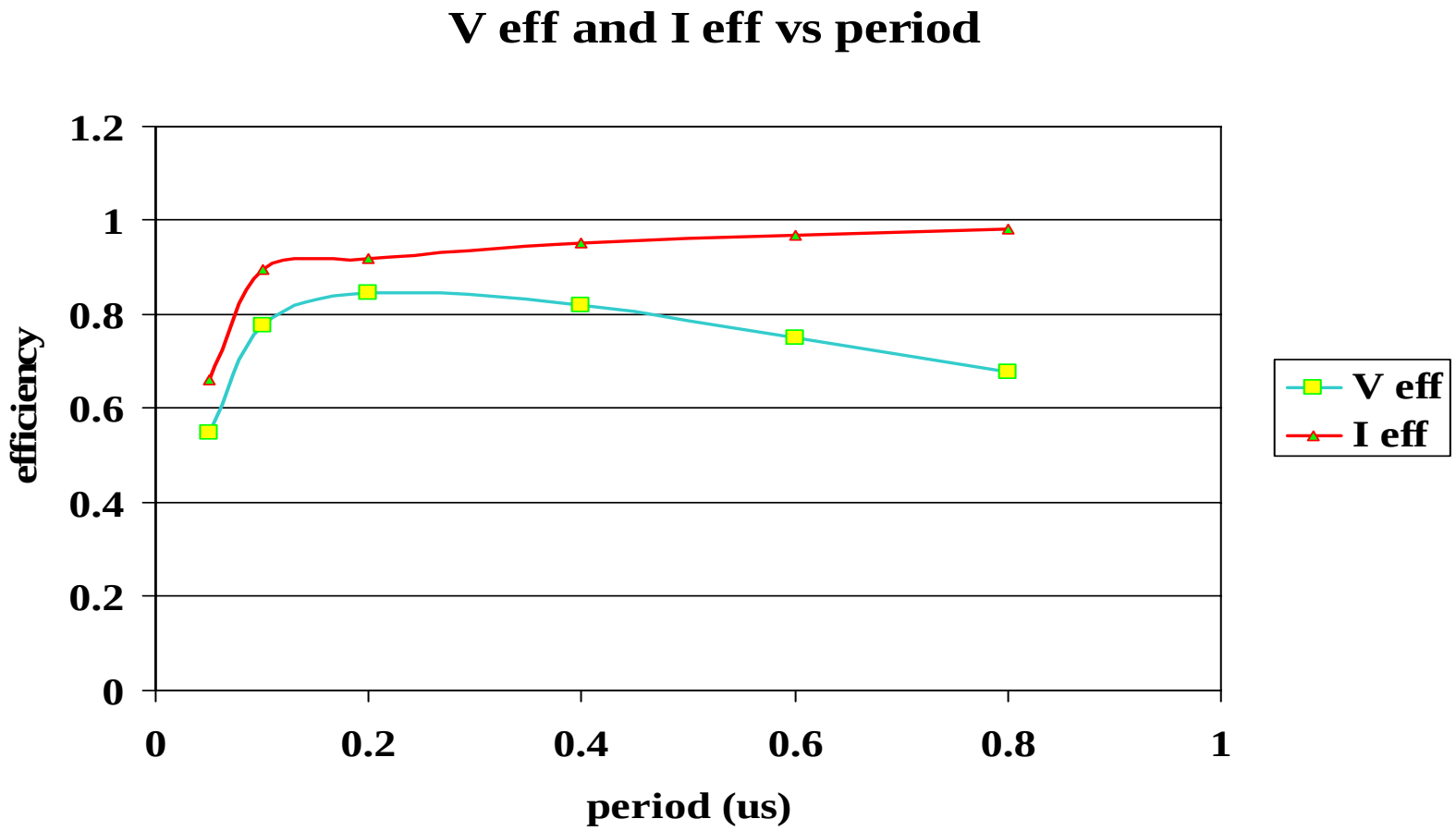
- Voltage efficiency - ε_V = n*Vout / Vin
  - Vout is a function of the load = Vin / n for no load
- Current efficiency - ε_I = Iout / n*Iin
  - Charge is lost charging the gate capacitance of the switches
- Power efficiency - $\varepsilon_p = \varepsilon_V * \varepsilon_I$
- Ripple - less than Iout*period/C

Divide by 5 Stack

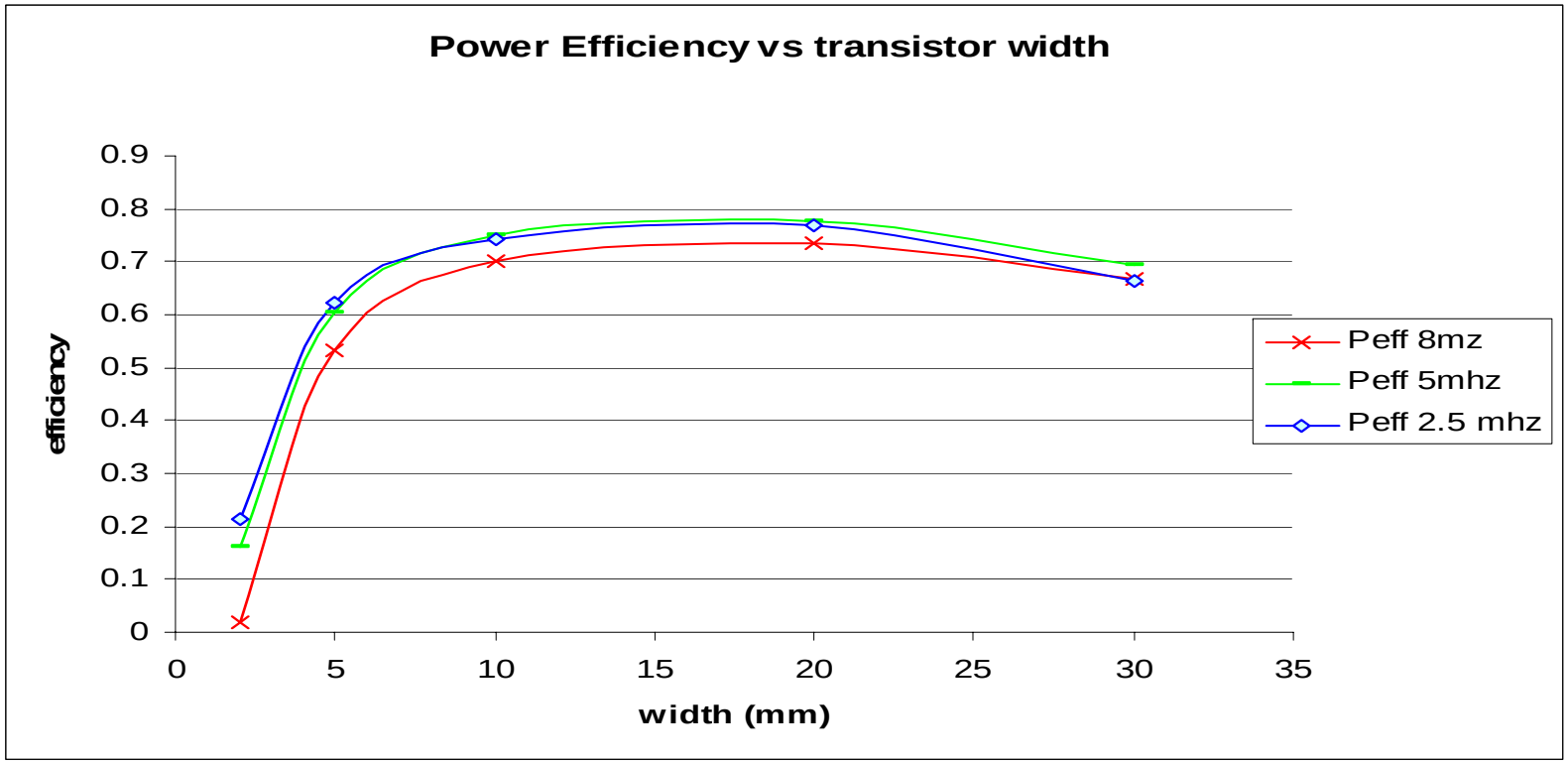




Efficiency versus Frequency



Power Efficiency



DC Conversion Conclusions

- At an operating freqency of 5mhz
  (Co = 4.7uf, C1 = 0.2uf
  - Voltage efficiency ~.84
  - Current efficiency ~.92
  - Ripple = 1.2%
  - Output impedance = 0.25 ohms (25mv / 100ma)

- Clock generator will reduce efficiency by 10%

First test chip
DC2DC_0 – Test Switches

Divide by 4 Stack

AMS 0.35u HV process

I_{out} = 250 ma

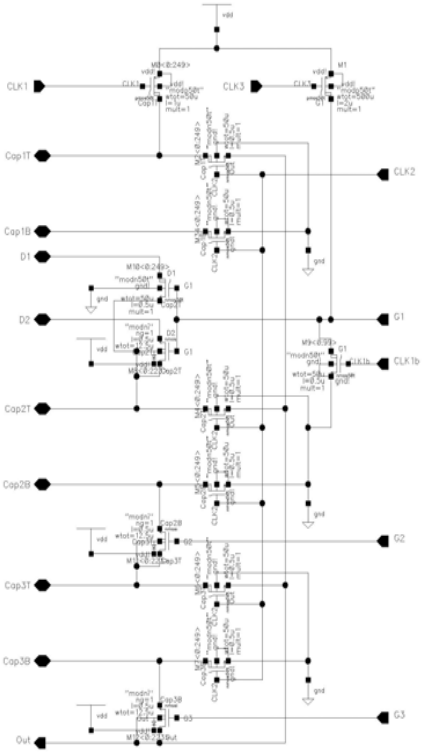
No internal clock gen

1/4th Size to save money

Purpose:

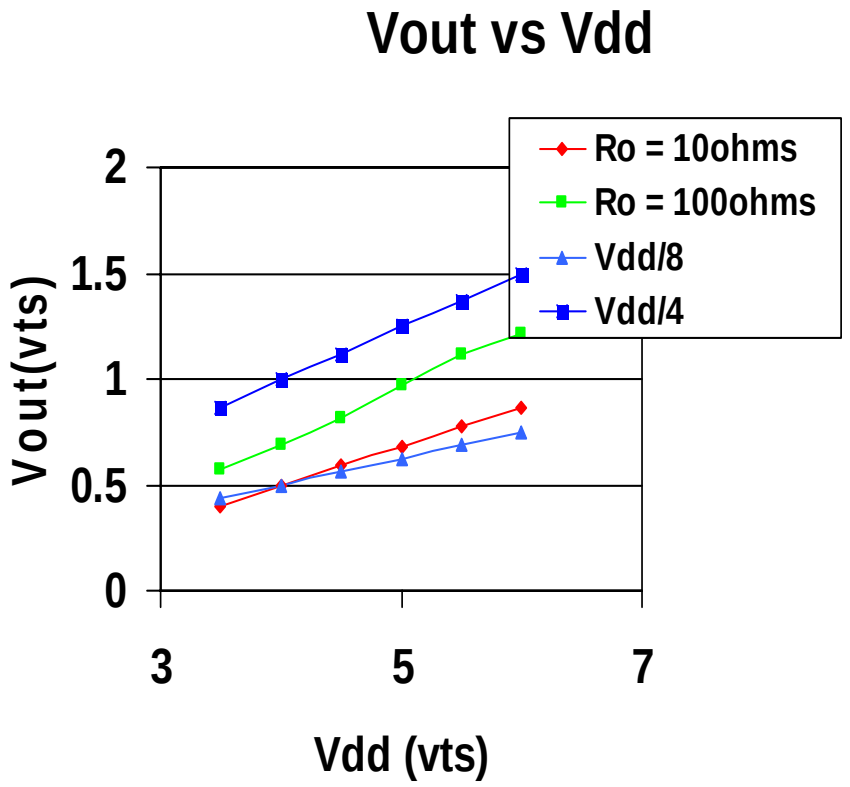
- Test circuit concept
- Characterize transistors
- Test radiation hardness

Submitted March 2006



DC2DC_0 Performance

- For Ro = 10 ohms
  - Voltage efficiency = .578
  - I_{in} / I_{out} ~1 - very high
- The large currents are due to a parasitic bipolar in Modni!
- Problem: bulk-drain is forward biased during discharge cycle
- Fix with Bulk bias control

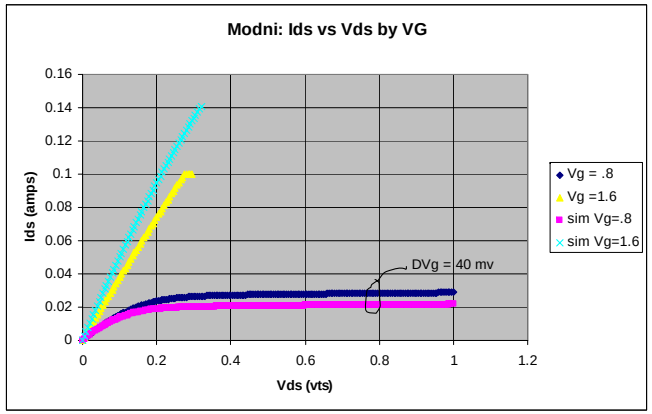


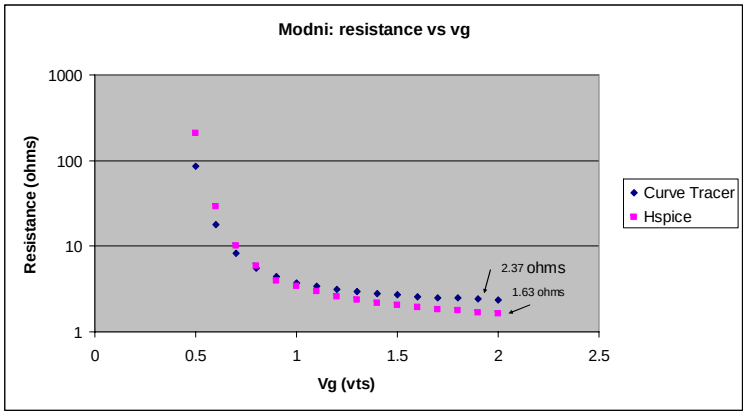
Transistor Measurements

- Use Agilent 4156c
- Measure Modni, Modn50t and Modp50t
- Compare with models supplied by AMS for hspice and eldo.
- In general the models for the n channel devices compare poorly. Especially at low Vds and short channel
- Of most interest is rds, d(vds)/d(ids), at low vds

Modni .5u/2.4mm

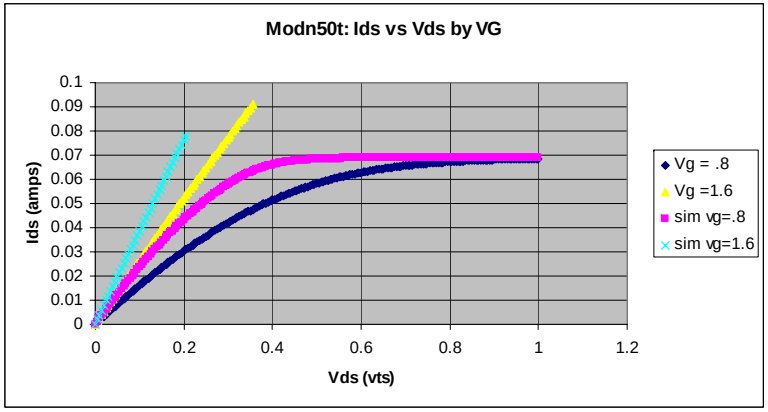
- The difference in Ids between meas and sim at Vg = 0.8 can be explained by a shift of the threshhold by 40mv
- Rds measured is 45% greater than Rds simulated



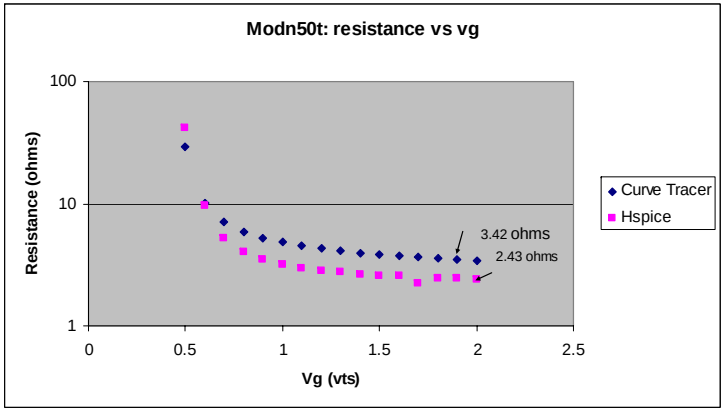


Modn50t .5u/12.5mm

- The comparison at Vg=.8 agrees with the AMS docs – the model is bad for intermediate Vds

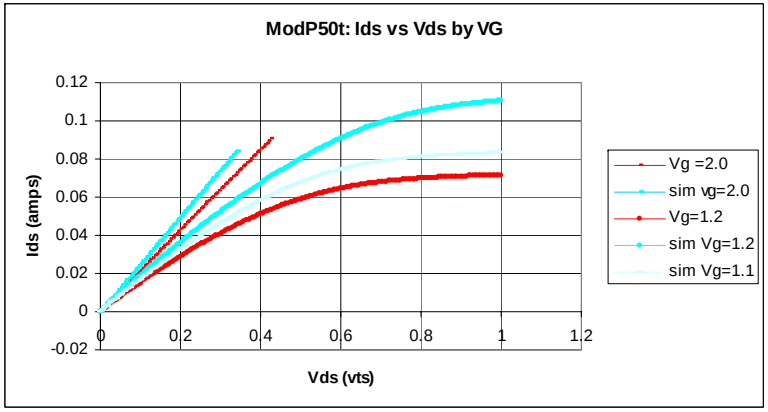


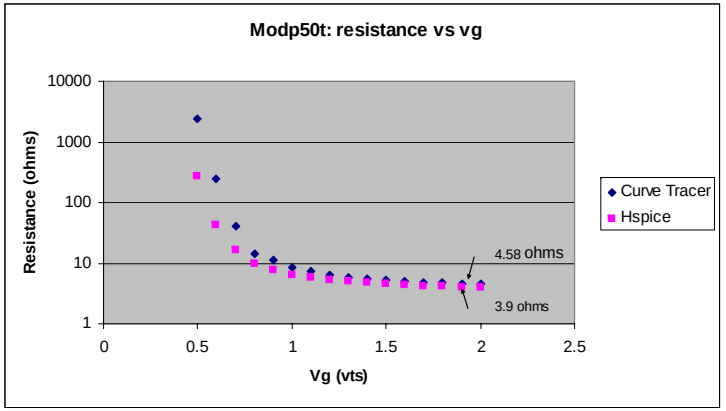
- Rds measured is 40% greater than Rds simulated



Modp50t .5u/12.5mm

- The disagreement at large Vds can be explained by a .12 v shift in the threshhold
- Rds measured is 35% greater than Rds simulated





Irradiation of DC2DC_0

- Use 55 Mev protons from the 88” cyclotron
- 20 namp up to 10^{15} p/cm^2
- “The best laid schemes of mice and men gang aft agley” - Burns

Reschedule in October

Conclusion

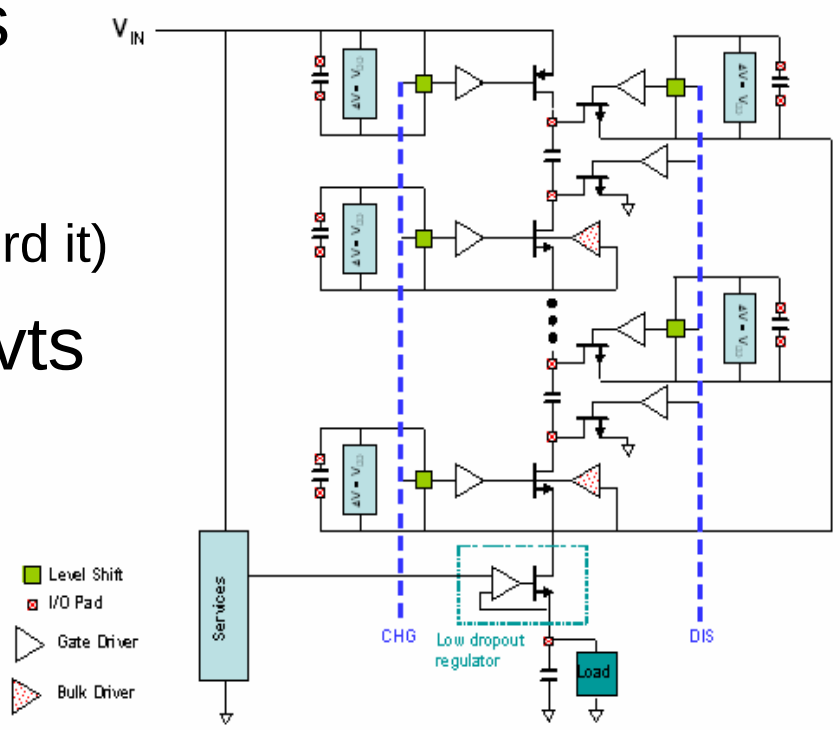
- We have to increase the size of the switches by 40% to achieve the low resistance required
- This is within the parameter variations advertised for the process

Future Plans

- Characterize several more chips
- Irradiate DC2DC_0 to 50 Mrad
- Submit a working prototype, DC2DC_1 next November (hopefully!)

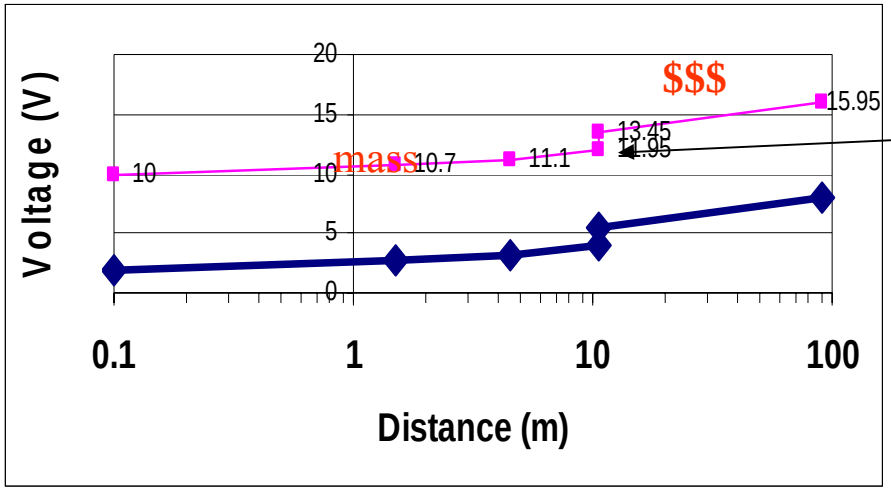
DC2DC_1

- Designed by P. Denes
- Divide by 4
- I_{out} ~ 1 amp (if we can afford it)
- V_{out} variable from 1-2 vts
- Substrate Bias control
- Voltage reference block
- Level shifted clock drivers
- Low dropout regulator



Finally, for example, Implement divide by 4 power converter

- Line drop from 16v to 10v with ¼ the mass
- 872 amps instead of 3488A!
- Deliver 62% of input power instead of 25%.



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