A readout system for microstrip silicon sensors (ALIBAVA)

Marco-Hernández, R.[a], Bernabeu, J.[a], Casse, G.[b], García, C.[a], Greenall, A.[b], Lacasta, C.[a], Lozano, M.[c], Martí i García, S.[a], Martinez, R.[c], Miñano, M.[a], Pellegrini, G.c, Smith, N. A.[b], Ullán, M.[c]

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OUTLINE

- Introduction:
  - Motivations.
  - Laser setup and radioactive source setup.
  - System requirements.
- System architecture.
- Daughter board:
  - Block diagram.
  - Readout chip main characteristics.
  - Daisy chain configuration vs. parallel configuration.
- Mother board:
  - Block diagram.
  - FPGA block diagram.
  - System functionality: system states diagram.
- Conclusion and outlook.

MOTIVATIONS

- Need of studying the main properties of highly irradiated microstrip silicon sensors (LHC, SLHC).
- Particularly the collected charge: detector performance.
- Difficulty for obtaining this type of measurements:
  - Required equipment is expensive.
  - A large number of channels has to be measured.
  - Minimum standardization: often the same functions are required (amp. & s.c., ADC, temporal logic, PC communication) but implemented with different modules (NIM, CAMAC, VME or custom electronic modules).
- Testing with an electronic system as similar as possible to those used at LHC experiments: a LHC front end readout chip should be used.
- Analogue readout is preferred for pulse shape reconstruction.

LABORATORY SETUPS

- Two types of setups are used for generating the charged particles at the laboratory: laser and radioactive source.
- Laser setup:
  - Laser light is generated by exciting a laser source with an external pulsed signal (for instance a 1 KHz rate).
  - This signal also can be used as a trigger.
- Radioactive source setup:
  - Charged particles are generated randomly.
  - A scintillator and a photomultiplier are necessary following the detector to generate a signal which will inform when a charged particle has crossed the sensor.

SYSTEM REQUIREMENTS

- The system will be compact and portable.
- The system will be used with two different laboratory setups:
  - It will have an external trigger input from one or two photomultipliers (radioactive source).
  - A synchronized external trigger output for pulsing an external excitation source (laser system).
- The system will contain two front-end readout chips (Beetle, LHCb) to acquire the detector signals.
- It will be communicated with a PC via USB, which will store and will process the data acquired.
- The system will be controlled from a PC software application in communication with a FPGA which will interpret and will execute the orders.
- The system will have its own supply system (from AC mains).

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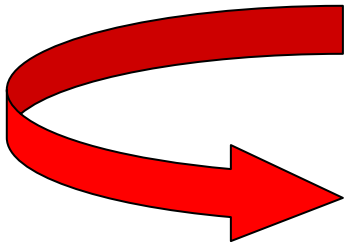
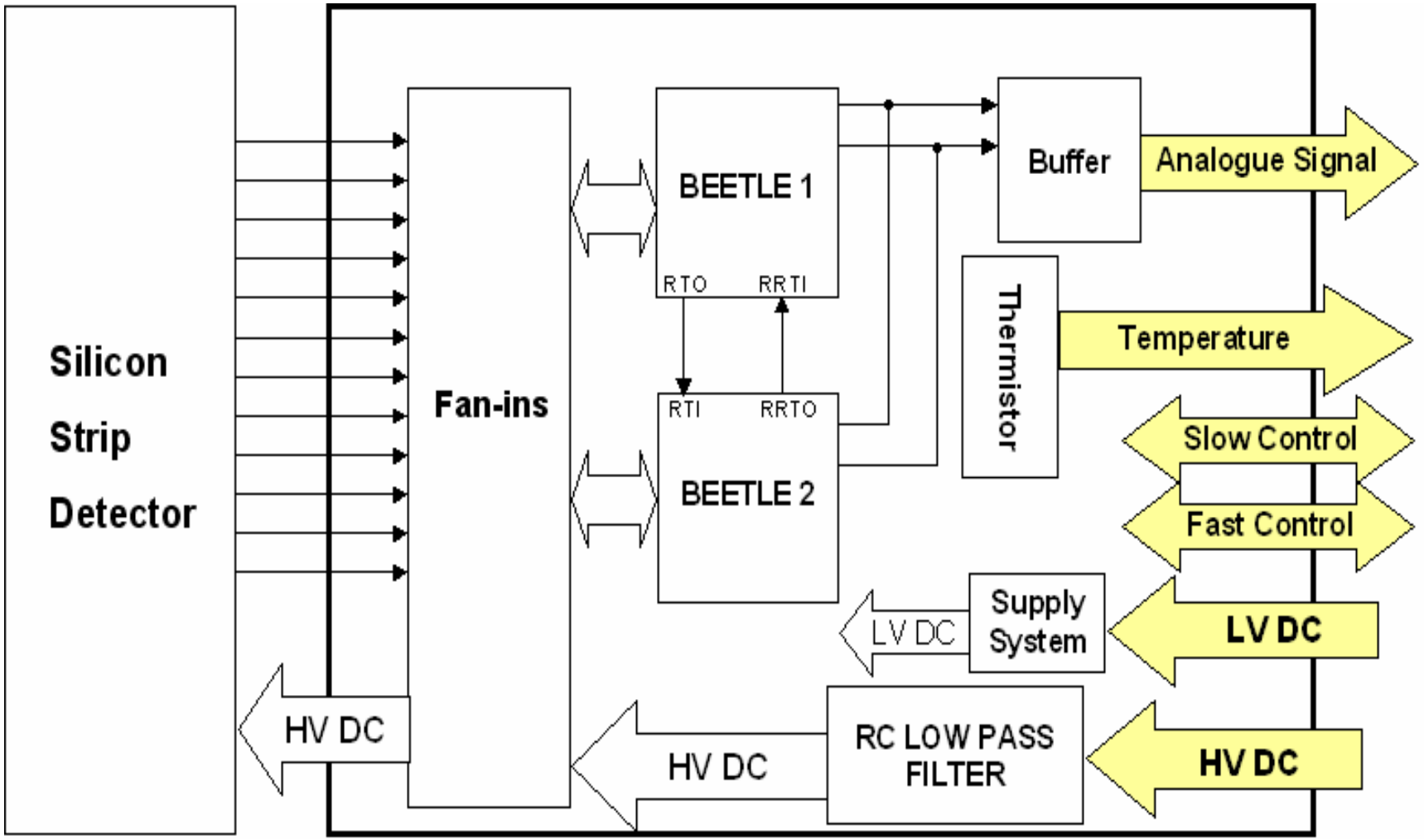


The main goal is reconstructing the analogue pulse shape at the readout chip front end with the highest fidelity from the acquired data.

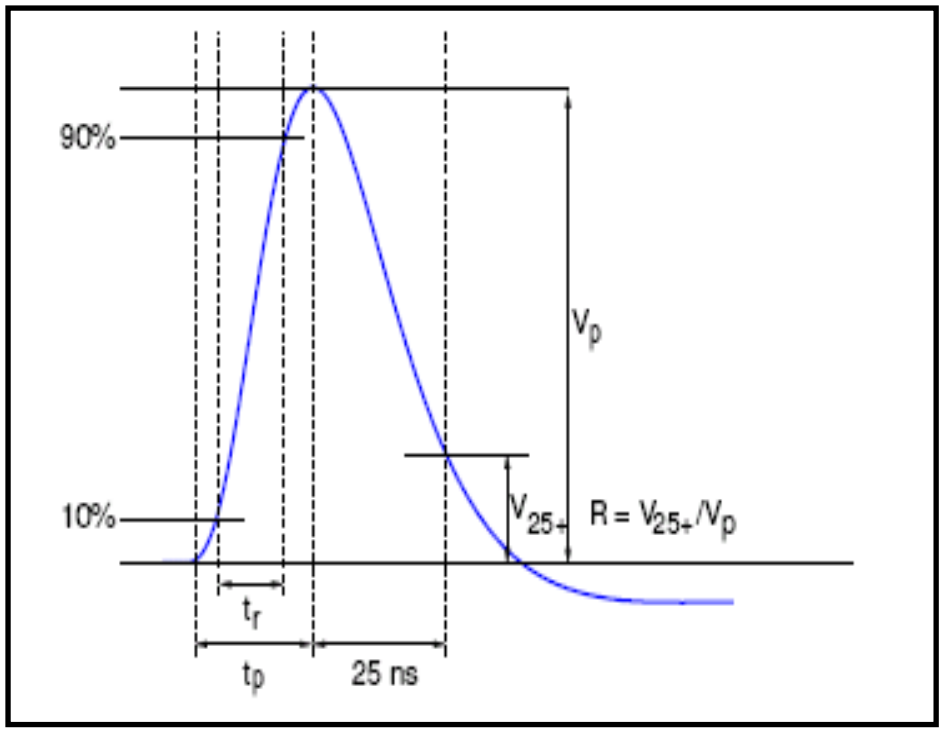
SYSTEM ARCHITECTURE

- Two main parts: software part (PC) and hardware part.
- Hardware part: a dual board based system.
  - Mother board intended:
    - To process the analogue data that comes from the readout chips.
    - To process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used.
    - To control the hardware part.
    - To communicate with a PC via USB.
  - Daughter board :
    - It will be a small board.
    - It will contain two Beetle readout chips
    - It will have fan-ins and detector support to interface the sensors.
- Software part:
  - It will control the whole system (configuration, calibration and acquisition).
  - It will generate an output file for further data processing.

DB: BLOCK DIAGRAM



BEETLE CHIP

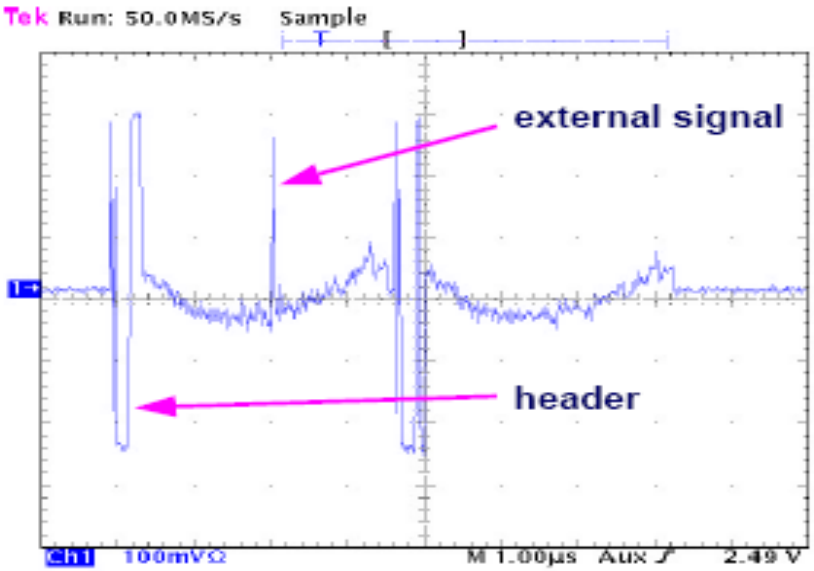


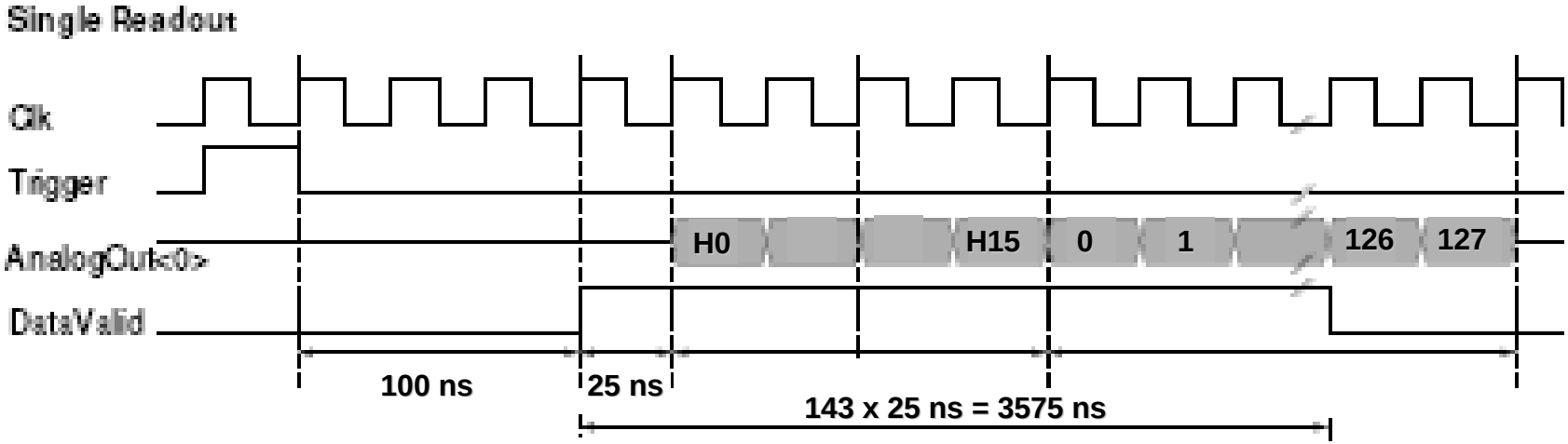
- Readout chip developed at ***ASIC laboratory of the University of Heildelberg.***
- Front-end output signal: this is the signal that will be reconstructed from analogue readout onto one port.
- This signal is sampled into the analogue pipeline (128x187 cells) with the frequency of the Beetle chip clock (40 MHz).
- V_p = kQ. T_p ~ 25 ns. Total pulse length about 65-70 ns.

- The analogue pipeline programmable latency will be fixed to 128 CLK cycles (3.2 μs).
- The TRIGGER signal will have to be active 128 CLK cycles (3.2 μs) after a particular front-end signal point of interest has been sampled.

BEETLE OUTPUT FORMAT

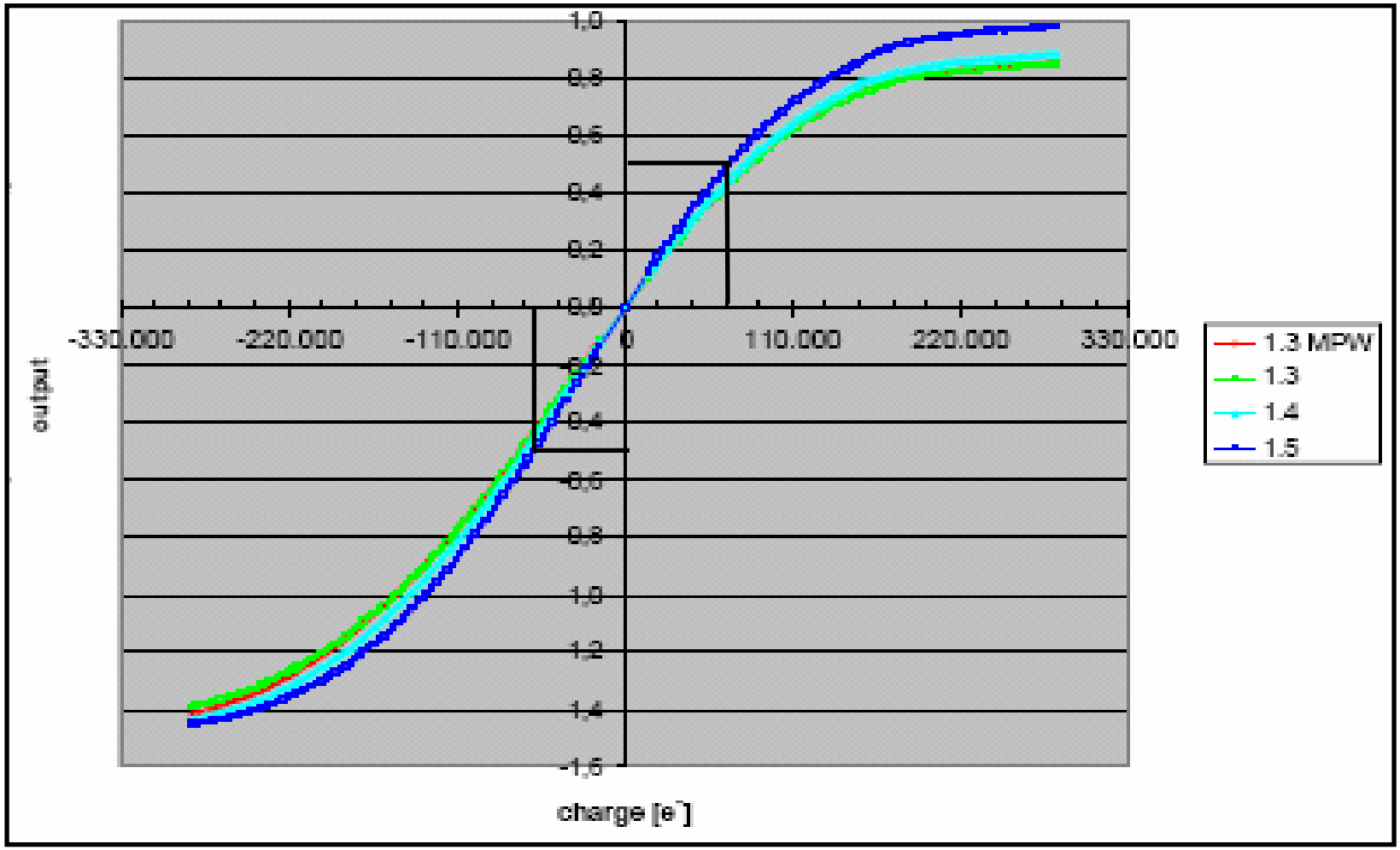
- Analogue output format: single readout.
- Readout: 16 bits header + 128 analogue multeplexed channels.
- Channel width of 25 ns.
- Datavalid signal for readout detection.



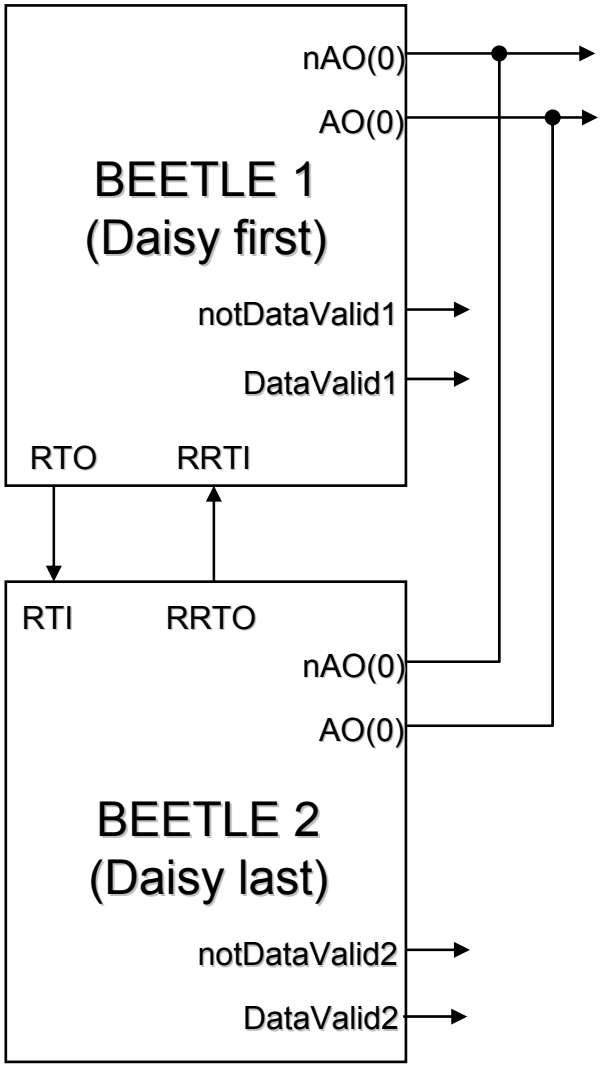


BEETLE OUTPUT FORMAT

- Output dynamic range: ±66000 e^- ~ ±500 mV.

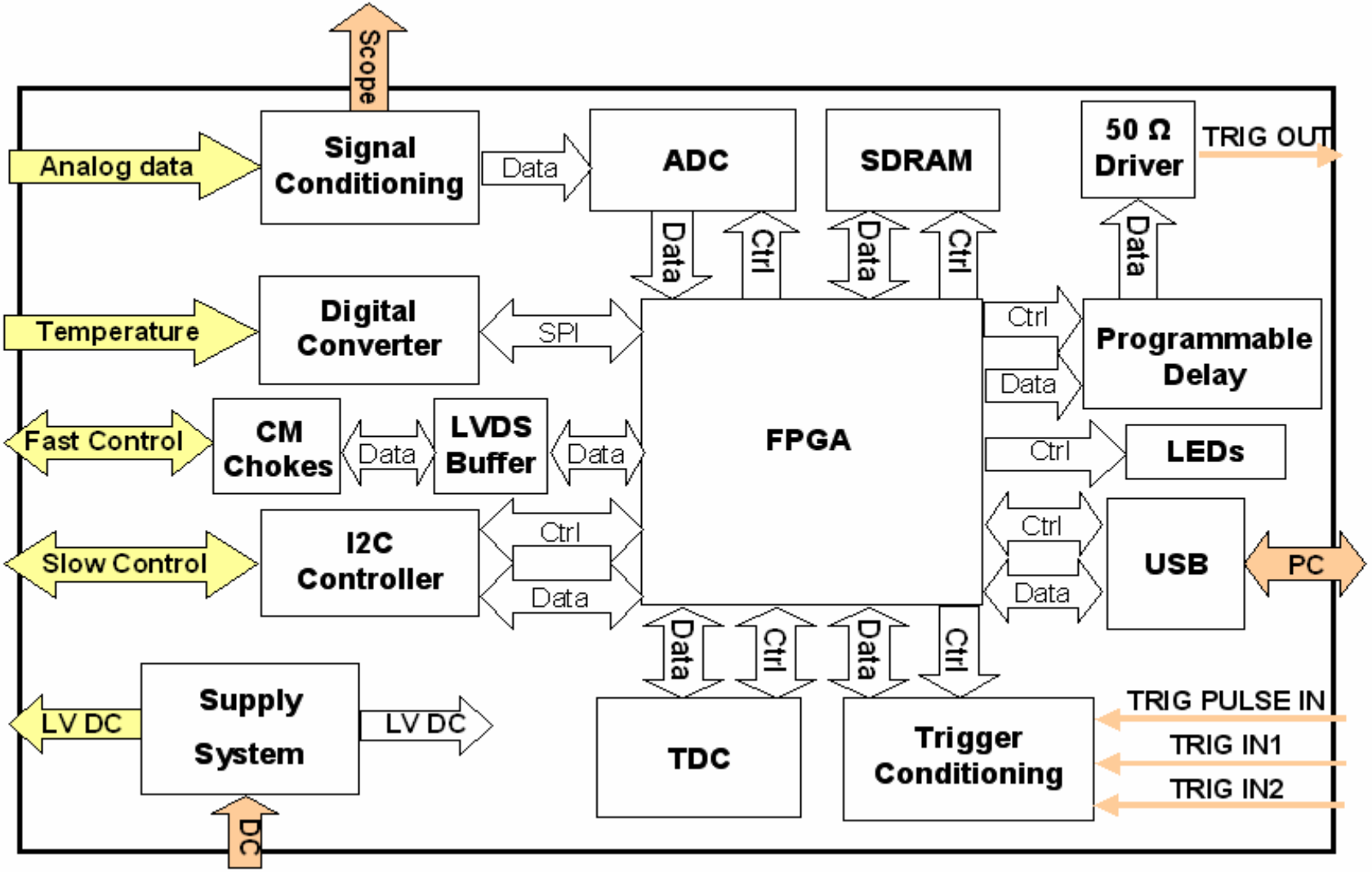


DAISY CHAIN CONFIGURATION



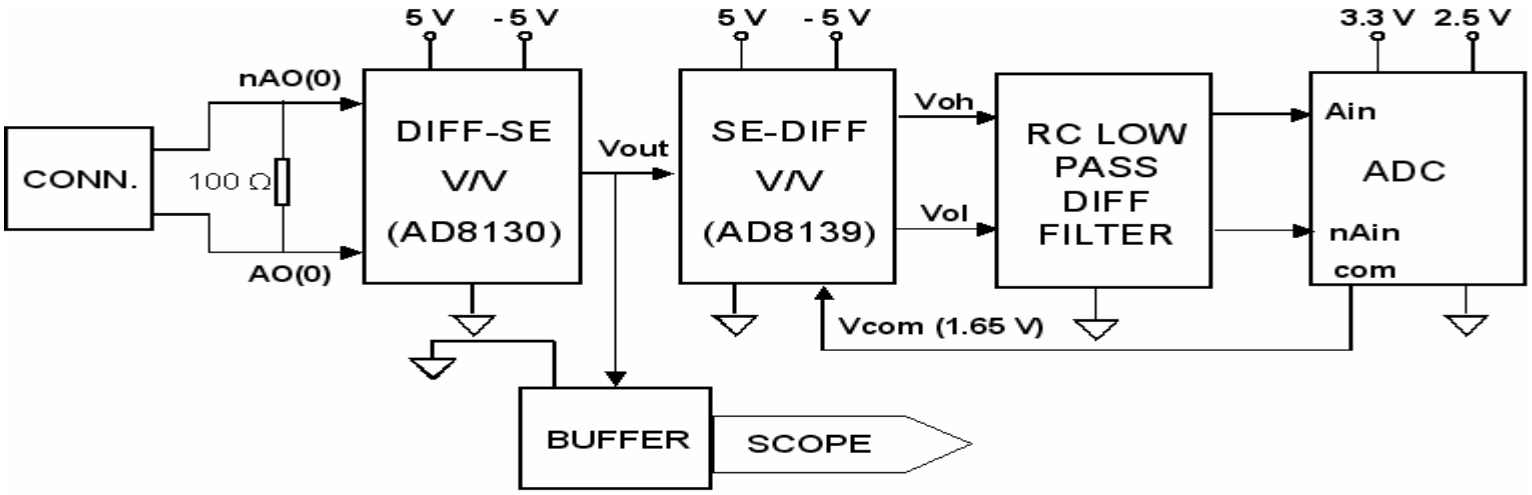
- It allows several chips to share the analogue output data lines.
- It consists of two signal paths, a token path (RTO, RTI) and a return token (RRTI, RRTO) path.
- The chip position in the chain has to be configured (slow control).
- Fast/slow control signals can be shared.

MB: BLOCK DIAGRAM



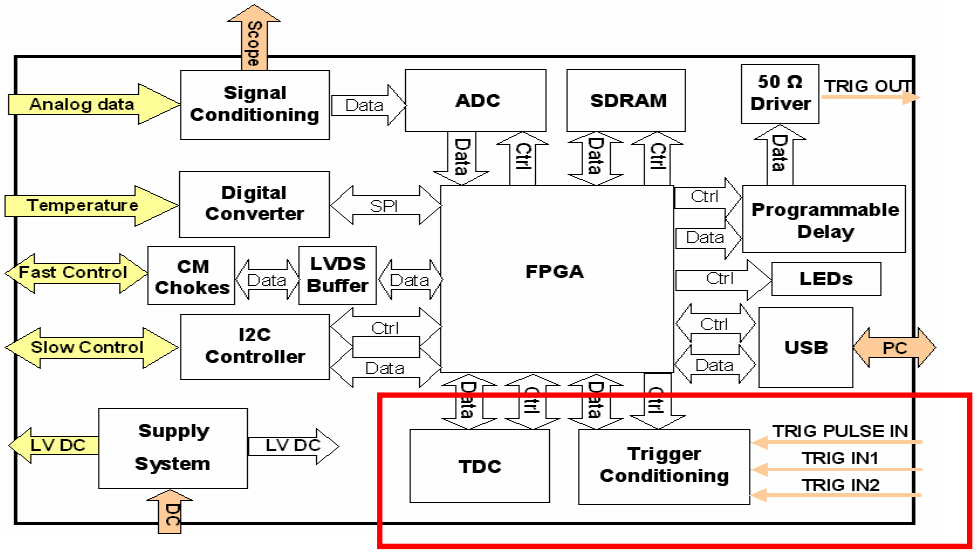
SIGNAL CONDITIONING/ADC

- The signal conditioning block is intended for transforming the differential voltage analogue input signal in order to:
  - Drive an oscilloscope which requires a single ended signal.
  - Drive an analogue to digital converter (ADC) which requires a differential input shifted signal.
- ADC:
  - 10 bit flash type with a sample rate of 40 MHz (MAX1448).
  - Nominal resolution of 2 mV (output signed code, 9 bits plus 1 sign bit).
  - Dynamic range will be ±512 mV.



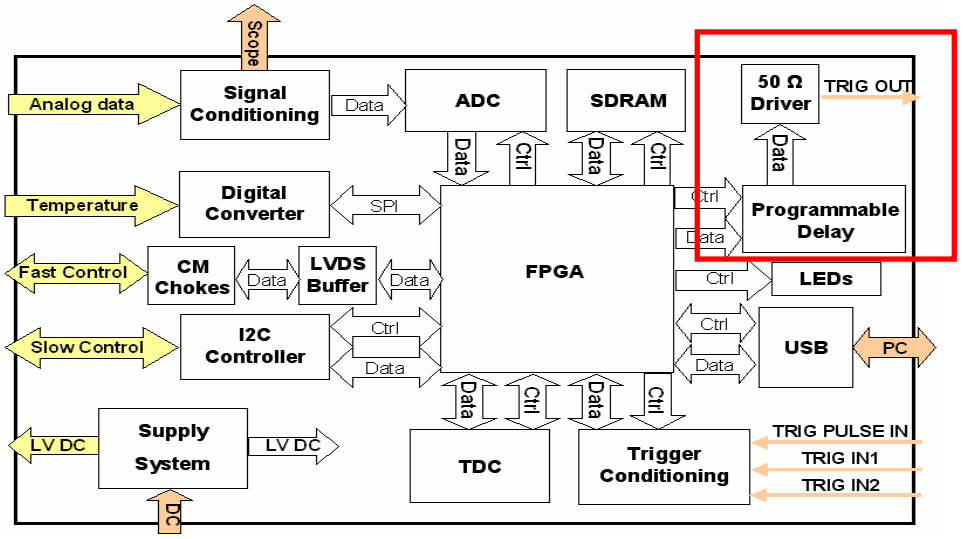
TRIGGER CONDITIONING-TDC

- In case of radioactive source setup for obtaining a time stamp of each trigger.
- Trigger conditioning:
  - Leading-edge discrimination of photomultiplier input signals.
  - Level conversion for an auxiliary signal.
  - Two dual LVPECL high speed comparators (MAX9601).
  - Four programmable voltage thresholds: generated with a quad 12 bits DAC (AD5582).
- TDC:
  - A TDC integrated circuit (TDC-GP1).
  - Nominal resolution: 600 ps.
  - 100 ns dynamic range.
  - Retrigger mode capability.



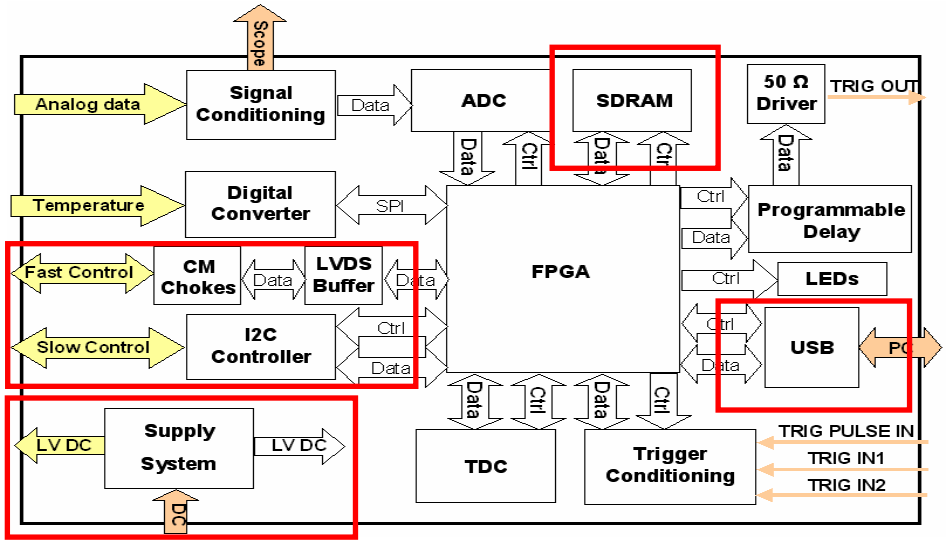
TRIGGER OUTPUT

- In case of laser setup.
- A synchronised trigger signal (TRIG OUT) will be generated to drive a laser source so that the pulse shape can be reconstructed.
- Programmable delay circuit (3D7428):
  - Resolution: 1 ns.
  - Range: up to 255 ns.
  - Programmed by FPGA by parallel interface (8 bits).
- Following this block a 50 Ω driver will be incorporated for driving a pulse generator input.



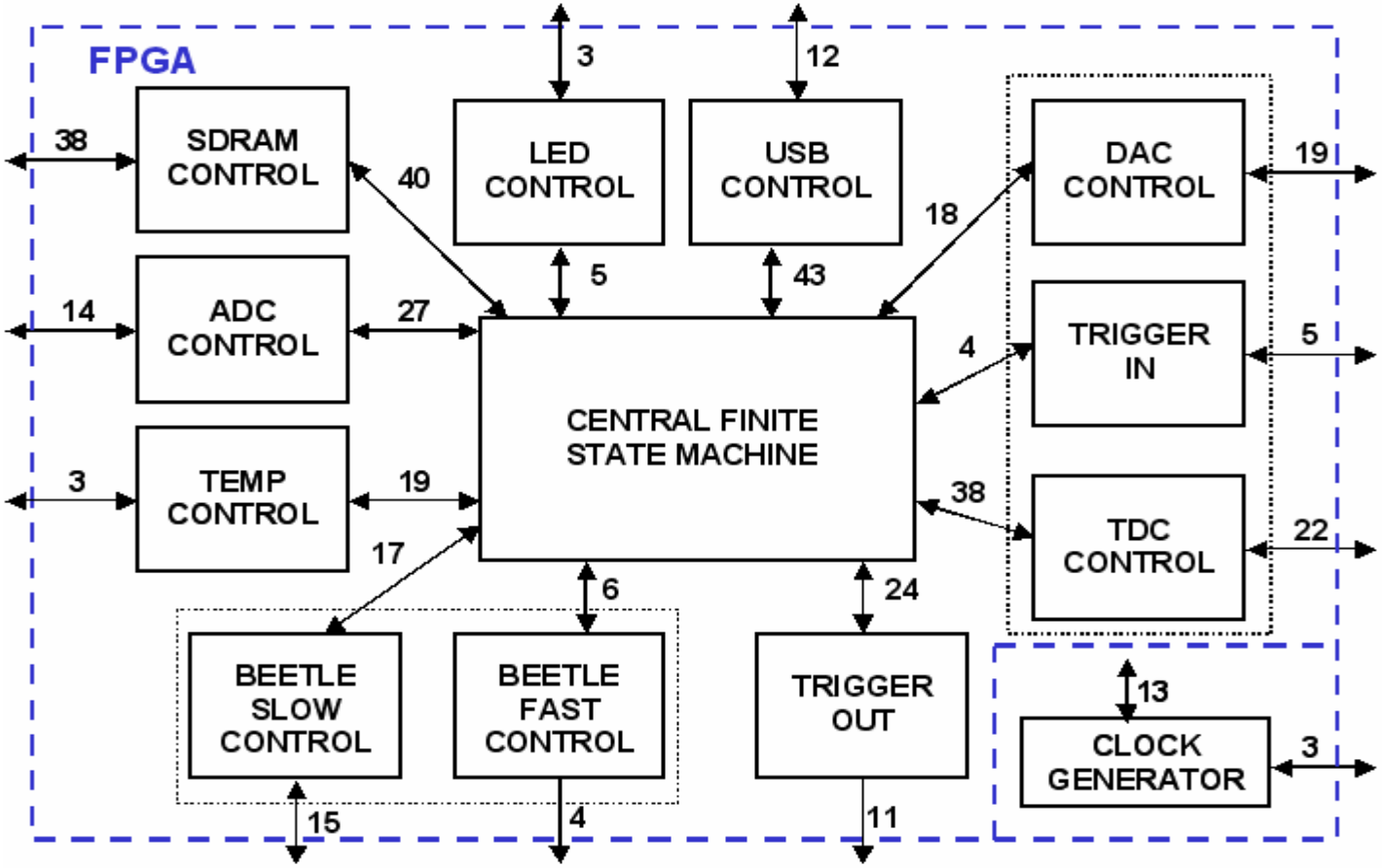
OTHER BLOCKS

- SDRAM (up to 512 Mb): for acquisition data storage.
- SLOW CONTROL: parallel (8 bits) to I2C controller (PCA9564).
- FAST CONTROL:
  - Two LVDS repeaters (DS90LV004).
  - Six CM noise suppressor chokes (23Z105SM).
- USB: USB controller (FT245R) for USB to FIFO parallel (8 bits) bidirectional data transfer.
- SUPPLY SYSTEM:
  - DC input from AC adapter.
  - Digital levels with 3 linear regulators.
  - Analogue levels from DC-DC converter + 3 linear regulators.
  - Daugther board level from DC-DC converter.



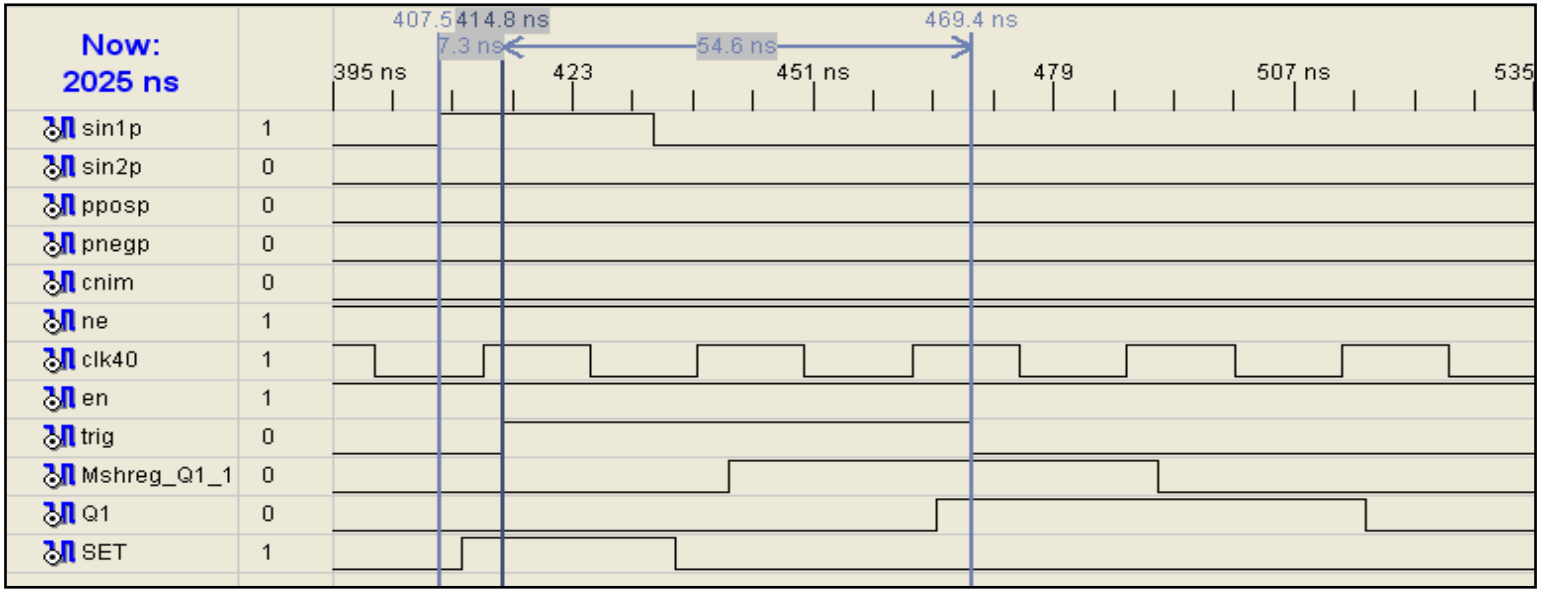
FPGA: BLOCK DIAGRAM

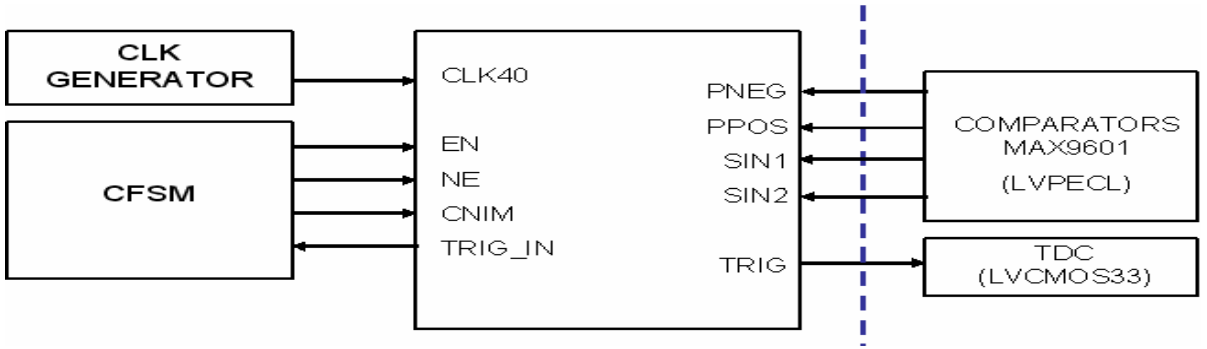
- Xilinx Spartan-3 clocked at 40 MHz.



TRIGGER IN SIMULATION

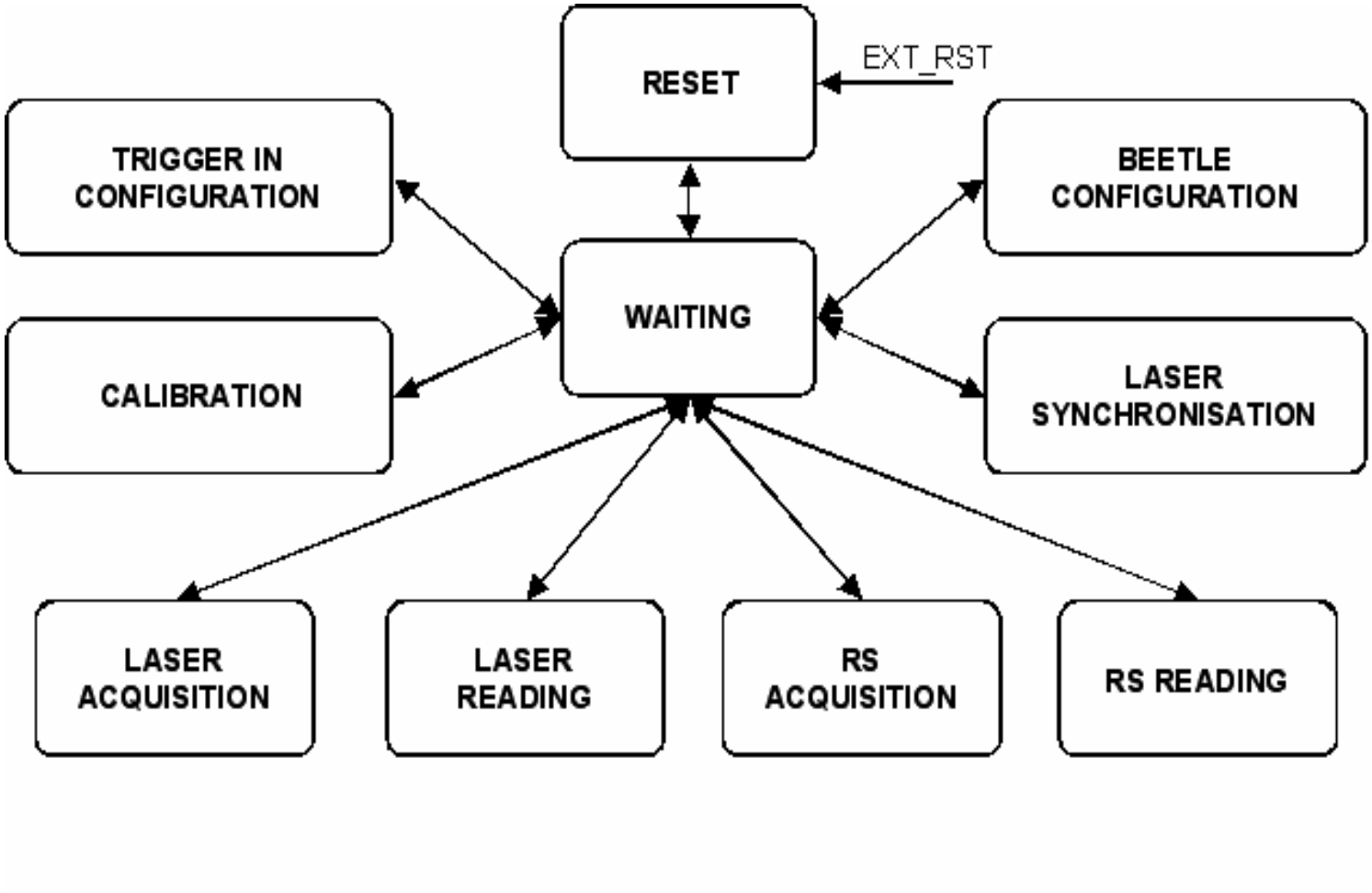
- IN1 input without coincidence (NE high). Post-Route simulation.





CFSM STATE DIAGRAM

- Possible system states.



CONCLUSION AND OUTLOOK

- A readout system for microstrip silicon sensors is being developed.
- The system is under development.
- The most of blocks of the mother board and some of the FPGA have already been designed and simulated.
- After the design will be finished, different blocks of the system will be tested with a FPGA development board and custom boards which will integrate some of these blocks.
- Finally, prototypes of the daughter board and the mother board will be manufactured and tested together.
- The software part of the system will be designed in parallel with the hardware part.
- A reduced version of this software will be used for testing the different blocks of the mother board with the development board.

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BEETLE ARCHITECTURE

- Readout chip for the microstrip silicon sensor data acquisition.
- Front-end: CSA+Shaper+Buffer (128 channels).
- A comparator per channel can provide a binary signal.
- Analogue pipeline: 128x187 cells.
- Output Stage: CSA+Multiplexer.
- Slow control: chip configuration via I2C.
- Fast control (LVDS): Clk (40 MHz), Reset, Trigger, Testpulse and DataValid.
- Binary/analogue output (through analogue pipeline) or digital output (LVDS).

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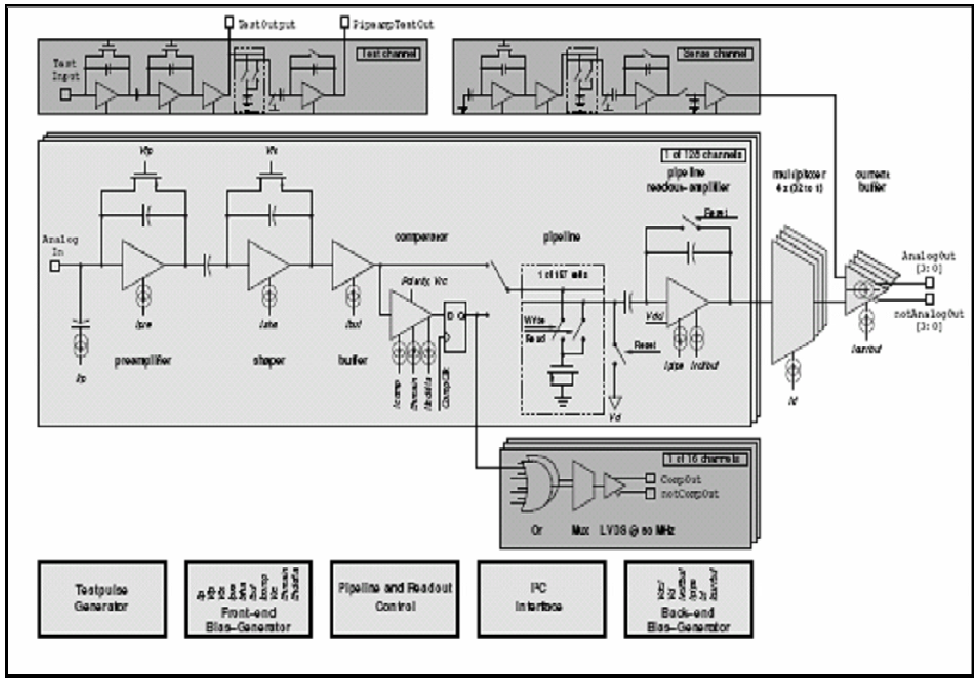
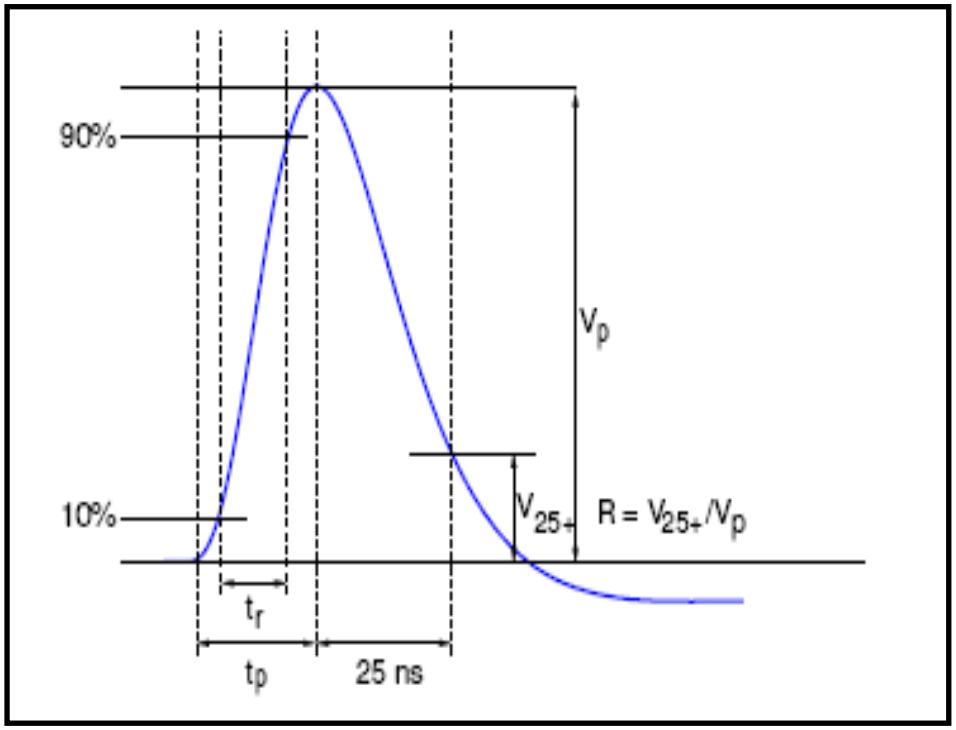


BEETLE IN THE SYSTEM

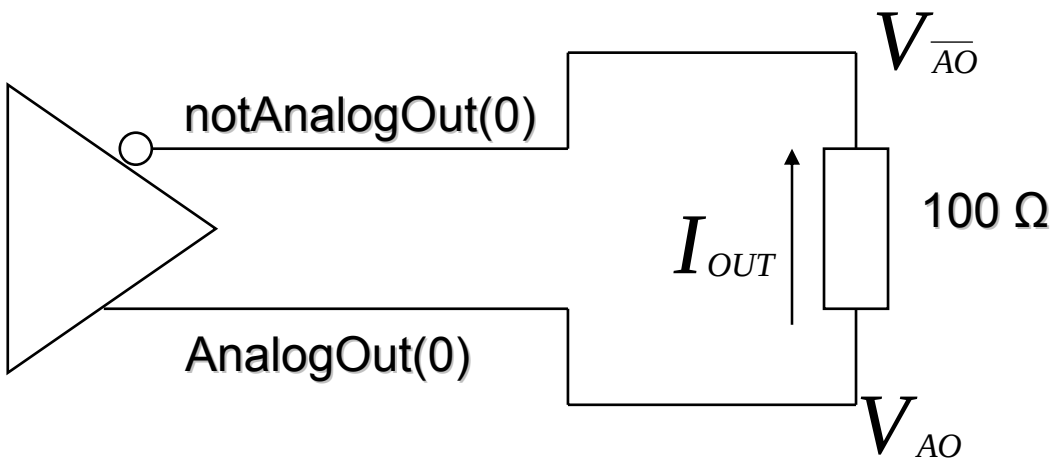


- Front-end output signal: this is the signal that will be reconstructed from analogue readout onto one port.
- This signal is sampled into the pipeline with the frequency of the Beetle chip clock (40 MHz).
- V_p = kQ.
- t_p ~ 25 ns. Total pulse length about 65-70 ns.
- The analogue pipeline programmable latency will be fixed to 128 CLK cycles (3.2 µs).

- The TRIGGER signal will have to be active 128 CLK cycles (3.2 µs) after a particular front-end signal point of interest has been sampled.
- The TESTPULSE signal is intended for activating the internal pulse generator for each input channel in order to calibrate the system.

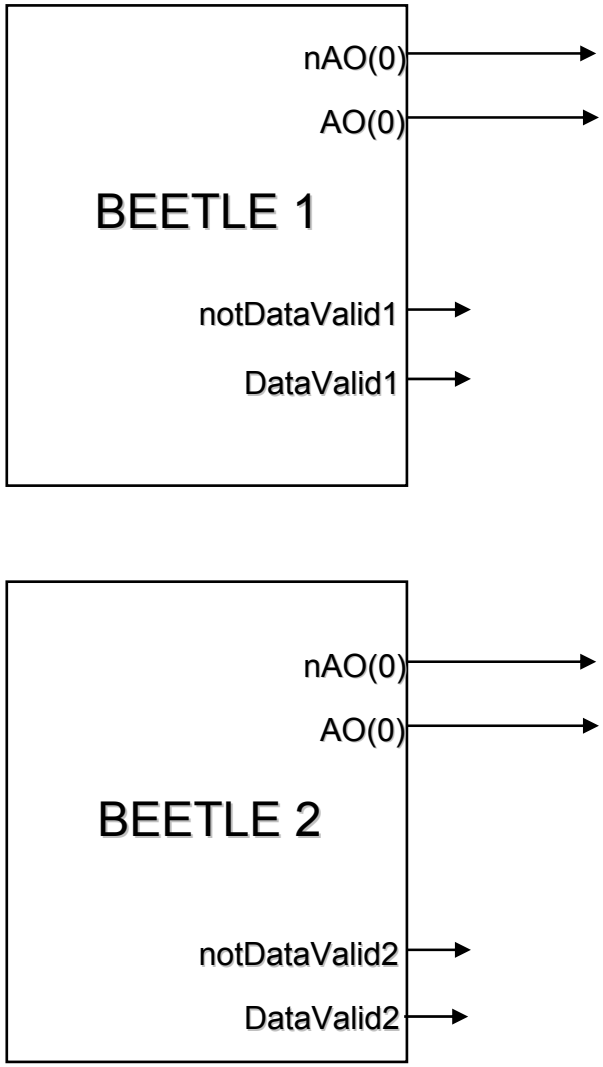
BEETLE IN THE SYSTEM

- Output buffer is a current buffer: voltage values measured over 100 Ω (for closing the loop).
- This differential voltage output will be buffered with a differential to differential unity gain voltage amplifier for sending it to the mother board.



		BinaryHeader: OFF CompDisable: ON PipelineMode: OFF		
		V_{AO} [mV]	$V_{\overline{AO}}$ [mV]	I_{out} [mA]
baseline		973	978	-0.05
header	high	916	1058	-1.42
	low	1014	912	1.29
binary	high	analogue readout		
	low			

PARALLEL CONFIGURATION



- The analogue output data lines cannot be shared.
- Buffer (DB), analogue signal processing, ADC and ADC control logic must be duplicated (two output data paths).
- Fast/slow control can be shared on both configurations.

TRIGGER CONDITIONING-TDC

- In case of radioactive source setup.
- Trigger conditioning:
  - TRIG IN1 and TRIG IN2: input signals from photomultipliers.
  - TRIG PULSE IN: positive/negative voltage pulse up to ±5V or fast negative NIM pulse.
  - Four signals will be generated in LVPECL indicating if TRIG IN1 or TRIG IN2 is active (with a leading edge discriminator per signal), or if a negative or a positive pulse have been received on TRIG PULSE IN (with two discriminators).
  - The four discriminators will be implemented with two dual LVPECL high speed comparators.
  - Four programmable voltage thresholds: generated with a quad 12 bits DAC.
- TDC:
  - This block will be composed only of a TDC integrated circuit with a resolution of 600 ps approximately.
  - It will measure the time passed between a start signal generated every 100 ns (time window for reconstructing an 75 ns long front end pulse) and a trigger signal generated if TRIG IN1 and/or TRIG IN2 are active, or TRIG PULSE IN are active.

TRIGGER OUTPUT

- In case of laser setup.
- A synchronised trigger signal (TRIG OUT) will be generated to drive a laser source so that the pulse shape will be able to be reconstructed.
- For this reason a digital programmable delay circuit will be used in order to delay the TRIG OUT signal.
- With this circuit TRIG OUT will be able to be delayed up to 75 ns in 1 ns steps by a 8 bits parallel programming code from the FPGA.
- Following this block a 50 Ω driver will be incorporated for driving a pulse generator input that will pulse the laser source.

OTHER MB BLOCKS

- Fast control (LVDS):
  - The FPGA will generate directly the output signals (CLK, TESTPULSE, TRIGGER and RESET) in LVDS format.
  - To protect the FPGA these signals will be buffered with two LVDS repeaters, one for the output signals to the daughter board (CLK, TESTPULSE, TRIGGER and RESET) and another one for the input signals from the daughter board (DATAVALID1 and DATAVALID2).
  - Also a common mode noise suppressor choke will be provided for each signal.
- Slow control: the slow control signals (SCL and SDA) will be generated by the I2C controller block from the 8 bits parallel code generated in the FPGA.
- SDRAM (up to 512 Mb): temporally store the digitized data in each acquisition prior to be read by the software.

OTHER MB BLOCKS

- Digital converter (temperature):
  - The thermistor signal coming from the daughter board will be digitized at the digital converter block by a digital converter circuit.
  - It will measure the voltage across the thermistor and will produce a 10 bits plus sign output code.
  - It will have a serial interface with the FPGA.
- USB block:
  - This block will have a USB controller for USB to FIFO parallel (8 bits) bidirectional data transfer.
  - The manufacturer of this controller also supplies the software drivers for interfacing the controller on the PC software.
- Supply system: centralized on the mother board.
  - A DC input level will be generated with a portable AC adapter.
  - From this DC level the mother board digital levels (1.2 V, 2.5 V and 3.3 V) will be generated by means of LDO linear regulators.
  - The mother board analogue levels (5 V, -5 V and 3.3 V) will be generated by a DC-DC converter and LDO linear regulators.
  - The daughter board supply level (3.3 V) will be generated by a DC-DC converter.

FPGA BLOCKS

- The slow control block will control the parallel bus to I2C-bus controller in order to program the Beetle configuration registers.
- Fast control (CLK, RESET, TRIGGER, TESPULSE):
  - The TESTPULSE will be generated from an internal calibration signal to trigger the Beetle internal pulse generator.
  - The TRIGGER signal will be generated from an internal TRIG_L signal (in case of laser setup) or from an internal TRIG_IN signal (in case of radioactive source setup) taking into account both the Beetle analogue pipeline latency and the particular synchronization delay.
- The ADC block:
  - It will control the ADC.
  - It will read the digitized data frames by the ADC when the DATAVALID signal will be active.
  - It will store these frames in an internal FIFO RAM.
- The SDRAM control block:
  - It will control the SDRAM.
  - It will implement the read/write data and control interface with the CFSM block.
  - Both the digitized data from Beetle chips (256 by 16 bits per two chips readout) and the TDC data (32 bits per readout) will be able to be stored.

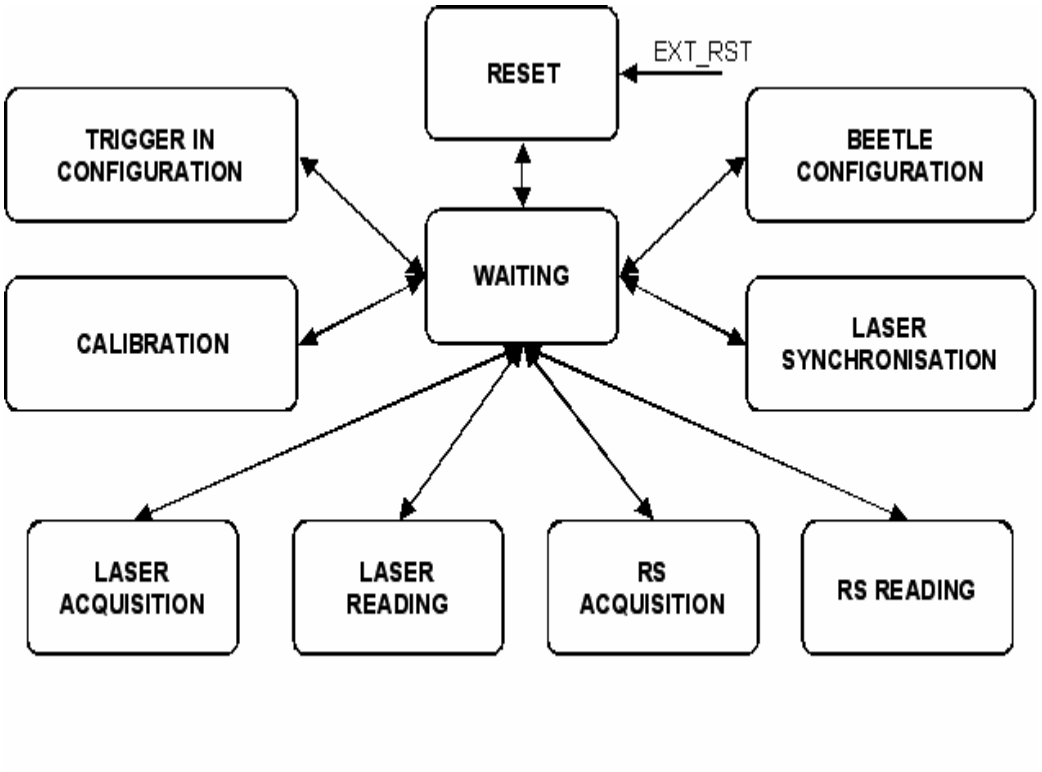
FPGA BLOCKS

- The trigger out block (laser setup):
  - It will produce an external trigger signal (TRIG OUT) that will be periodic (1 KHz) and an internal trigger signal (TRIG_L) for the Beetle fast control block.
  - With these signals the pulse shape at the Beetle chips front end will be sampled in 1 ns intervals from its beginning till its end (that is 100 ns).
- The trigger in block (radioactive source setup)
  - It will generate an external and internal trigger signal (TRIG and TRIG IN, respectively) from signals SIN1 and/or SIN2 (discriminated signals from two photomultipliers), PPOS (external positive pulse) or PNEG (external negative pulse) coming from the trigger conditioning block.
  - The coincidence of SIN1 and SIN2 as well as which inputs will be used will be able to be programmed.
- The DAC control block (radioactive source setup) will control the DAC that will supply the four voltage thresholds for the trigger conditioning comparators.
- The TDC control block (radioactive source setup) :
  - It will control the TDC, which will measure the time from a START signal leading edge (100 ns periodic signal internally generated) to the TRIG signal leading edge.
  - It will also generate a TRIG_R signal (for the Beetle fast trigger control) related in time to the TRIG signal when the last will be active.

FPGA BLOCKS

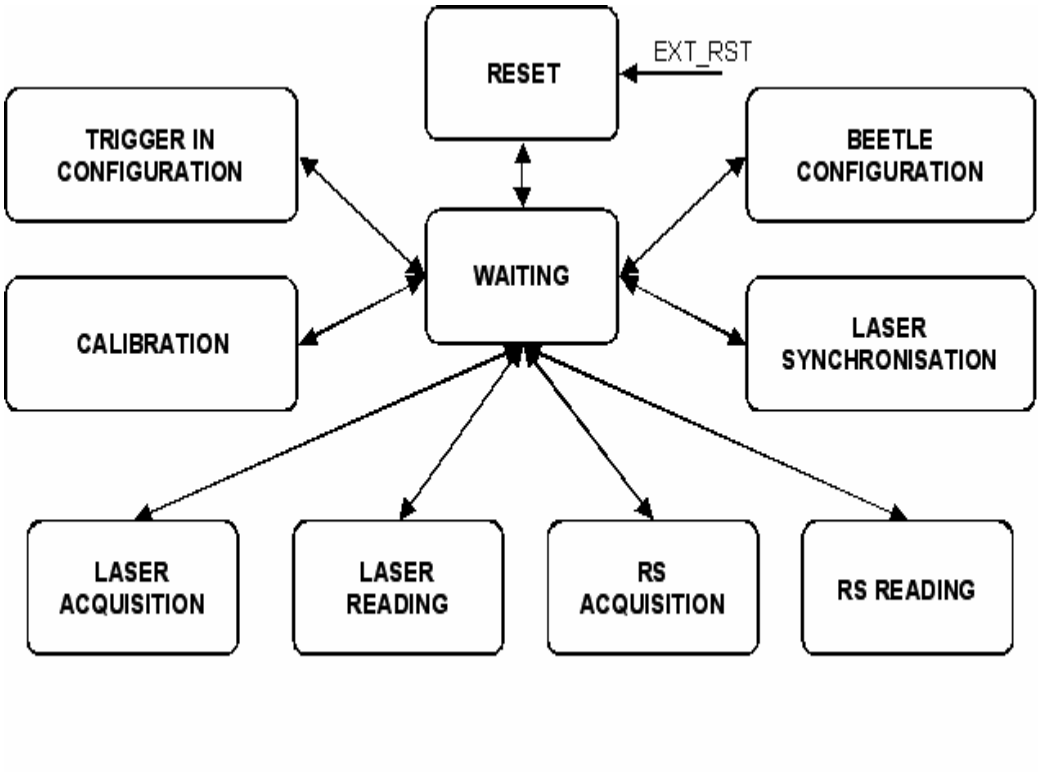
- The USB control will have to control the USB chip and to implement the data input/output and control interface with the CFSM.
- The temperature control block will read the digital conversion of the thermistor signal from the digital converter by serial interface.
- The LED control block:
  - It will activate a red LED, yellow LED or green LED depending on its input code value.
  - This will be used to show to the user the state of the system.
- The clock generator block will supply the FPGA internal clock signals and the SDRAM clock signal.
- The CFSM (Central Finite State Machine) block:
  - It will control the system hardware part by interpreting the orders that the system software part (PC software) will send by USB.
  - Depending on the current state the CFSM will use different blocks and it will enable the communication among those blocks.

CFSM STATE DIAGRAM



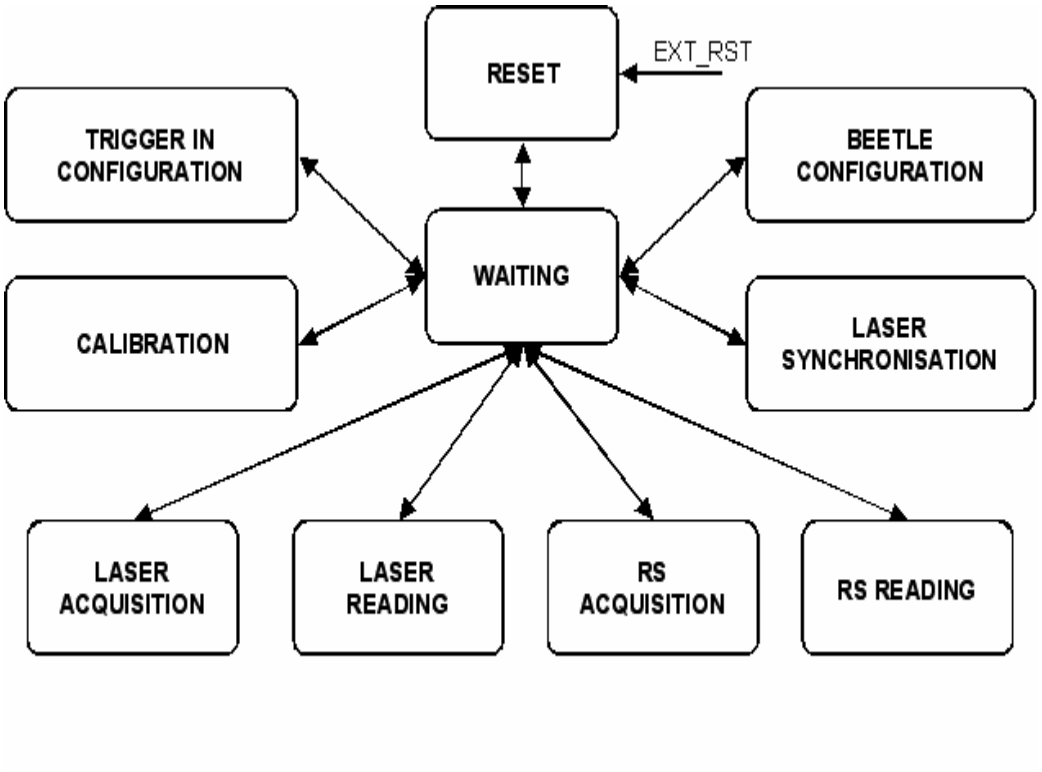
- RESET:
  - System initialization.
  - On a power on, with an external reset or by a software reset.
- WAITING:
  - The system will wait for an order coming from the PC software to go to another state.
- BEETLE CONFIGURATION:
  - Beetle chips configuration registers programming.
- CALIBRATION:
  - System calibration by the Beetle internal test pulse generator
  - Known amplitude readouts will be acquired in order to have the calibration data.

CFSM STATE DIAGRAM



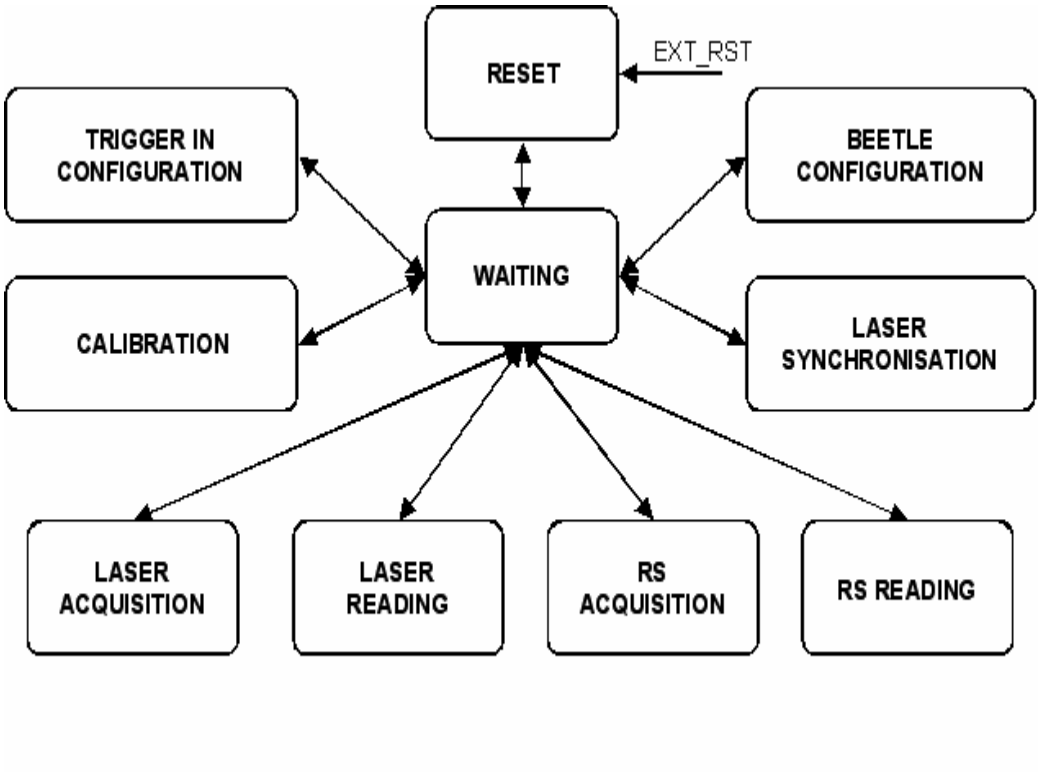
- TRIGGER IN CONFIGURATION:
  - DAC voltage thresholds will be programmed
  - Trigger inputs scheme will be configured.
- LASER SYHRONIZATION:
  - The system will be synchronized for the Beetle front end pulse reconstruction.
  - By delaying the TRIG OUT signal 100 ns in 1 ns steps.

CFSM STATE DIAGRAM



- LASER ACQUISITION:
  - A hundred of readouts will be acquired for each 1 ns step that TRIG OUT will be delayed.
  - So 10000 readouts (100 ns time window) will be acquired and stored in the SDRAM.
  - The TRIG OUT frequency will be 1 KHz.
  - A temperature readout will be acquired and stored in this state as well.
- LASER READING:
  - The last laser acquisition will be read from SDRAM and data will be sent to PC.

CFSM STATE DIAGRAM



- RS ACQUISITION:
  - A programmable number of readouts will be able to be acquired.
  - For each event a Beetle chips readout (256 by 16 bits) and a TDC readout (32 bits) will be stored in the SDRAM.
  - Two temperature readouts, before and after the acquisition, will be stored as well.
- RS READING:
  - The last RS acquisition will be read from SDRAM and data will be sent to PC.