

On the development of the final optical multiplexer board prototype for the TileCal experiment

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This presentation aims to describe the architecture of the final optical multiplexer board (also known as preROD) for the TileCal experiment. The results of the first VME 6U prototype have led to the definition of the final block diagram and functionality of this prototype. Functional description of constituent blocks and the state of the work currently undergoing at the Department of Electronic Engineering is presented. As no board is still produced, no results are presented but, nevertheless, design issues that has been taking into account as component placement and signal integrity issues will be detailed.

Summary

1. INTRODUCTION

The Optical Multiplexer Board (OMB), also known as PreROD, will be the module which will decide which of the two optical fibers coming from the Front-End (FE) electronics of the TileCal detector carry error-free data. This is necessary because radiation inside the detector can produce malfunctioning of the digital circuits of the FE. To solve this problem two optical fibers come out from the FE carrying the same data. Should radiation produce any error, the OMB will detect it by checking the CRC codes for the data packet and select the error-free fiber.

A first prototype of this OMB is already functioning and used for ROD commissioning tasks. This prototype only includes two input channels (4 input fibers) and two output channels (2 fibers) and is implemented in a VME 6U board. A brief description of this board is presented in the next section.

1. OMB 6U prototype

The basic building blocks of the 6U prototype are:
- the VME slave controller
it operates the whole board, keeping records on the number of errors detected in each channel, and sets its working mode which can be normal or

injection. This second mode allows the OMB to inject data blocks either automatically or previously loaded from VME.

- the CRC and link controller it holds two input and one output high-speed link controller and the CRC algorithm calculation and checking logic. It's connected to the VME controller for control and debug operations.

The prototype has two CRC and link controller blocks, one per input channel, and one VME slave controller.

One of the most interesting functionality of the board, provided the TileCal detector is not yet built, is the injection mode. With this mode it has been possible to carry out ROD commissioning tasks at Valencia thanks to the possibility of injecting known data blocks and the selection of trigger inputs, either internally generated or input from NIM logic.

1. OMB 9U description and current work

The good results achieved from the 6U experience are being now used to define the final OMB prototype. This prototype is conceived in a 1 to 1 ratio with respect to RODs. This is to say that each final prototype will have 8 input channels (16 fibers) and 8 output channels (8 fibers). Due to this modification a 9U format has been chosen for this new implementation.

With respect to functionality there are some minor modifications among of which, the inclusion of the TTC receiver chip is the main one. This would lead to the possibility of having trigger directly from the TTC system, something which is not possible now.

Electrically speaking the new board poses some problems related to signal integrity and component placement issues. The use of a single JTAG chain for the programming of all the FPGA chips in the board and the bus connecting the VME controller and the CRC controllers are the main issues. Simulation of this connections as well as firmware modification in the FPGA used are part of the work currently going on and that will be included in the presentation.

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