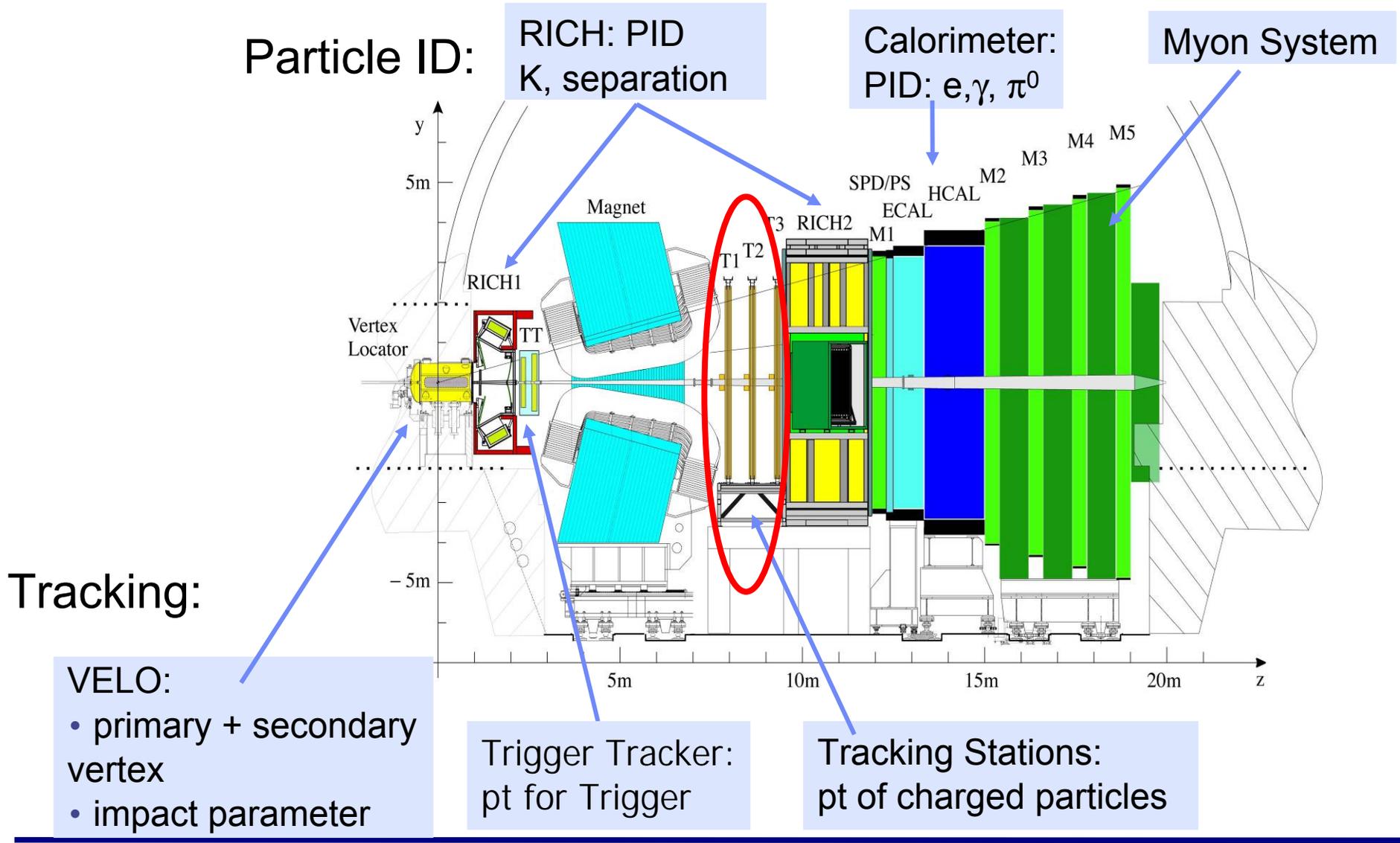
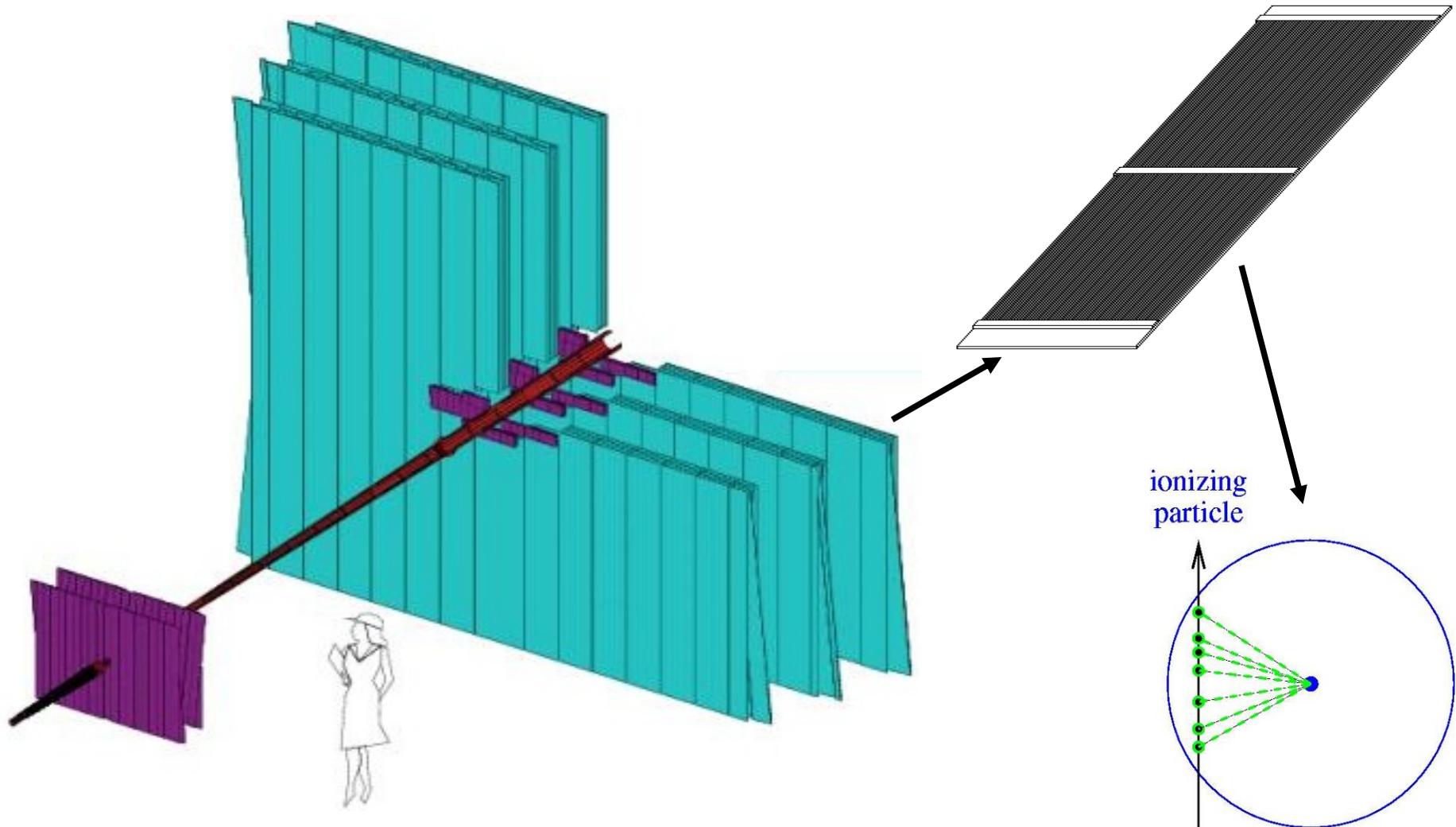


The readout system for the LHCb Outer Tracker

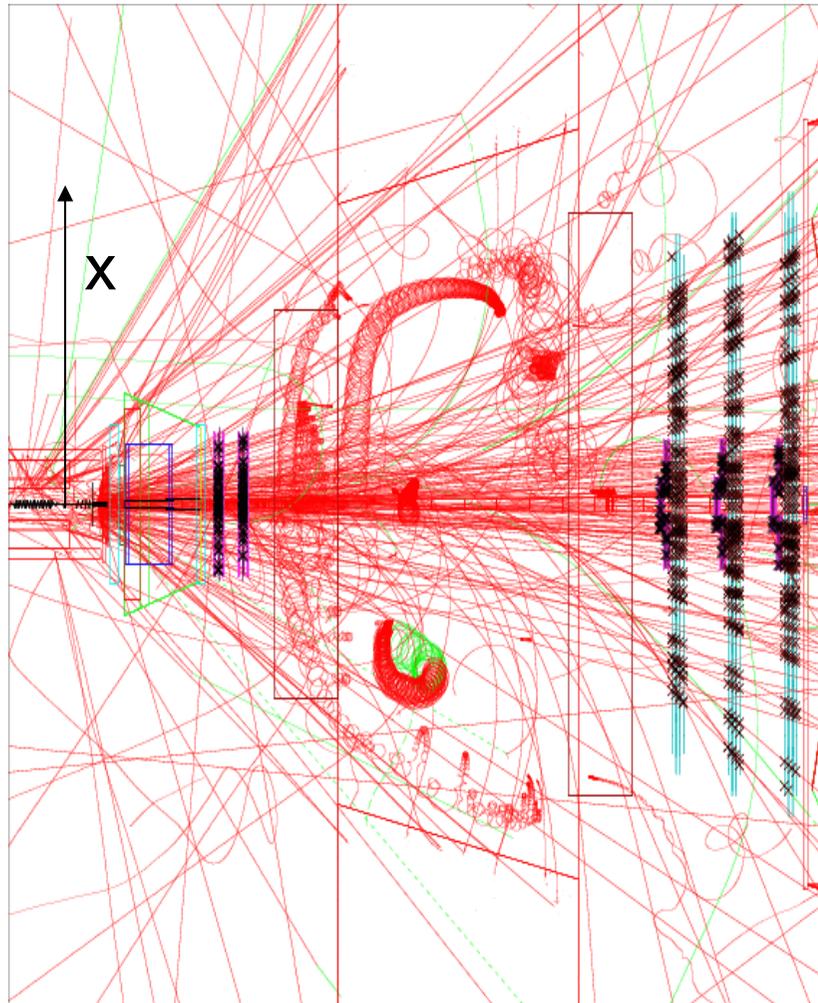
LHCb



Outer Tracker

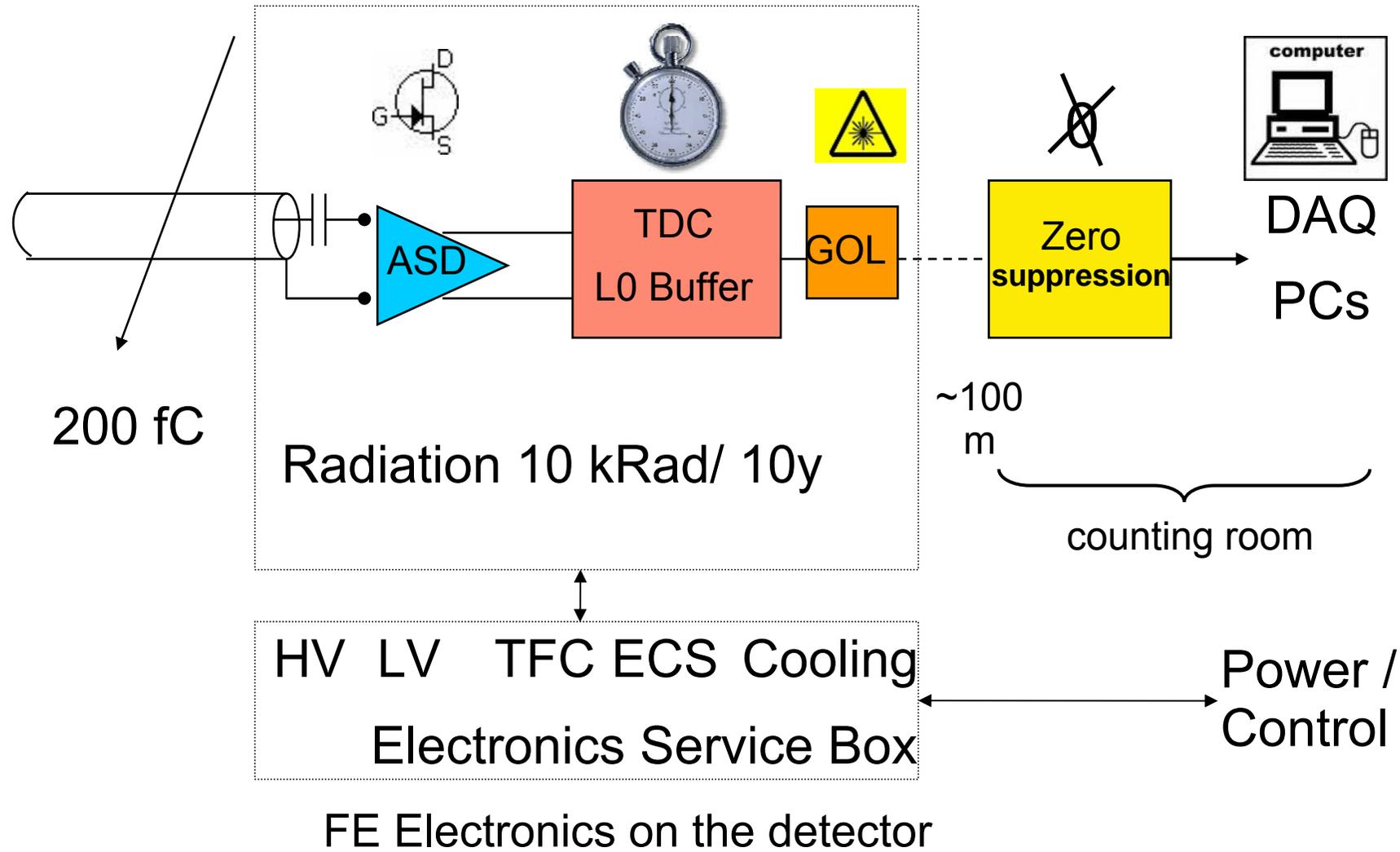


Requirements



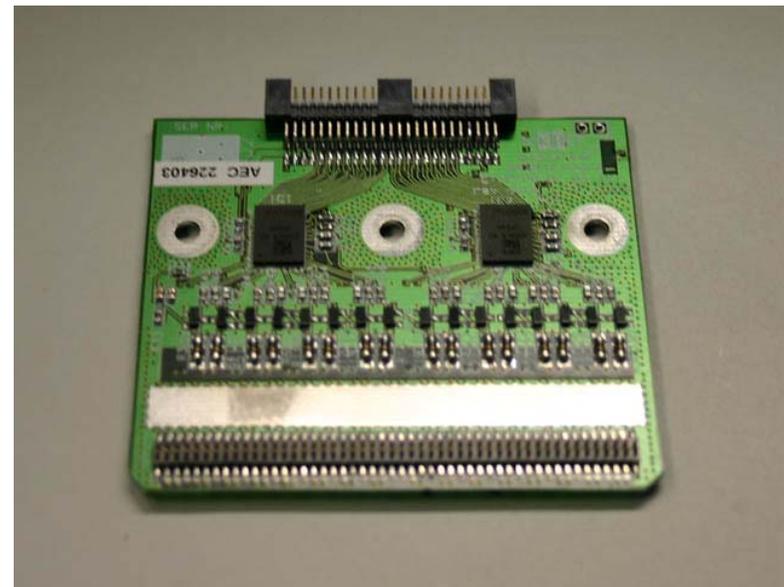
- 40 MHz collision rate
 - Reference Frequency
- In average one interaction every 25 ns
- 1.1 MHz readout
- B hadron production rate around 75 kHz
- Radiation tolerance 10 kRad
- Resolution
 - $\delta p/p = 0.4\%$ (20 GeV particle)
 - 200 nm in x
 - 1 ns drift time resolution

Outer Tracker FE Electronics

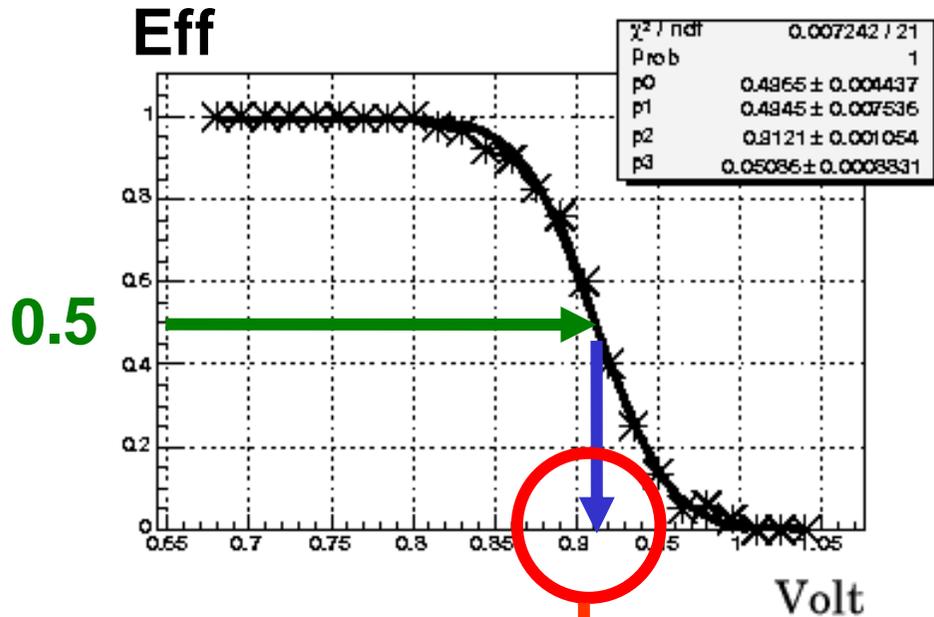


Amplifier

- ASDBLR (ATLAS DEMILL)
- Amplifier with around 12 ns shaping time
- 2x 8 Channels per board



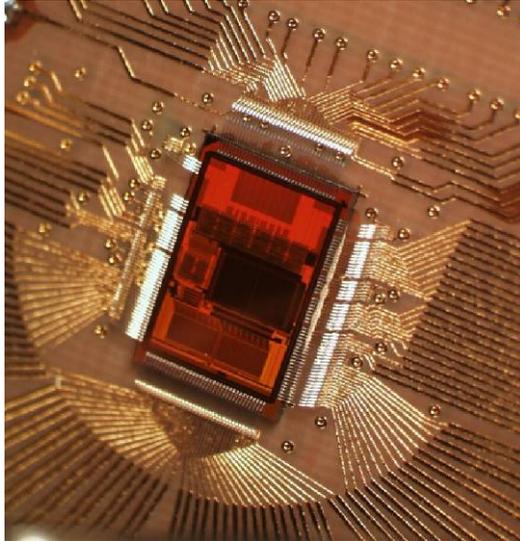
ASDBLR Testing



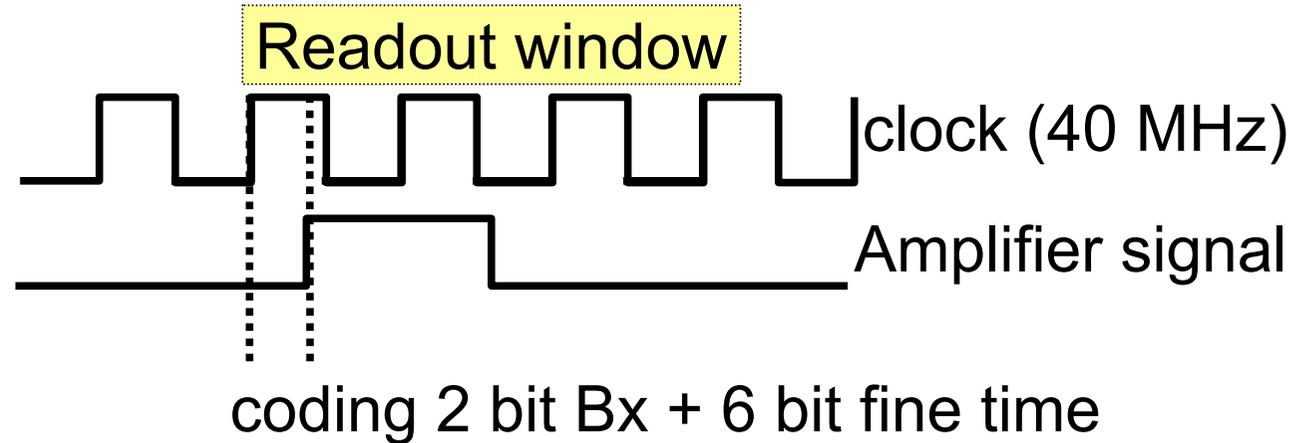
Half Efficiency
 $V_{thr}^{[50\%]}$

- Chips categorized:
- pre-selection:
 - current consumption
 - broken channels etc.
 - → 62.2% accepted
- performance:
 - threshold spread checked
 - → 32 % best chips chosen

TDC (OTIS*)



TDC = Time to Digital Converter



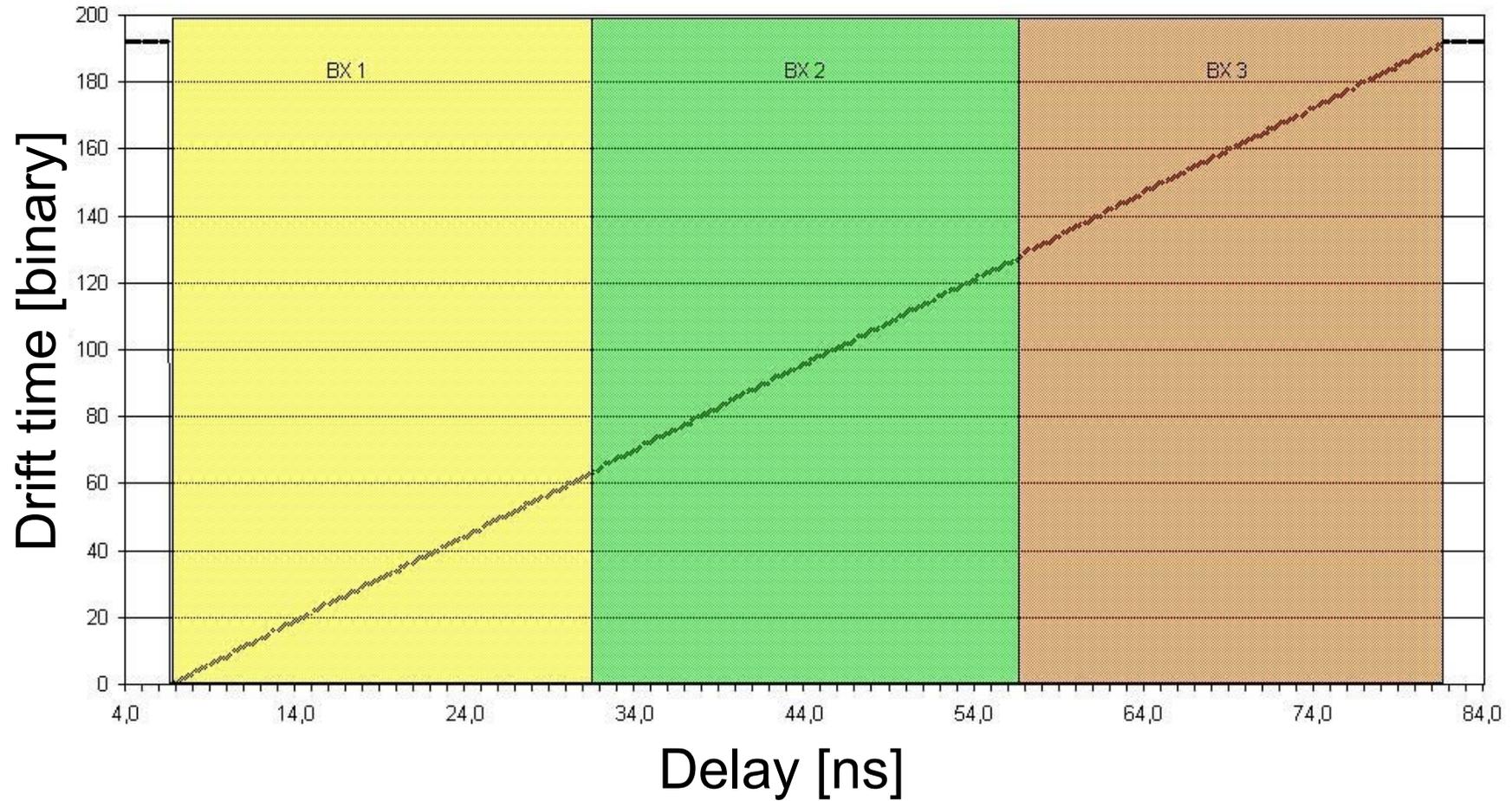
- ▶ 32 channel TDC
- ▶ one time bin is $25 \text{ ns} / 64 \approx 390 \text{ ps}$
- ▶ time reference is rising edge of LHC clock
- ▶ Read out window: 75 ns

*Outer Tracker Time Information System

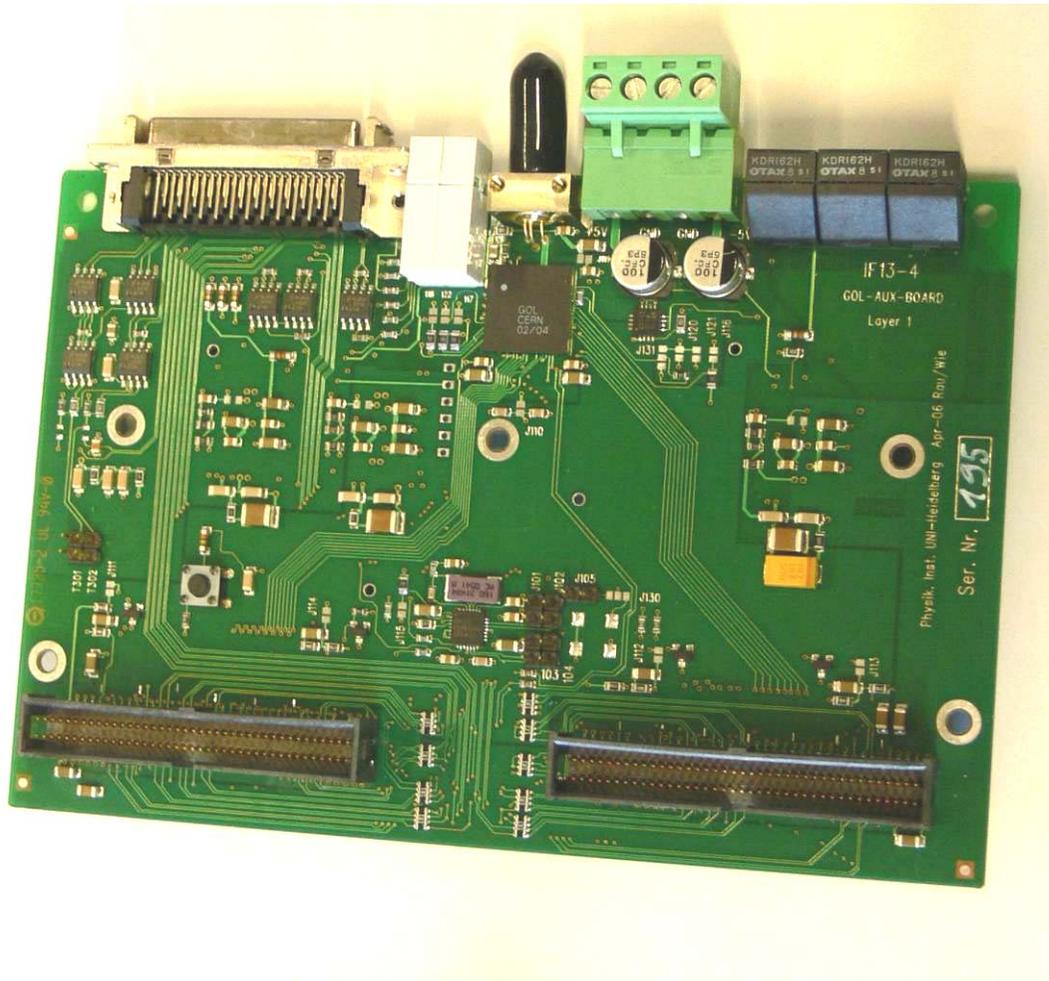
TDC linearity

OTIS1.2 Drift Time Scan

Single Hit Mode, 3BX per Trigger, Channel 15



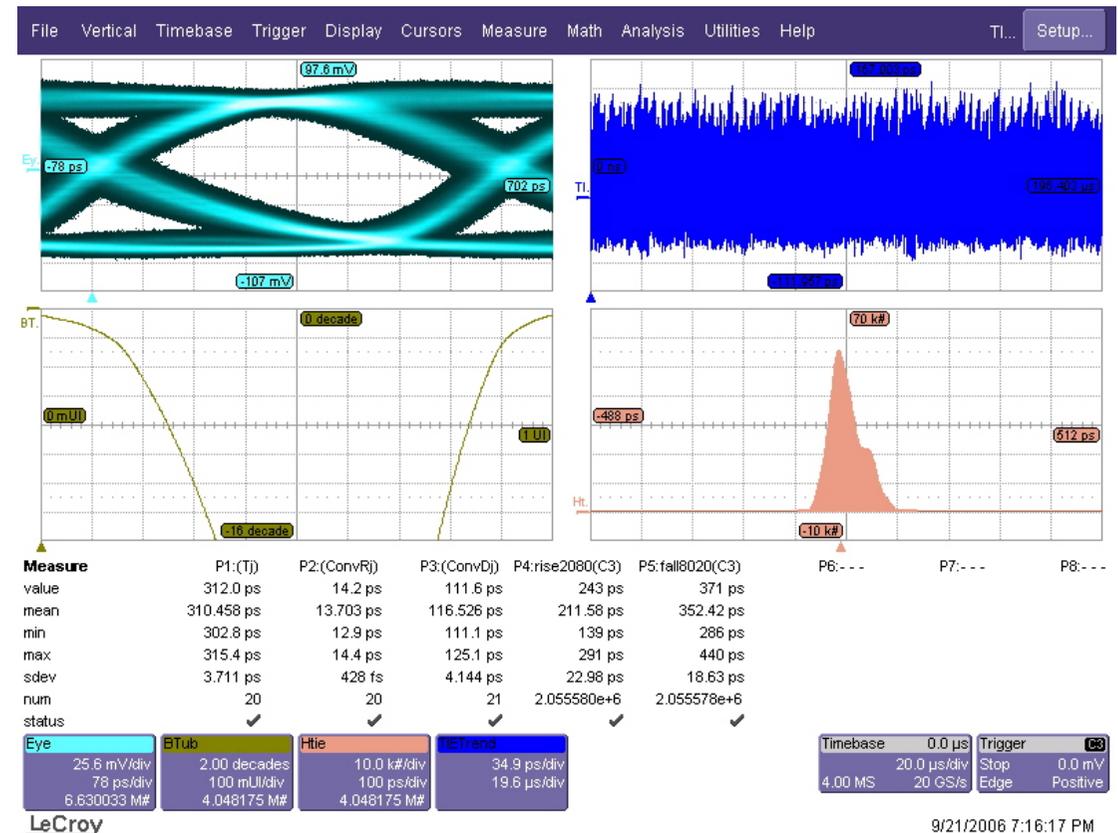
Gigabit Optical Link board



- 1.6 Gbit/s output
- 1 fibre per 128 channels
- Fast and slow control distribution
- Jitter filter (≤ 7 ps RMS)
- Low voltage regulators

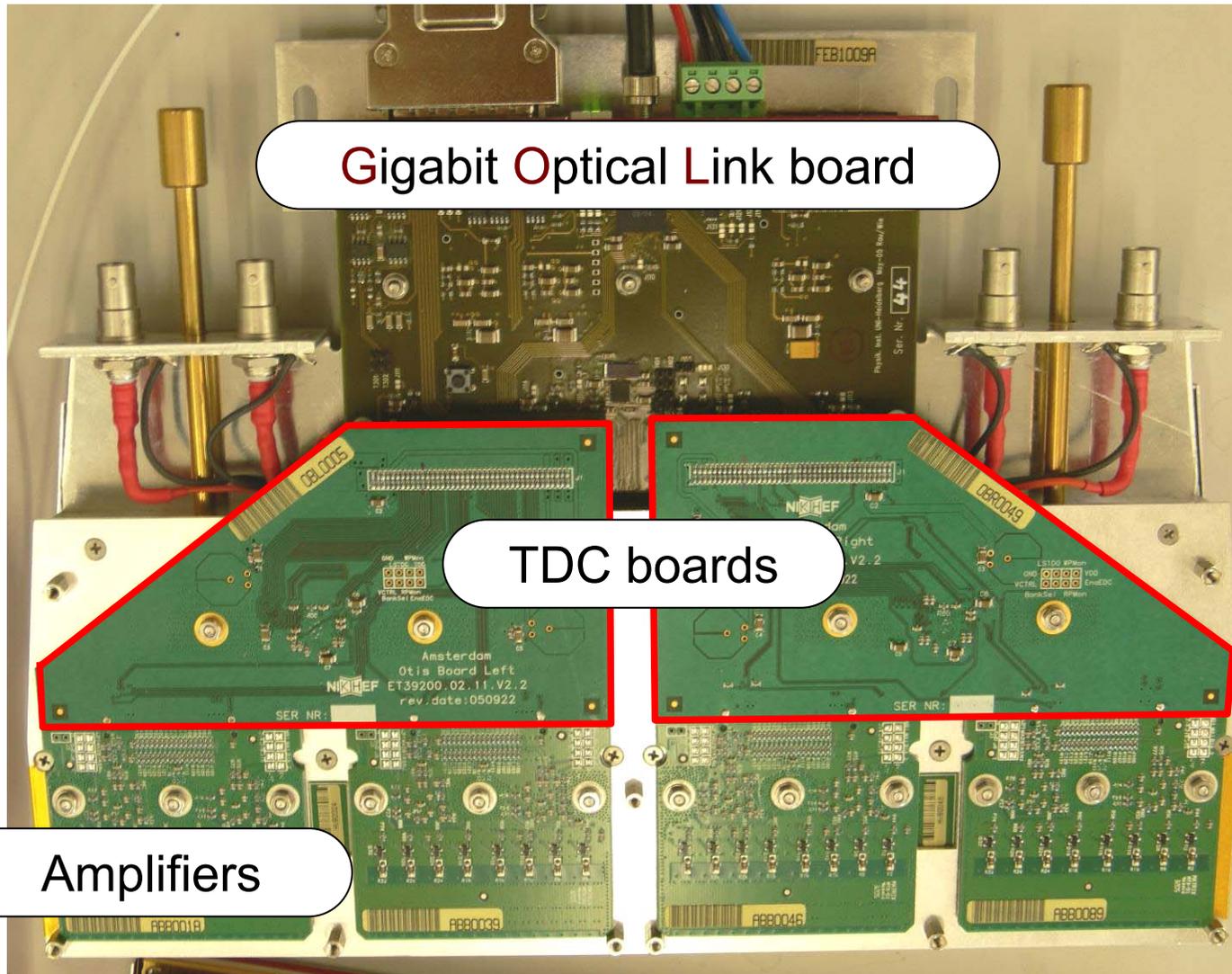
GOL Board jitter

- Jitter in optical data output sufficiently low
- Production bit error rate test with 9dB attenuation (4 min.)



Frontend box

Water cooled
Power dissipation:
20 W



432 Frontend
Boxes

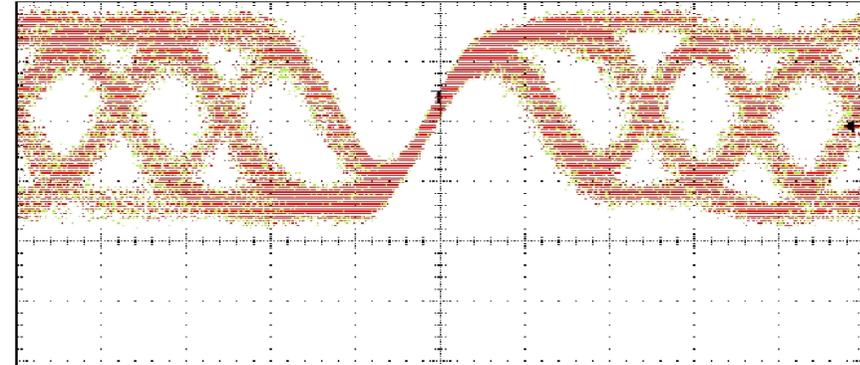
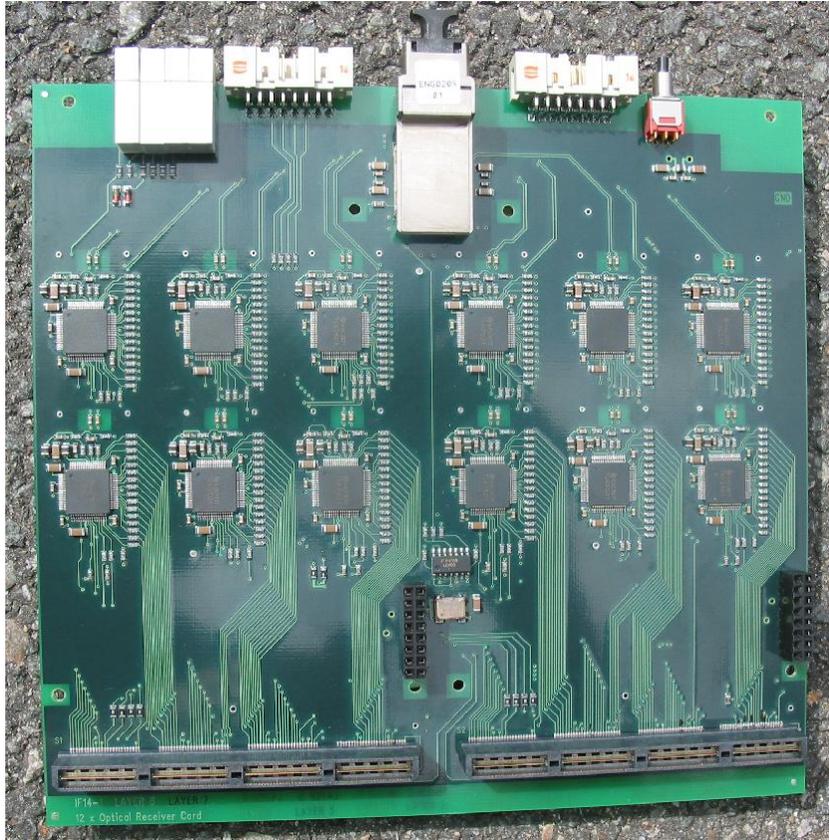
HV-boards
Inside

Amplifiers

Gigabit Optical Link board

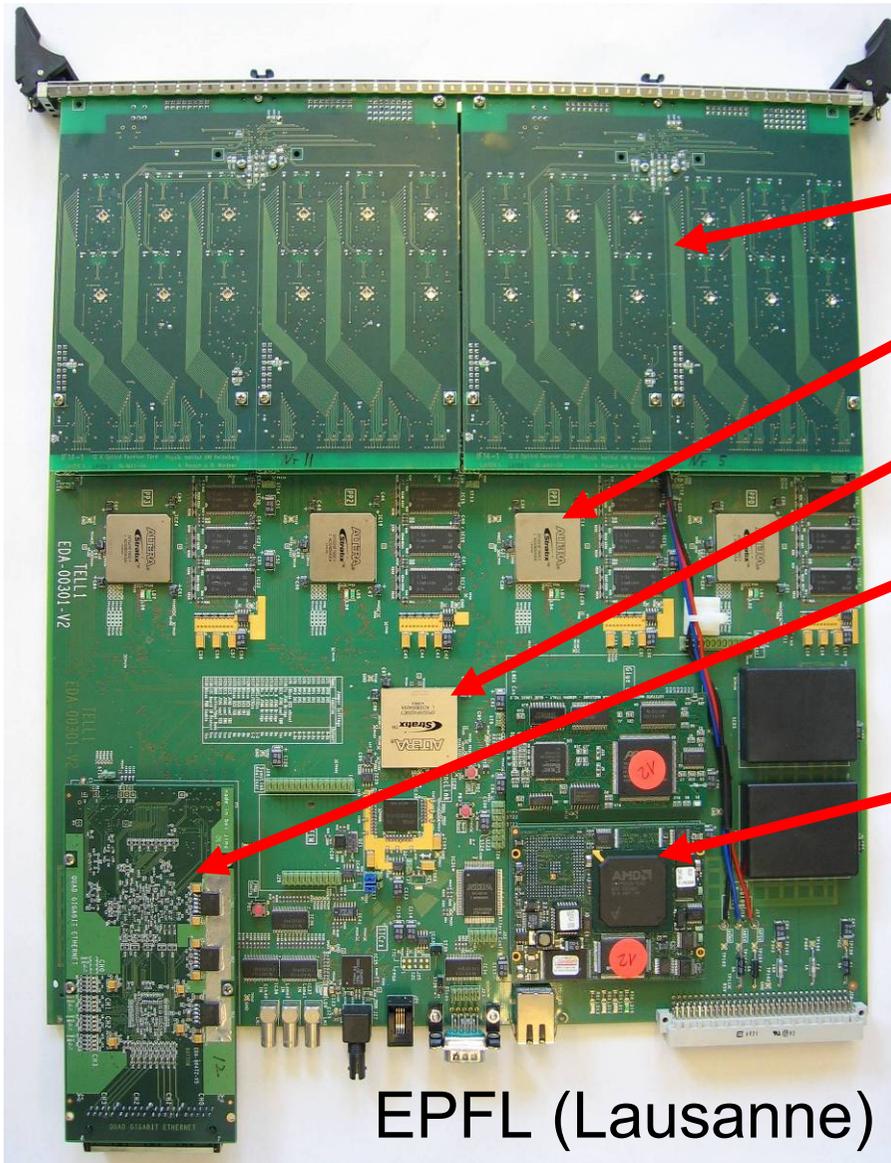
TDC boards

Optical Receiver Card



- Input mezzanine for DAQ board (TELL1)
- 12 optical inputs
- 19,2 Gbit/s
- 288 parallel electrical outputs
- Bit error rate below $< 10^{-15}$

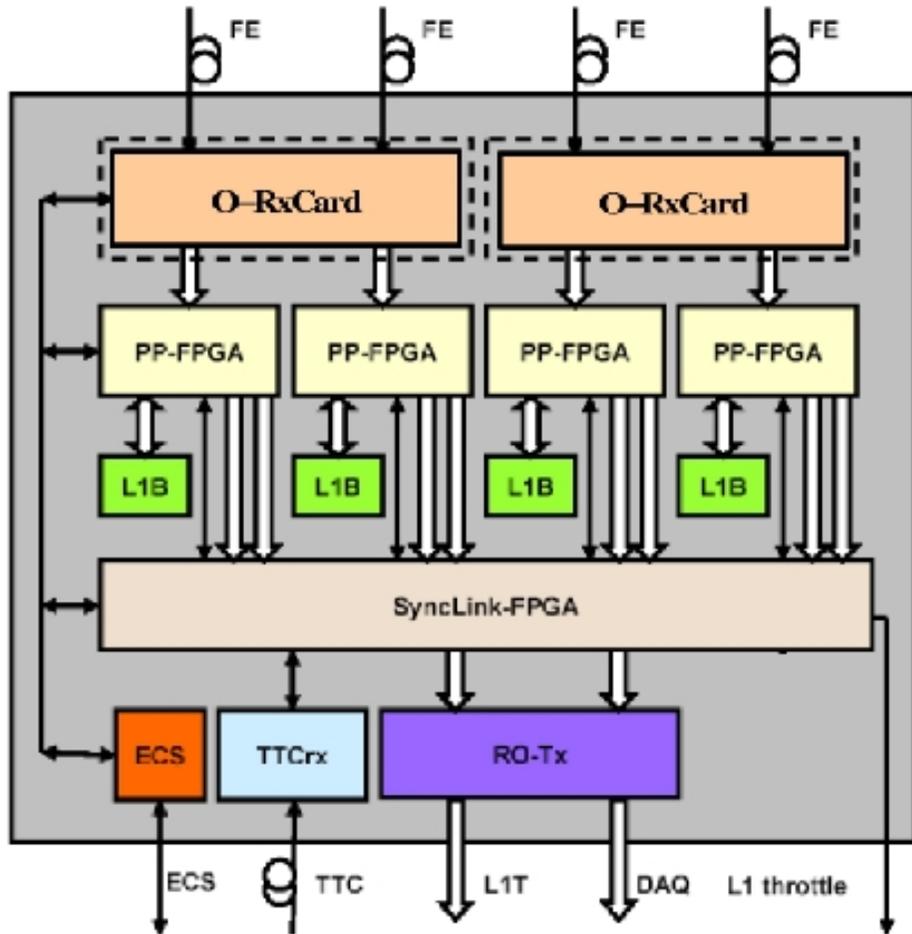
DAQ Board TELL1



- Optical receiver card
- Processing FPGAs
- SyncLink FPGA
- Quad Gigabit ethernet transmitter mezzanine
- Credit Card PC
- 1 MHz readout to PC farm LHCb wide

EPFL (Lausanne)

TELL1

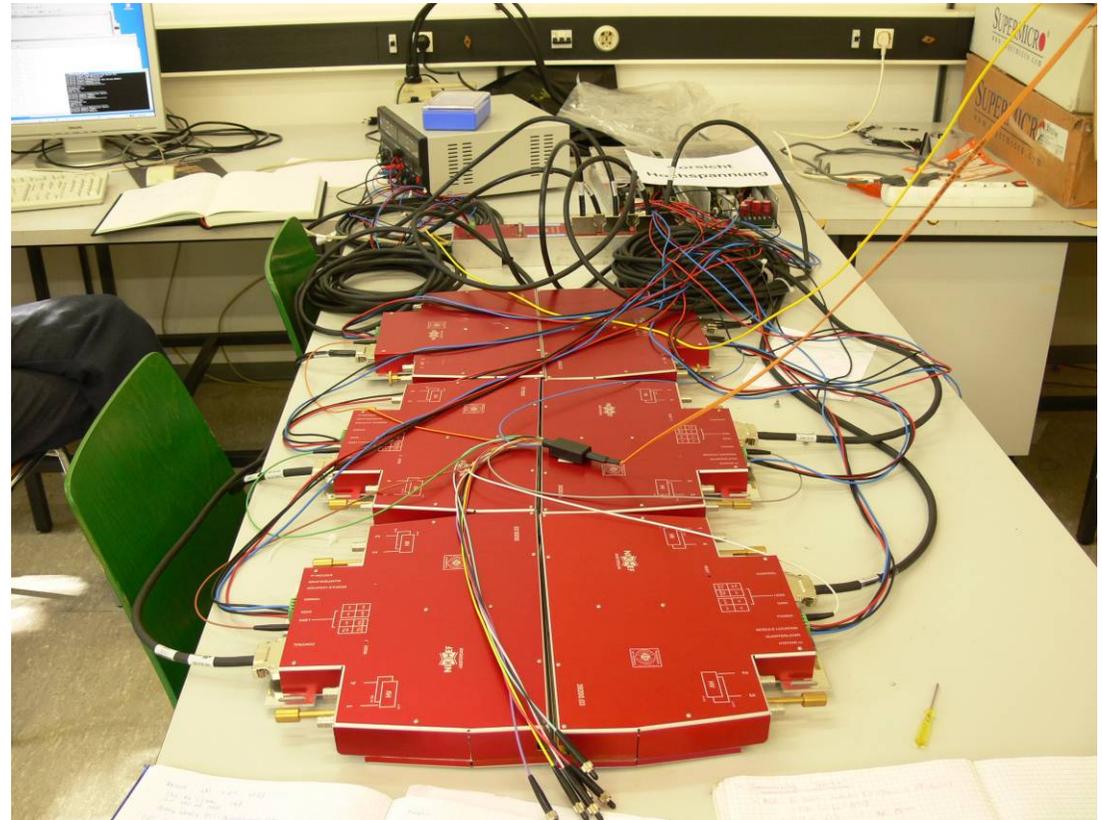


© Guido Haefeli

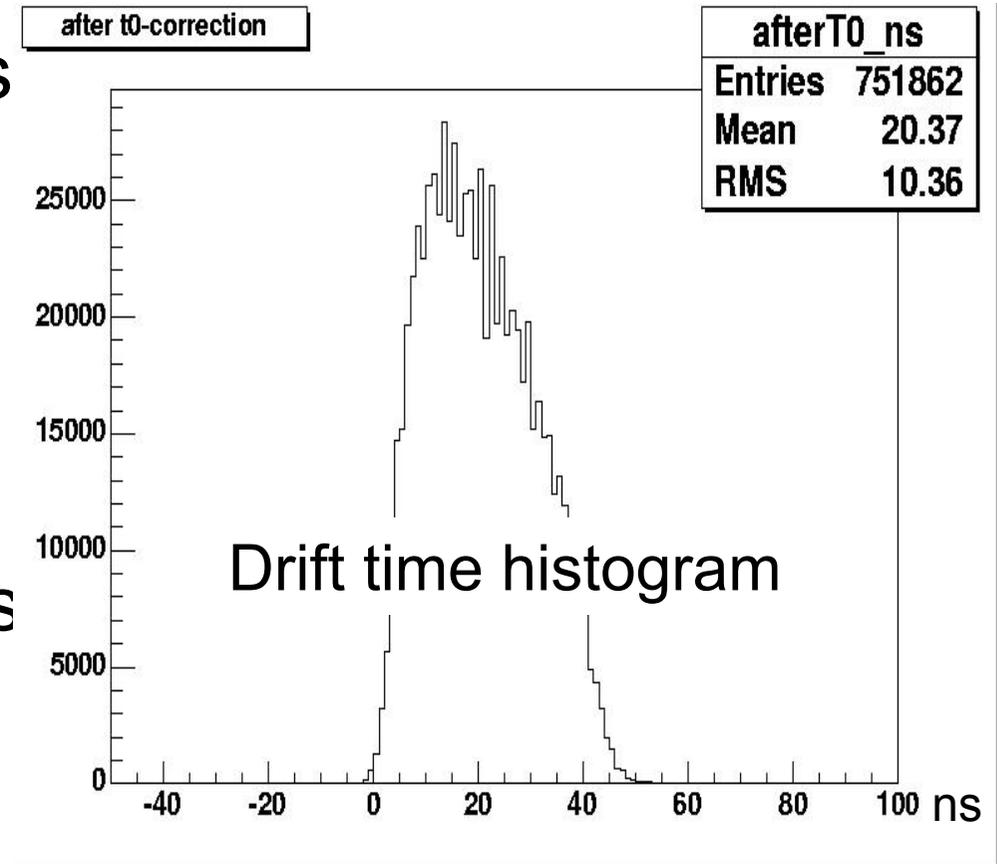
- Data from 9x128 channels (quarter layer)
- Deserialisation
- Synchronisation
- Zero suppression
- 4x Gbit Ethernet transmission to PC farm

Integration

- OT specific:
 - FE-Boxes
 - Distribution box
- LHCb wide
 - DAQ: TELL1
 - Readout Supervisor: ODIN
 - Slow Control: SPECS, PVSS



- Drift time resolution 0.5 ns
- Efficiency >94%
(uncorrected)
- Resolution ~175 μm
- Readout electronics works
form straw to PC



Summary and outlook

- Achieved

- Pre series production showed good performance in beam test with 512 channels
- Readout electronics in production (500 units)
- Produced & tested:
 - all Optical Receiver Cards
 - all ASICs, see Poster session
 - >100 boards of each type in the FE-box



- Next step

- Assembly and test of FE-boxes
- Installation & commissioning at CERN

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Time resolution

- Time difference from two scintillators
- RMS = 0.72 ns

