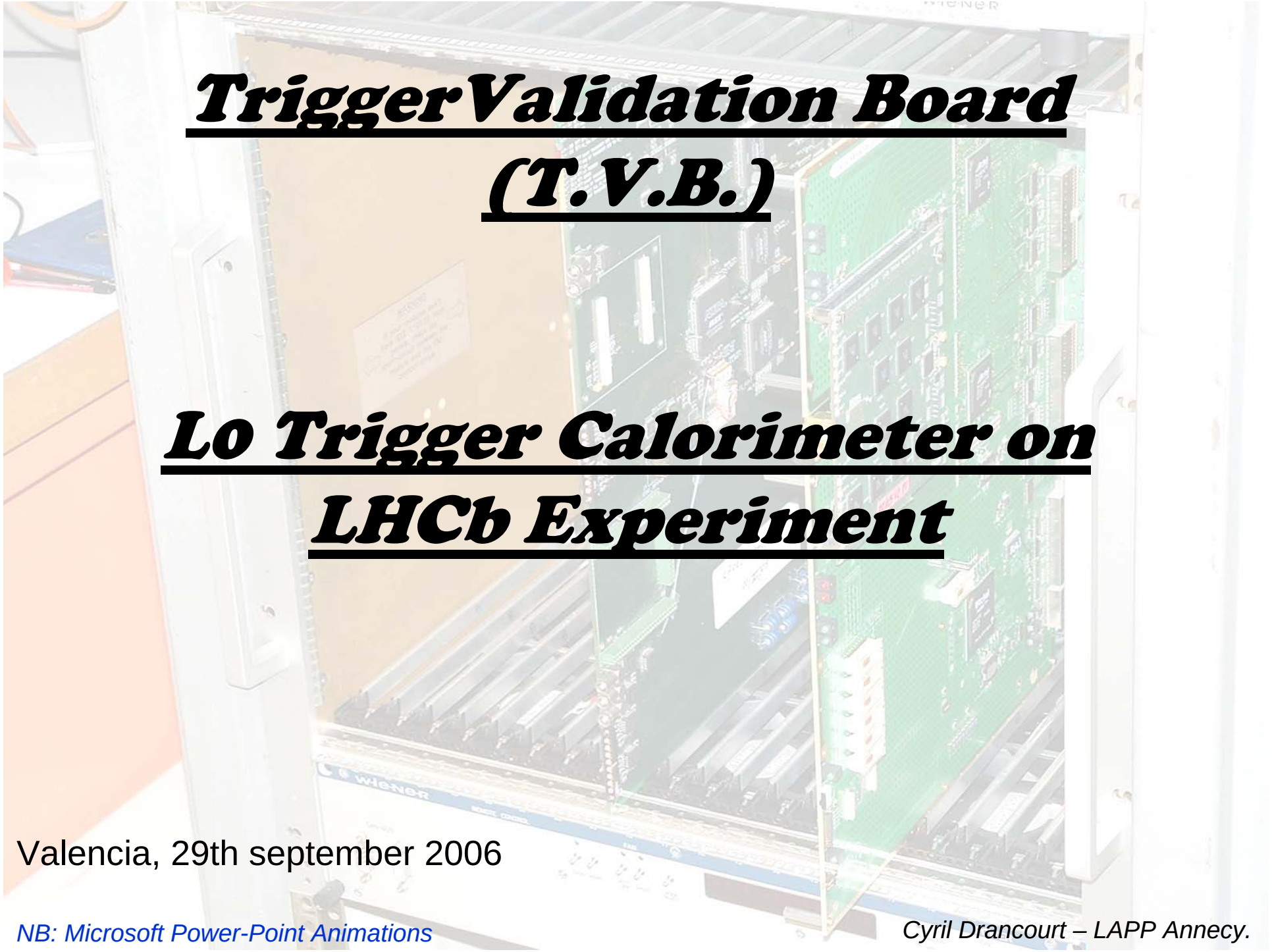


TriggerValidation Board (T.V.B.)

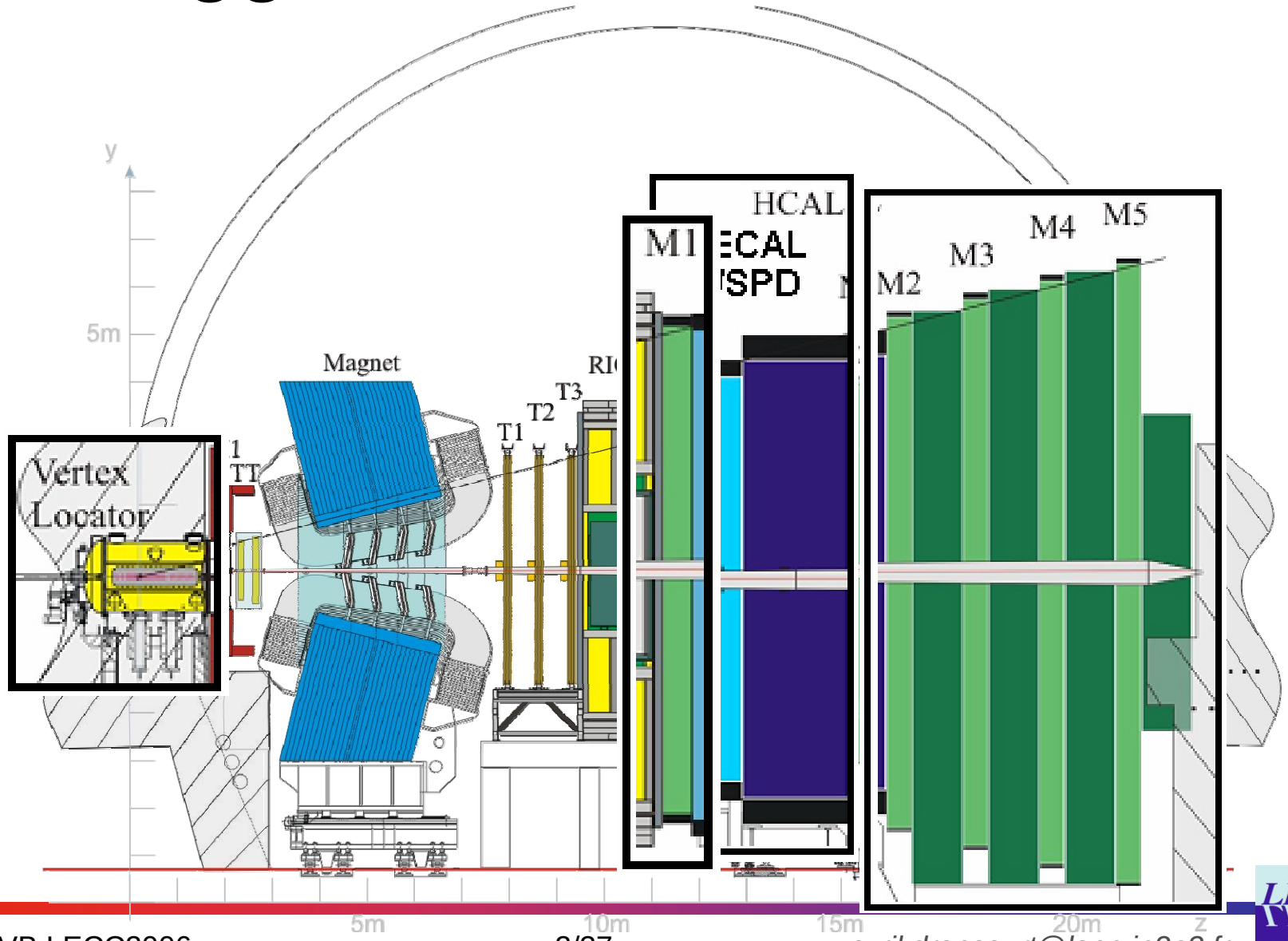
Lo Trigger Calorimeter on LHCb Experiment

Valencia, 29th september 2006

NB: Microsoft Power-Point Animations

Cyril Drancourt – LAPP Annecy.

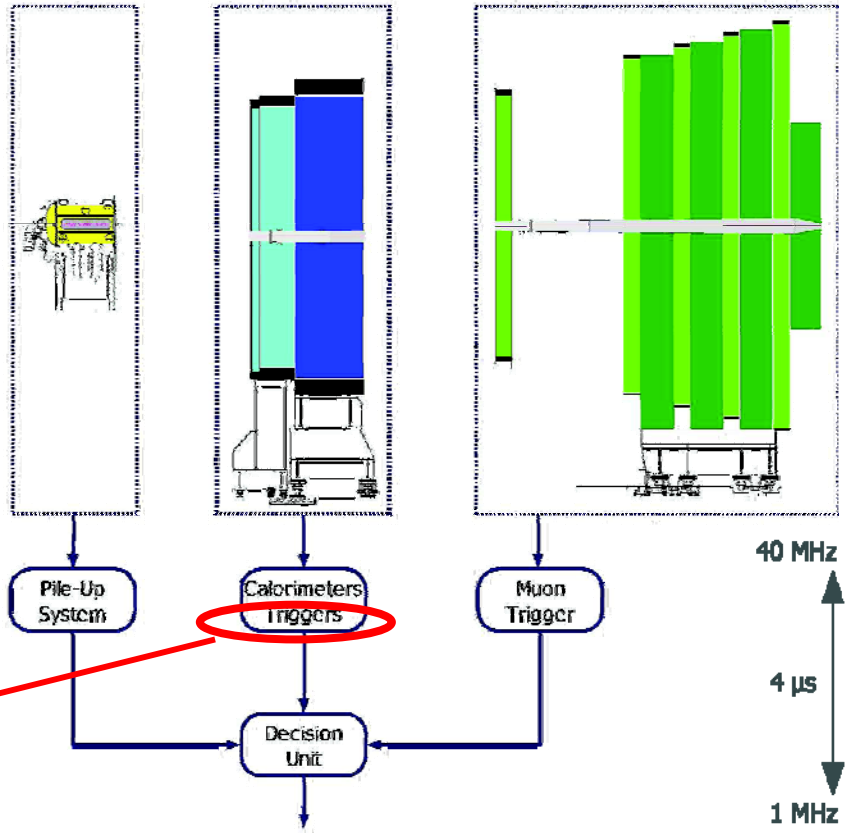
Trigger detector on LHCb



Le TRIGGER

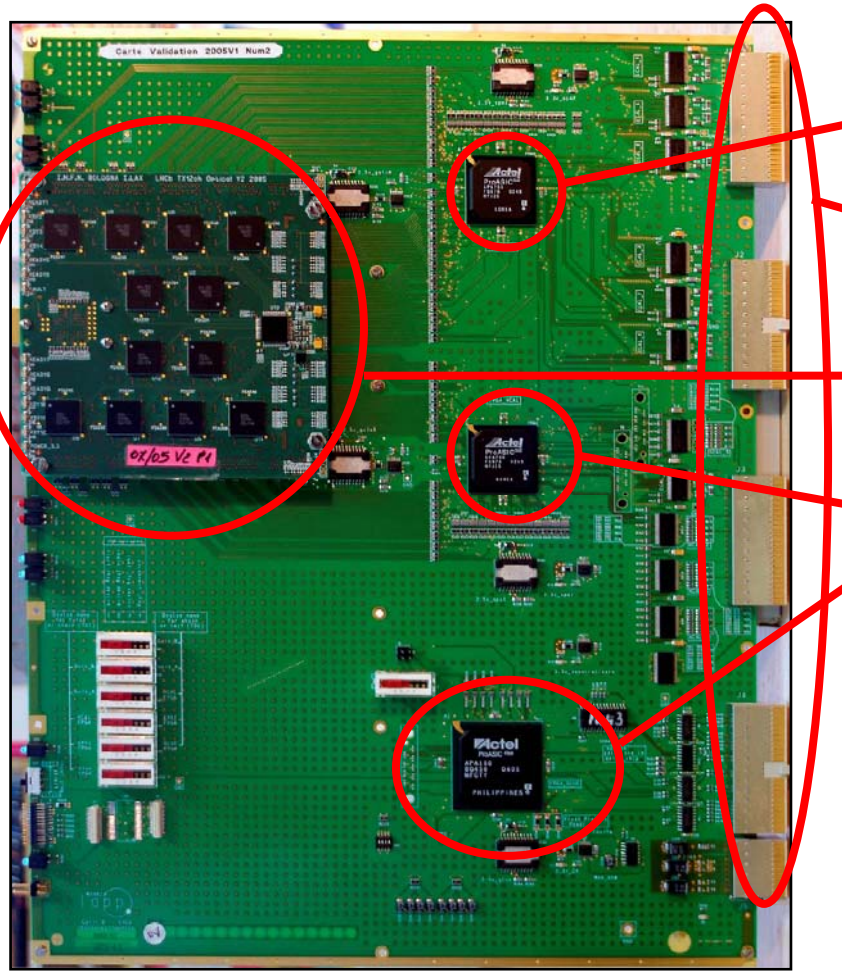
- **Data**:
  40 Téra-bytes/s

- **Trigger selection:**
  first level



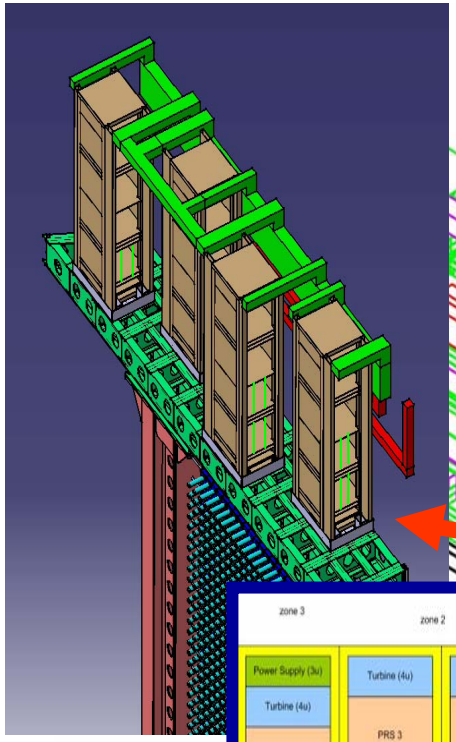
Trigger Validation Board
(only for calorimeters)

Trigger Validation Board



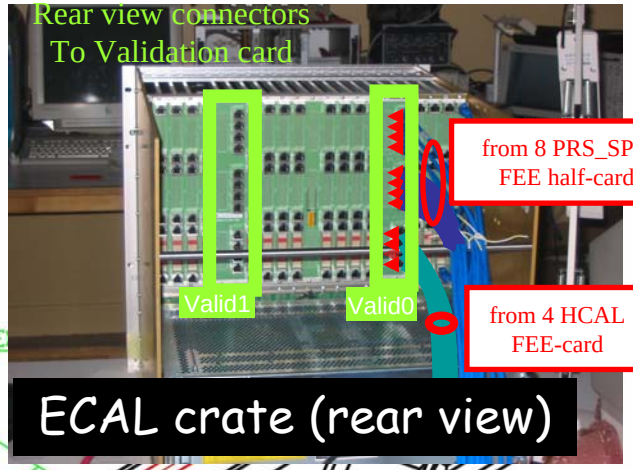
FPGA EPPI
Inputs
Outputs: électron
4 bus photon
8 bus e/γ
Optical Mezzanine
8 bus
Glue FPGA

FPGA HCAL
4 outputs « Hadron »

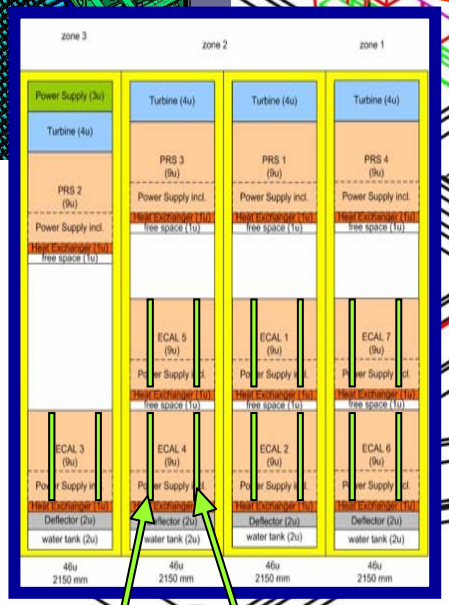


Selection board in barrack

12 optic fiber rubbon (8 used)

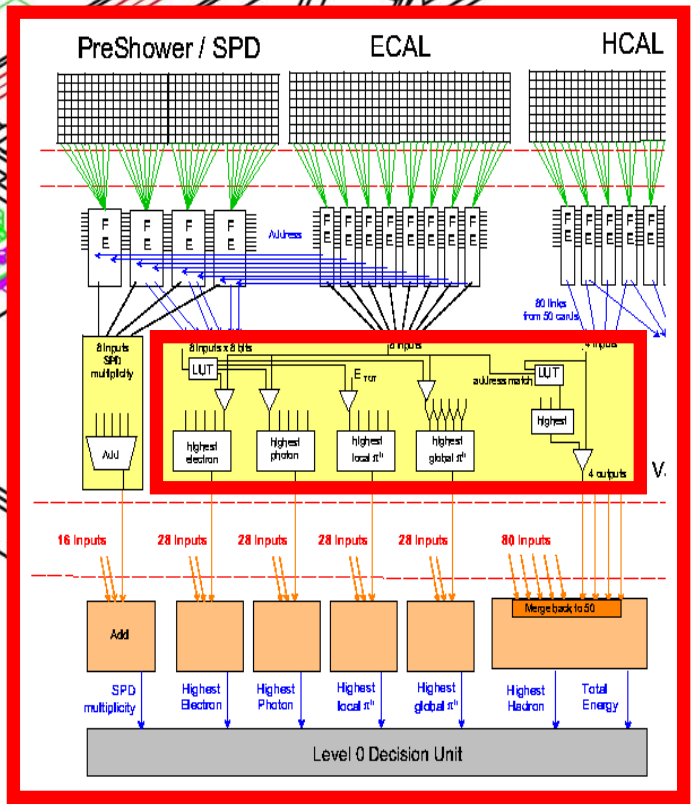


ECAL crate (rear view)



Validation Board *(2x14 boards in ECAL Crate)*

ECAL crate (front view)



Validation Board

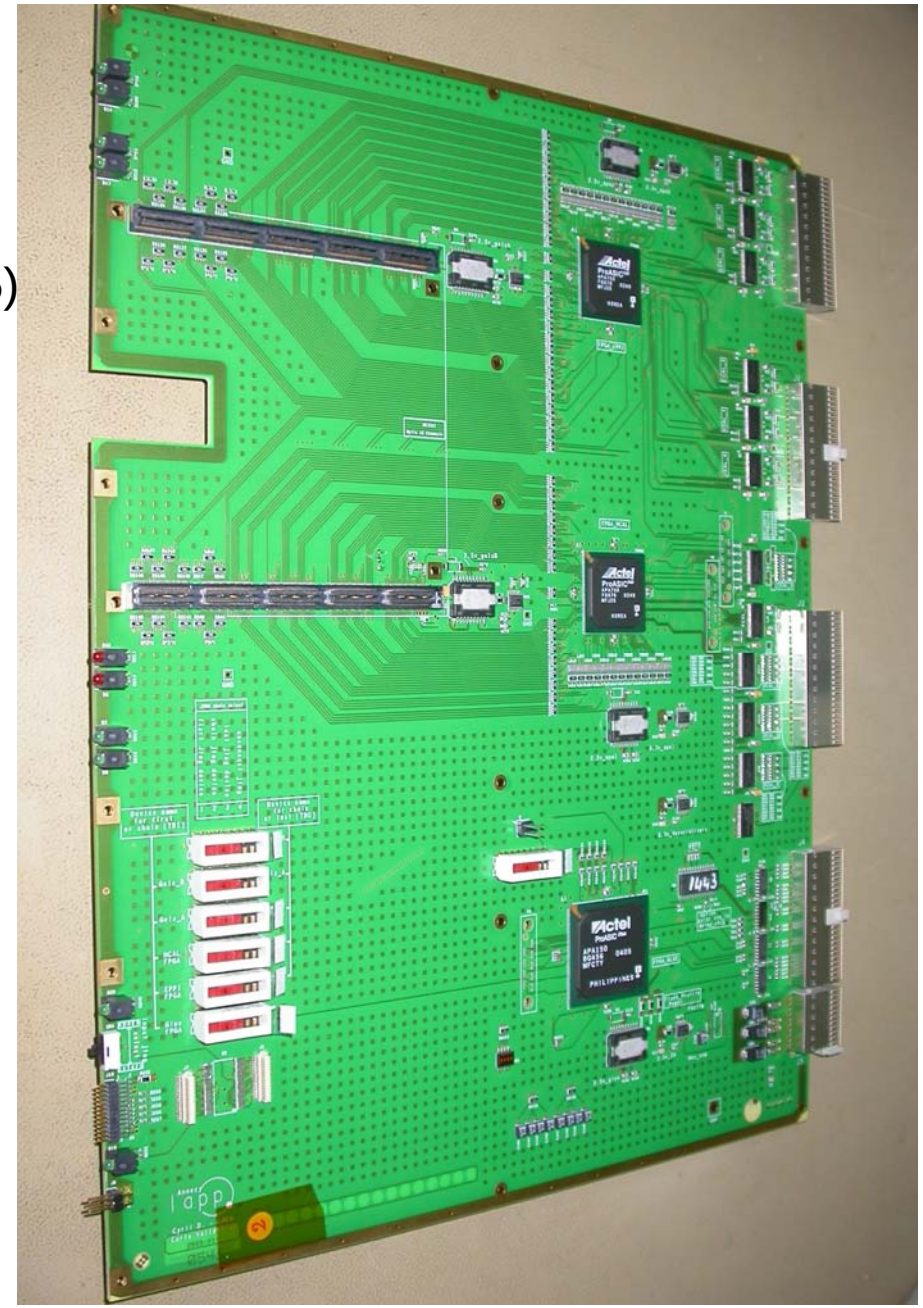
- Start design: Sept 2004
- 3prototypes in lab: 2 in Annecy (nov05&apr05)

  1 in Orsay (dec05)
- Cost for 1 proto: 4428€
(PCB+Soldering+Takaya_test+Front_Panel)

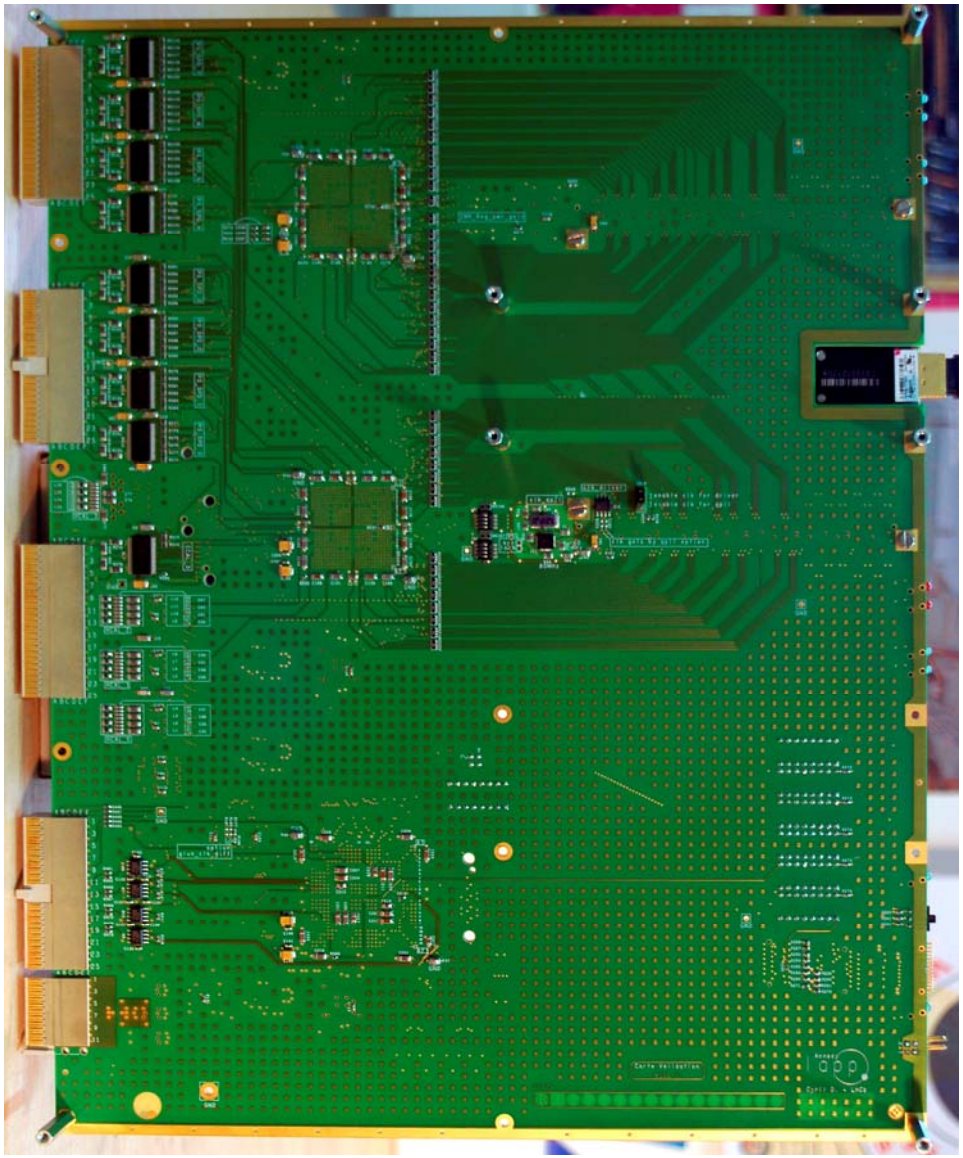
MaineCI ASCO ASCO SCHROFF

- Some technical details:
  - 16 layers
  - 2,4mm tchickness
  - **250 µm vias**
  - **Free Halogen dielectric**
  - ~1000 components
  - **3 Actel ProAsic** FPGAs

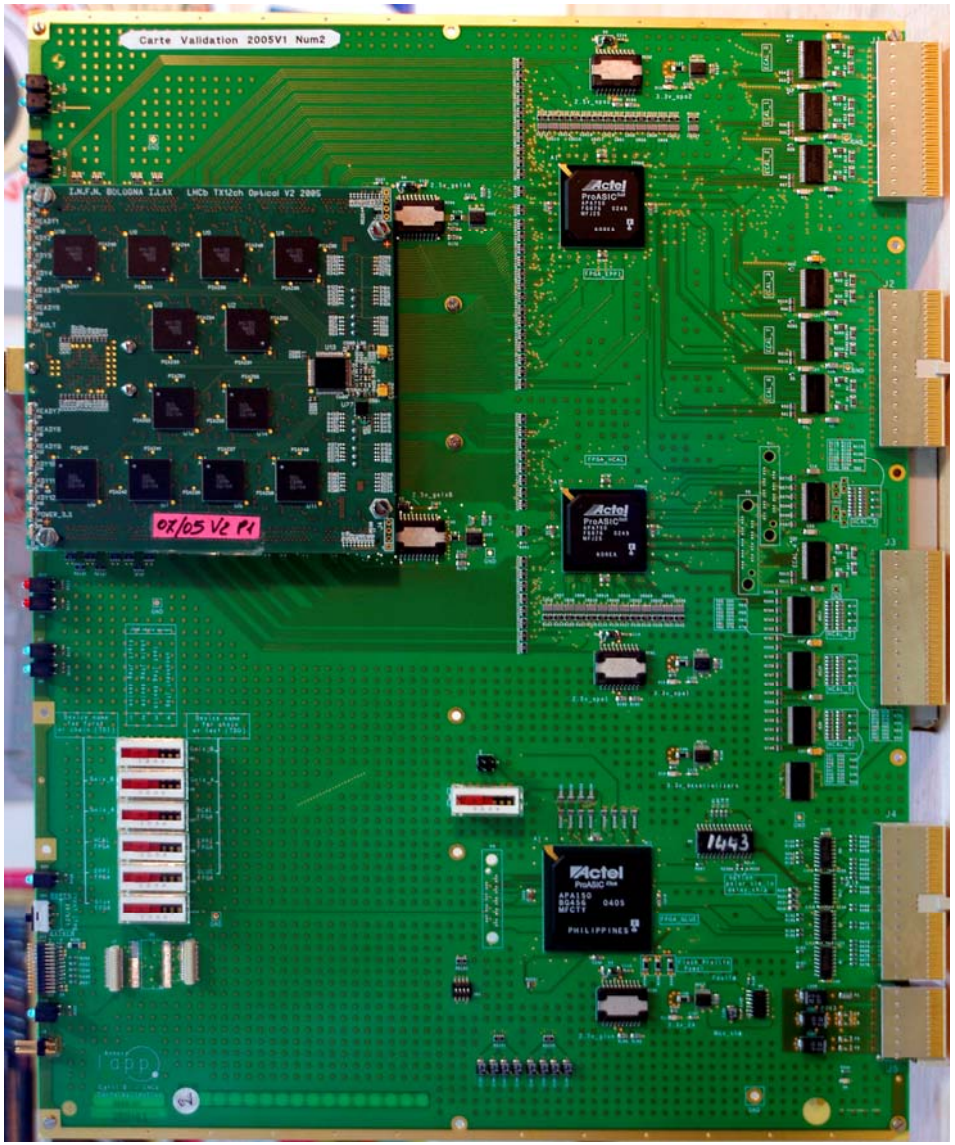
    (APA750, APA750, APA150)
- Start product: August 2006



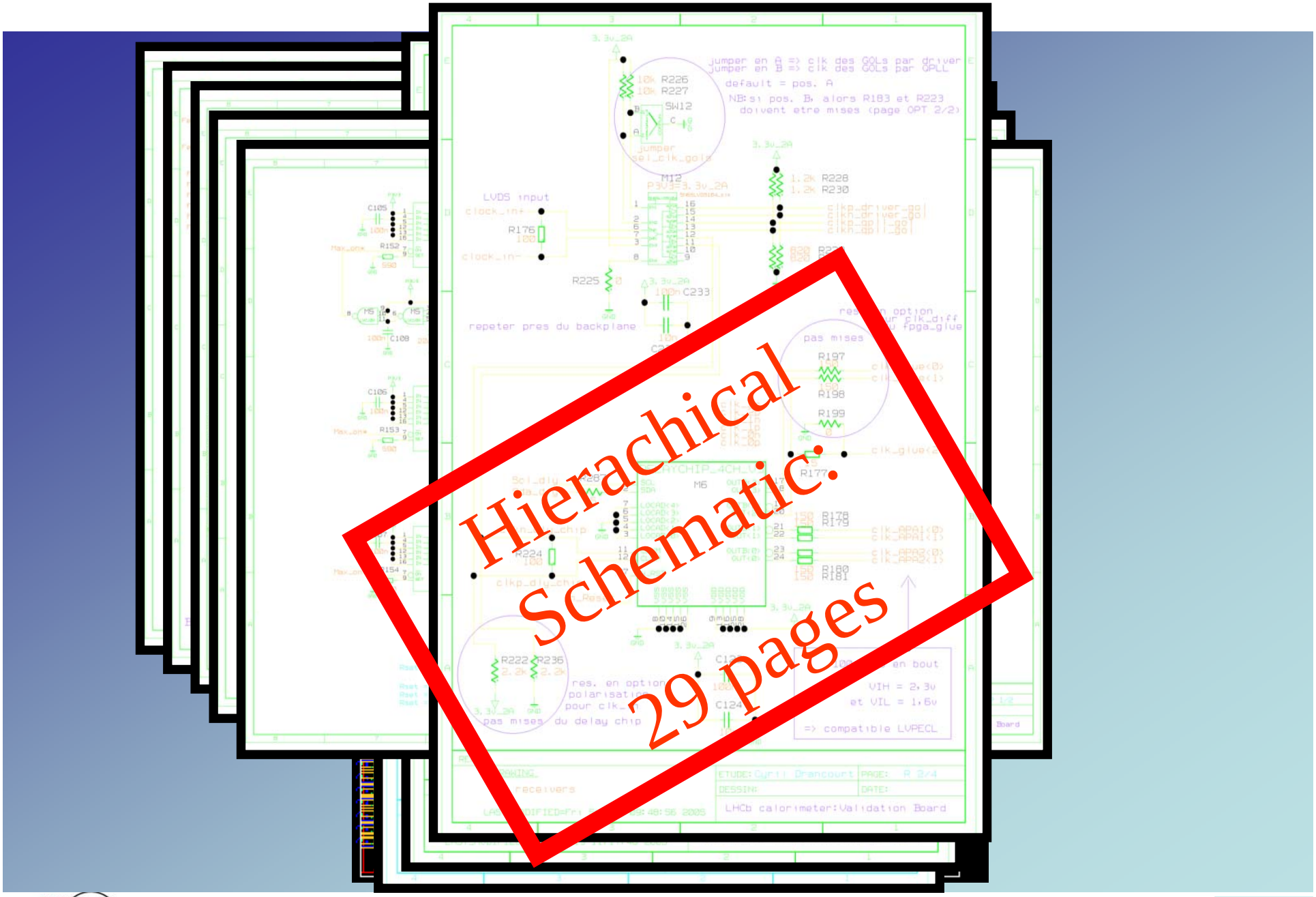
Complete Validation board with 12 ch optic mezzanine(from bologna)

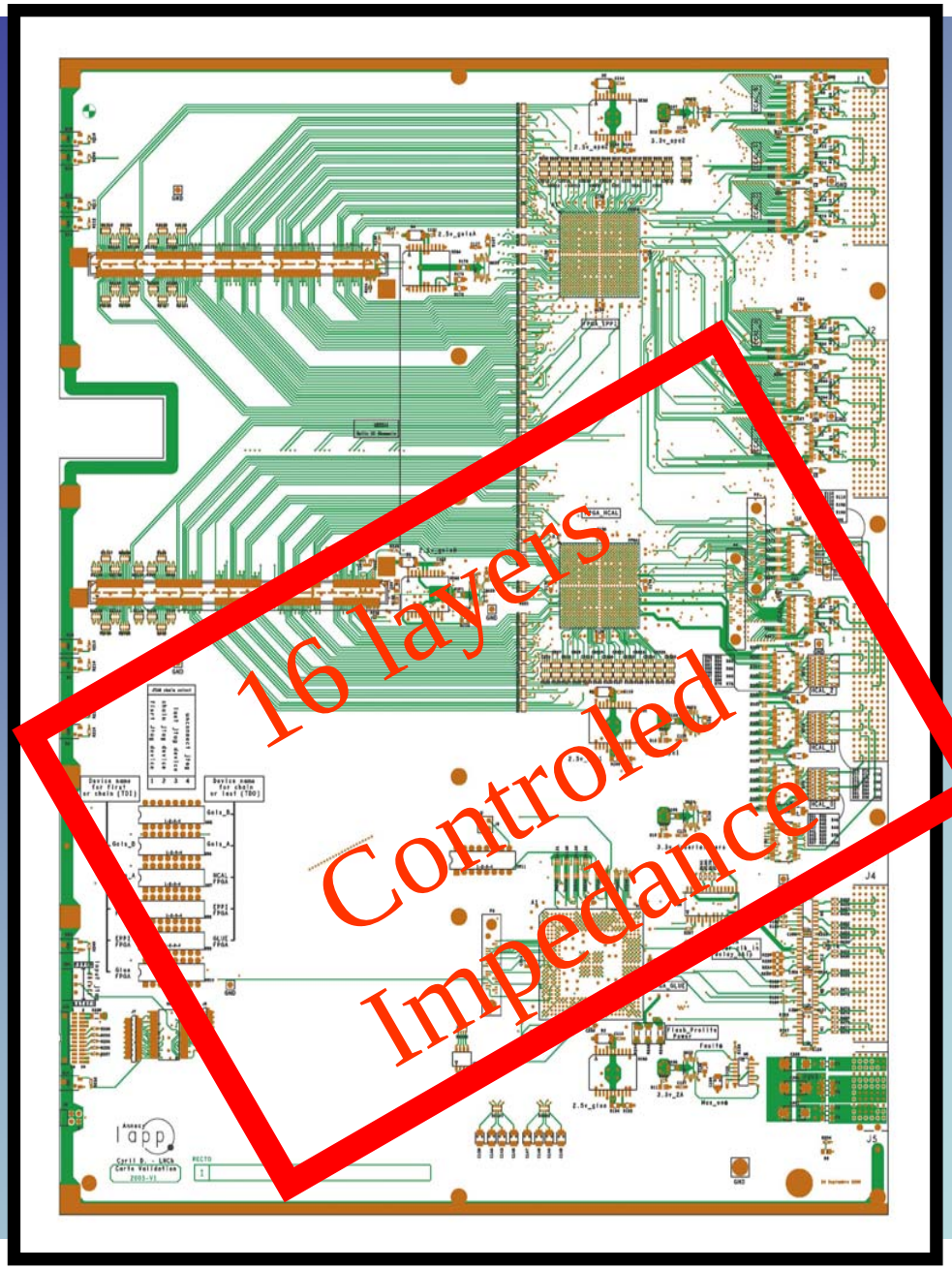


BOTTOM View

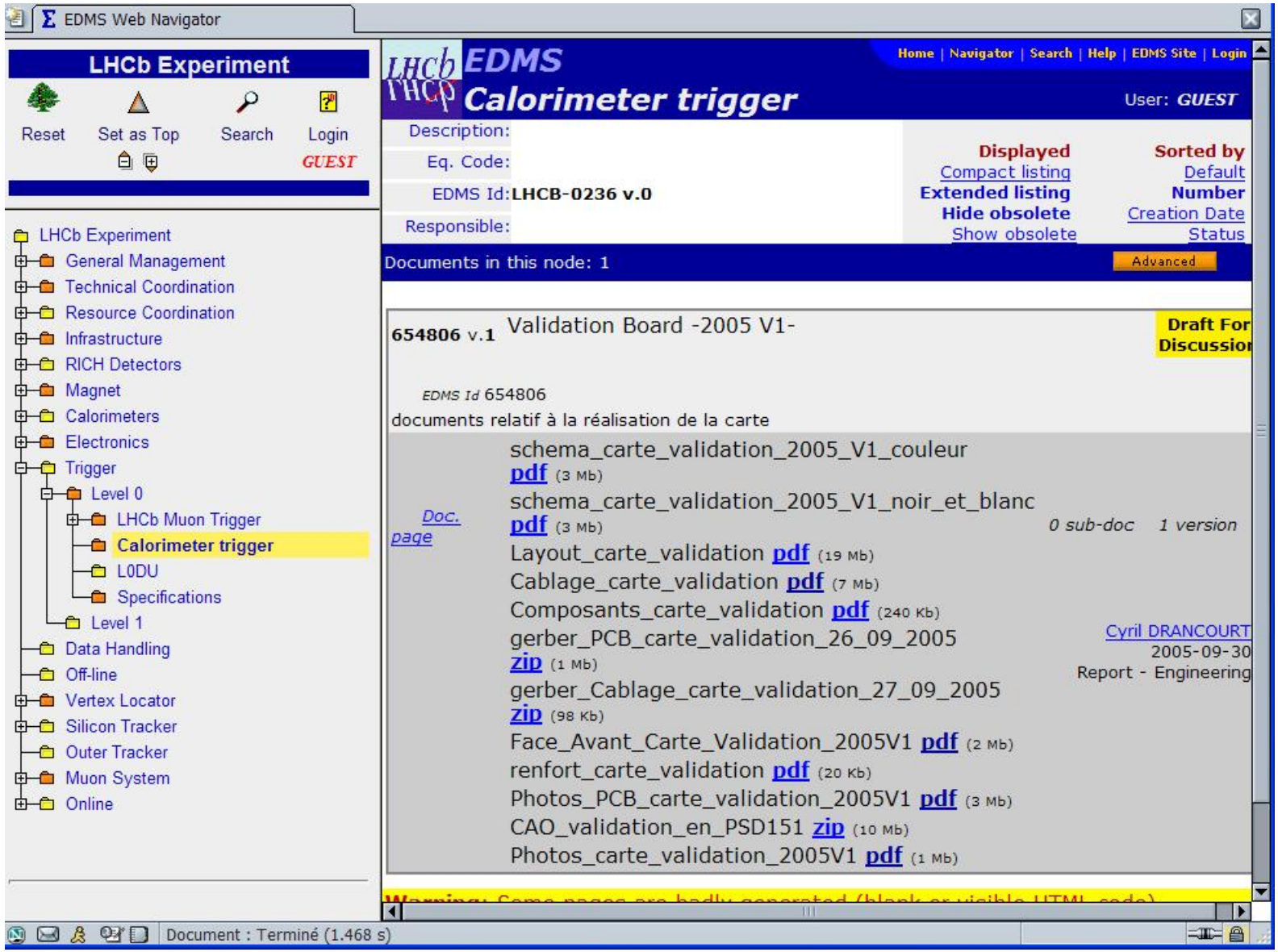


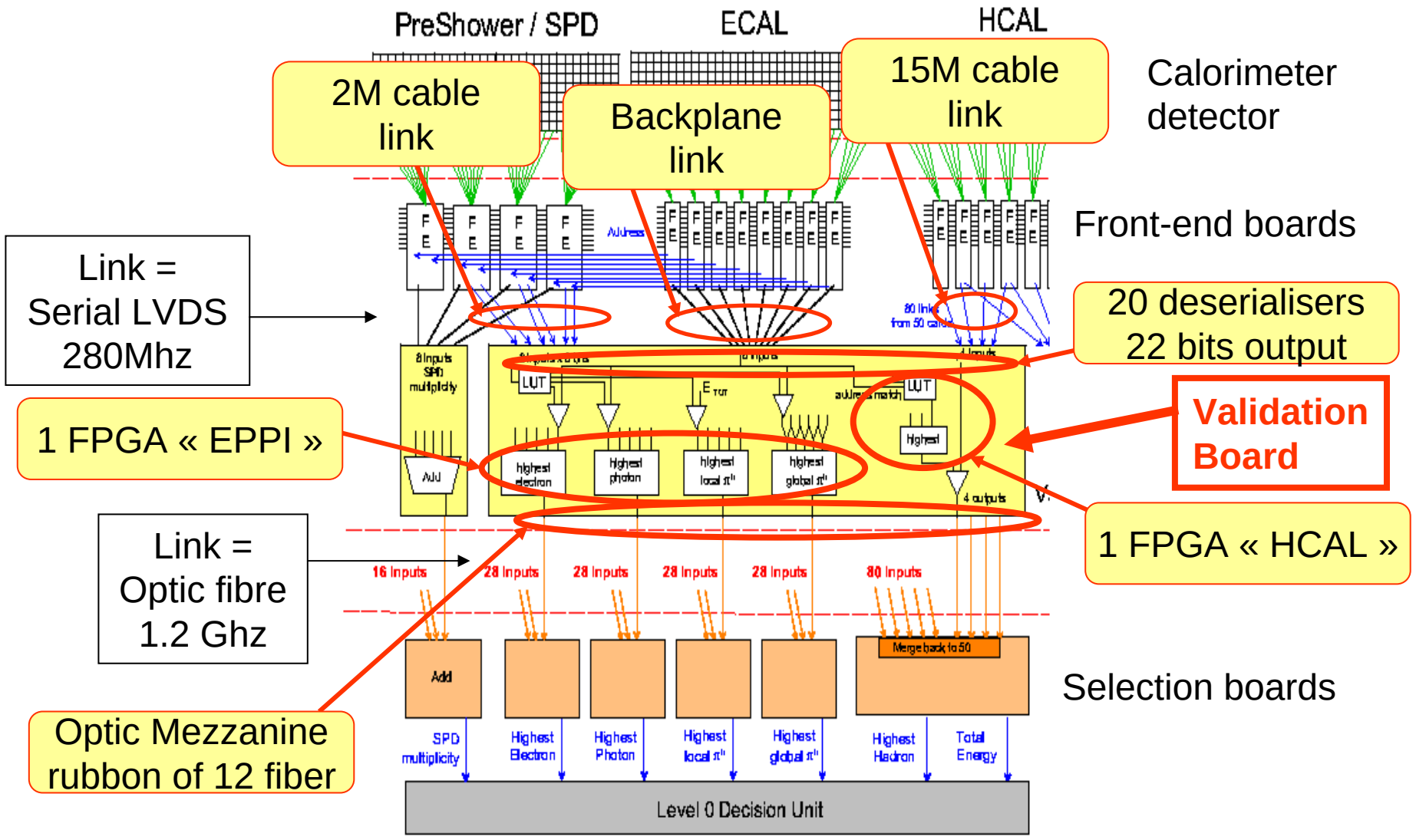
TOP View

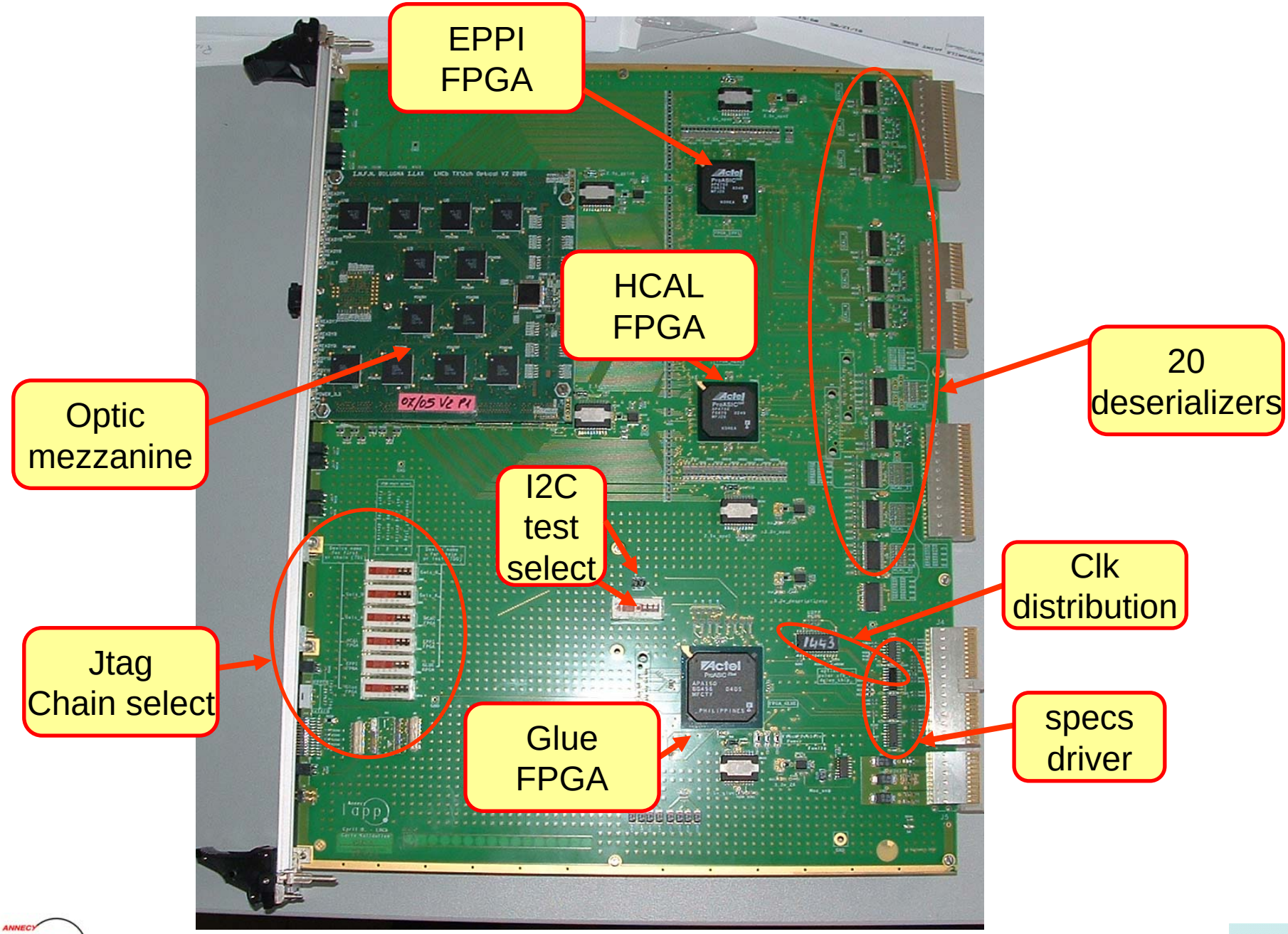

Hierachical Schematic:
29 pages

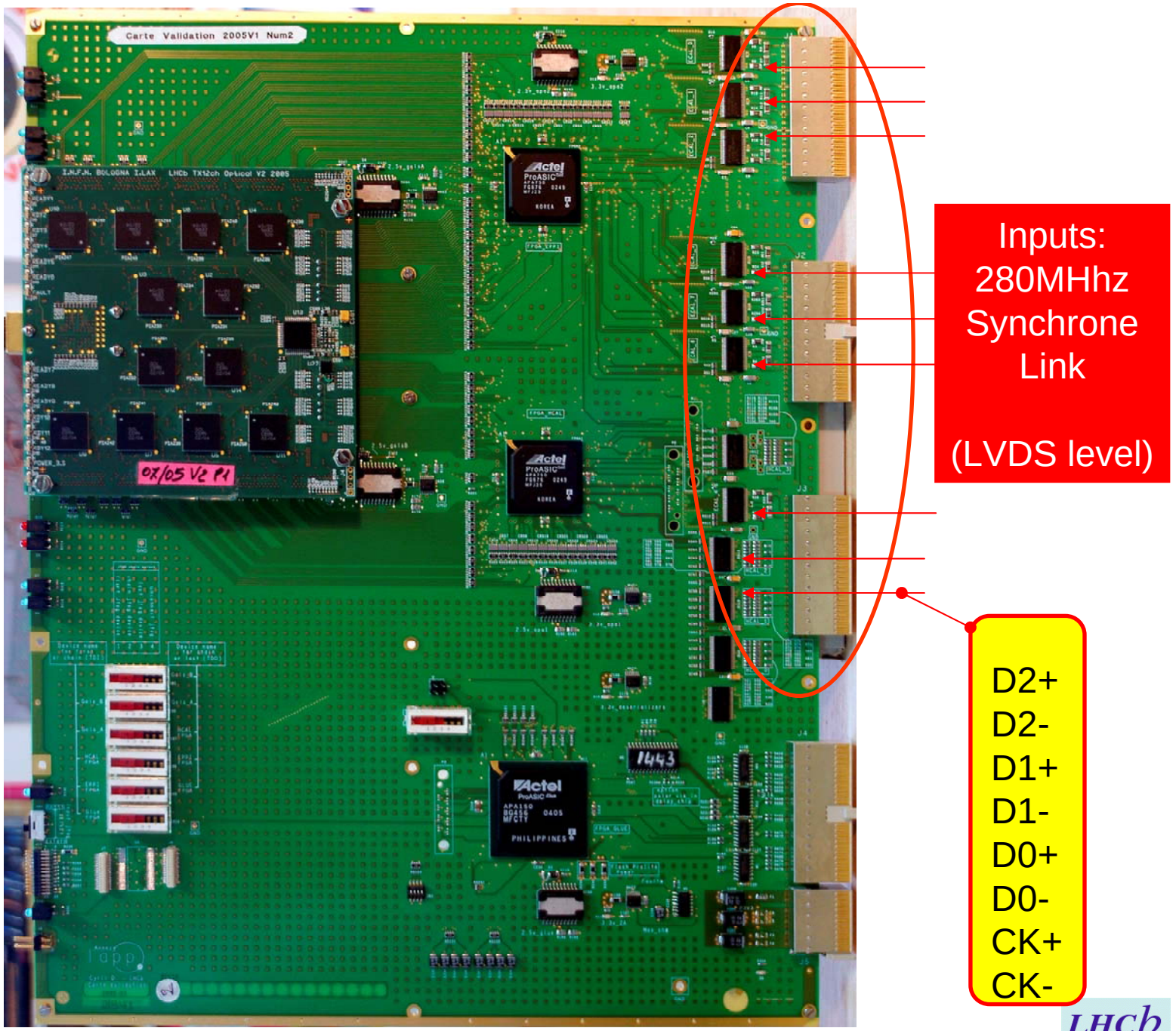

16 layers
Controled
Impedance

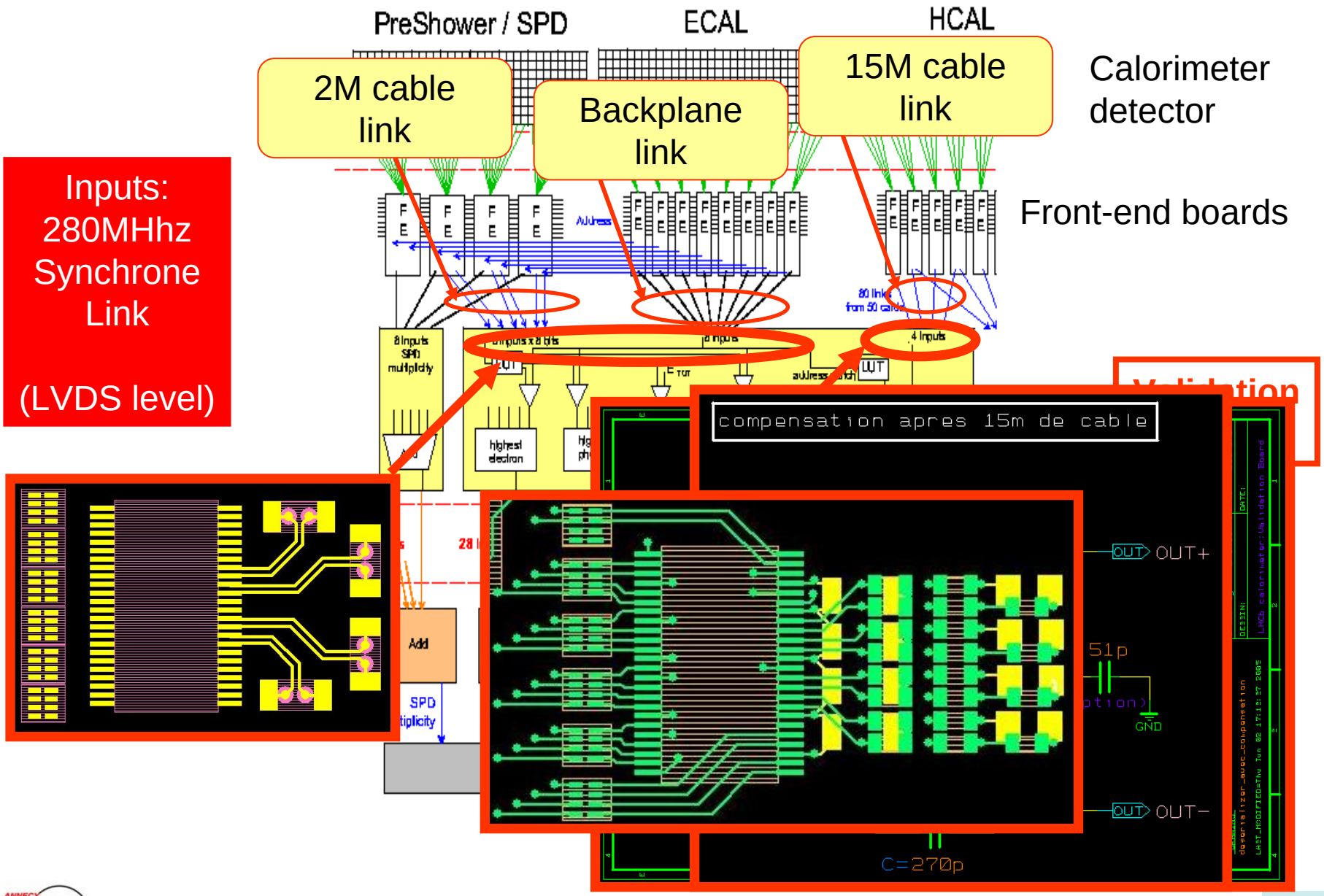
https://edms.cern.ch/document/654806



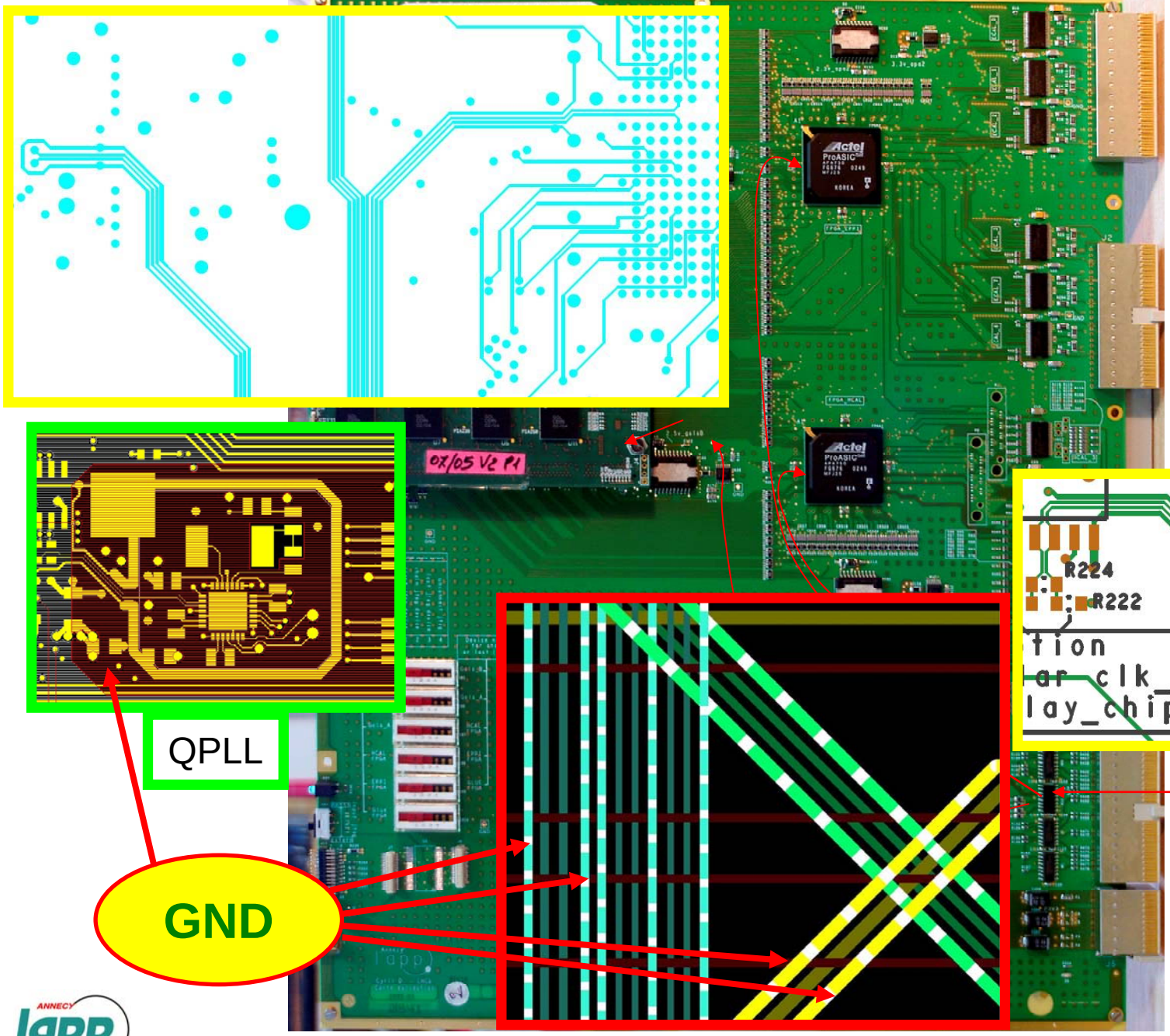

PreShower / SPD
ECAL
HCAL
2M cable link
Backplane link
15M cable link
Calorimeter detector
Front-end boards
Link = Serial LVDS 280Mhz
20 deserialisers 22 bits output
Validation Board
1 FPGA « EPPI »
1 FPGA « HCAL »
Link = Optic fibre 1.2 Ghz
Optic Mezzanine rubbon of 12 fiber
Selection boards
16 Inputs
28 Inputs
28 Inputs
28 Inputs
28 Inputs
80 Inputs
Add
Merge back to 50
SPD multiplicity
Highest Electron
Highest Photon
Highest local π°
Highest global π°
Highest Hadron
Total Energy
Level 0 Decision Unit

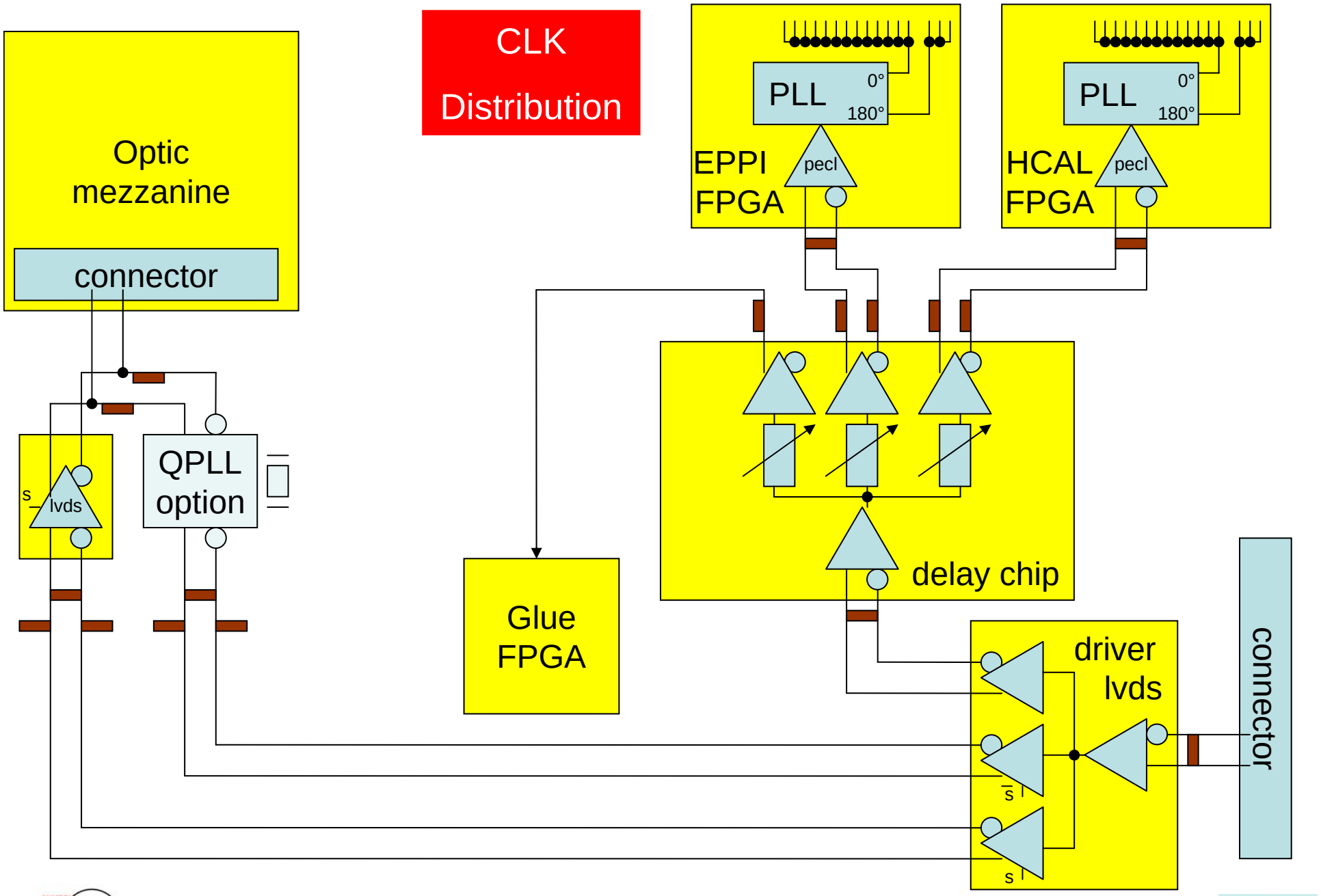

EPPI
FPGA
HCAL
FPGA
20
deserializers
Optic
mezzanine
I2C
test
select
Clk
distribution
Jtag
Chain select
Glue
FPGA
specs
driver

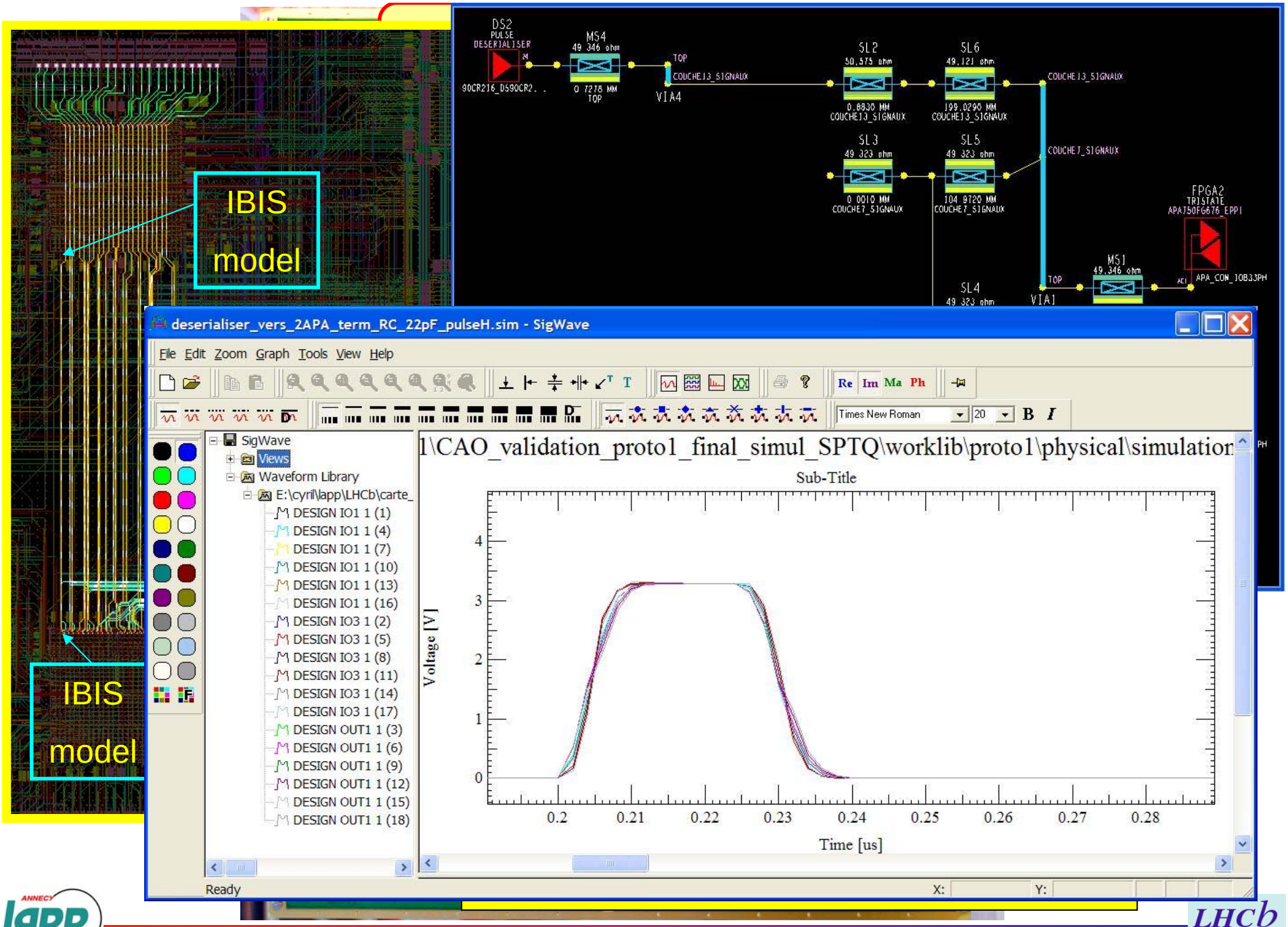

Carte Validation 2005V1 Num2
I.N.F.N. BOLOGNA I.LAX LHCb TX12ch Optical V2 2005
07/05 V2 P1
Actel ProASIC
1443
Inputs:
280MHhz
Synchrone
Link
(LVDS level)
D2+
D2-
D1+
D1-
D0+
D0-
CK+
CK-


PreShower / SPD
ECAL
HCAL
2M cable link
Backplane link
15M cable link
Calorimeter detector
Front-end boards
Inputs: 280MHhz Synchrone Link
(LVDS level)
compensation apres 15m de cable
OUT+
OUT-
51p
GND
C=270p
Add
SPD

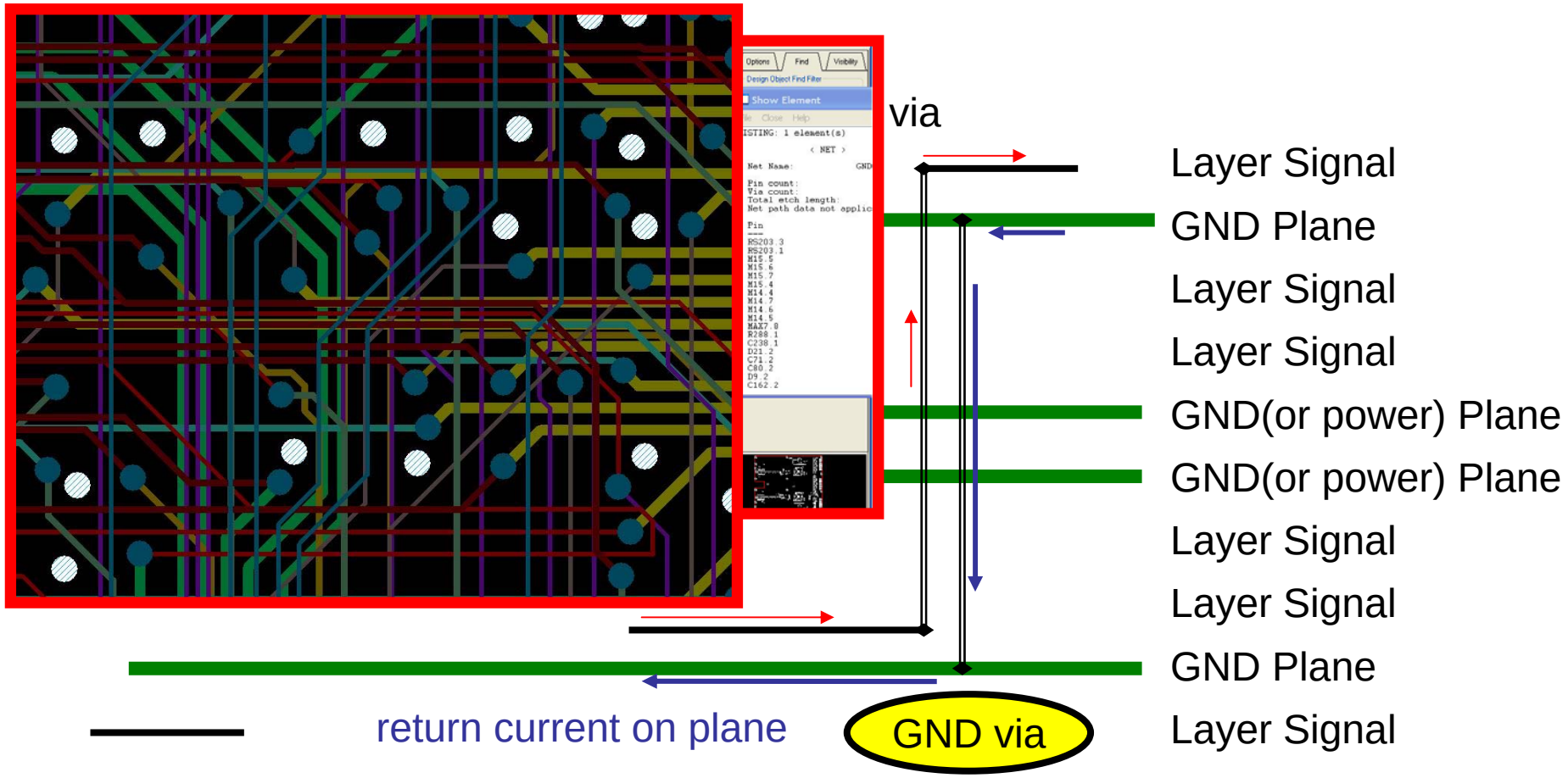
CLK Distribution




CLK
Distribution
Optic
mezzanine
connector
PLL
0°
180°
EPPI
FPGA
pecl
PLL
0°
180°
HCAL
FPGA
pecl
s
lvds
QPLL
option
delay chip
Glue
FPGA
driver
lvds
connector
s
s


IBIS
model
IBIS
model
DS2
PULSE
DESERIALISER
MS4
49.346 ohm
TOP
COUCHE13_SIGNAUX
VIA4
SL2
50.575 ohm
SL6
49.121 ohm
SL3
49.323 ohm
SL5
49.323 ohm
SL4
COUCHE7_SIGNAUX
FPGA2
TRISTATE
APA750FG676_EPP1
MS1
49.346 ohm
VIA1
APA_CON_10B33PH
deserialiser_vers_2APA_term_RC_22pF_pulseH.sim - SigWave
File Edit Zoom Graph Tools View Help
Re Im Ma Ph
Times New Roman
20
SigWave
Views
Waveform Library
E:\cyril\app\LHCb\carte_
DESIGN IO1 1 (1)
DESIGN IO1 1 (4)
DESIGN IO1 1 (7)
DESIGN IO1 1 (10)
DESIGN IO1 1 (13)
DESIGN IO1 1 (16)
DESIGN IO3 1 (2)
DESIGN IO3 1 (5)
DESIGN IO3 1 (8)
DESIGN IO3 1 (11)
DESIGN IO3 1 (14)
DESIGN IO3 1 (17)
DESIGN OUT1 1 (3)
DESIGN OUT1 1 (6)
DESIGN OUT1 1 (9)
DESIGN OUT1 1 (12)
DESIGN OUT1 1 (15)
DESIGN OUT1 1 (18)
1\CAO_validation_proto1_final_simul_SPTQ\worklib\proto1\physical\simulation
Sub-Title
Voltage [V]
Time [us]
0
1
2
3
4
0.2
0.21
0.22
0.23
0.24
0.25
0.26
0.27
0.28
Ready
X:
Y:

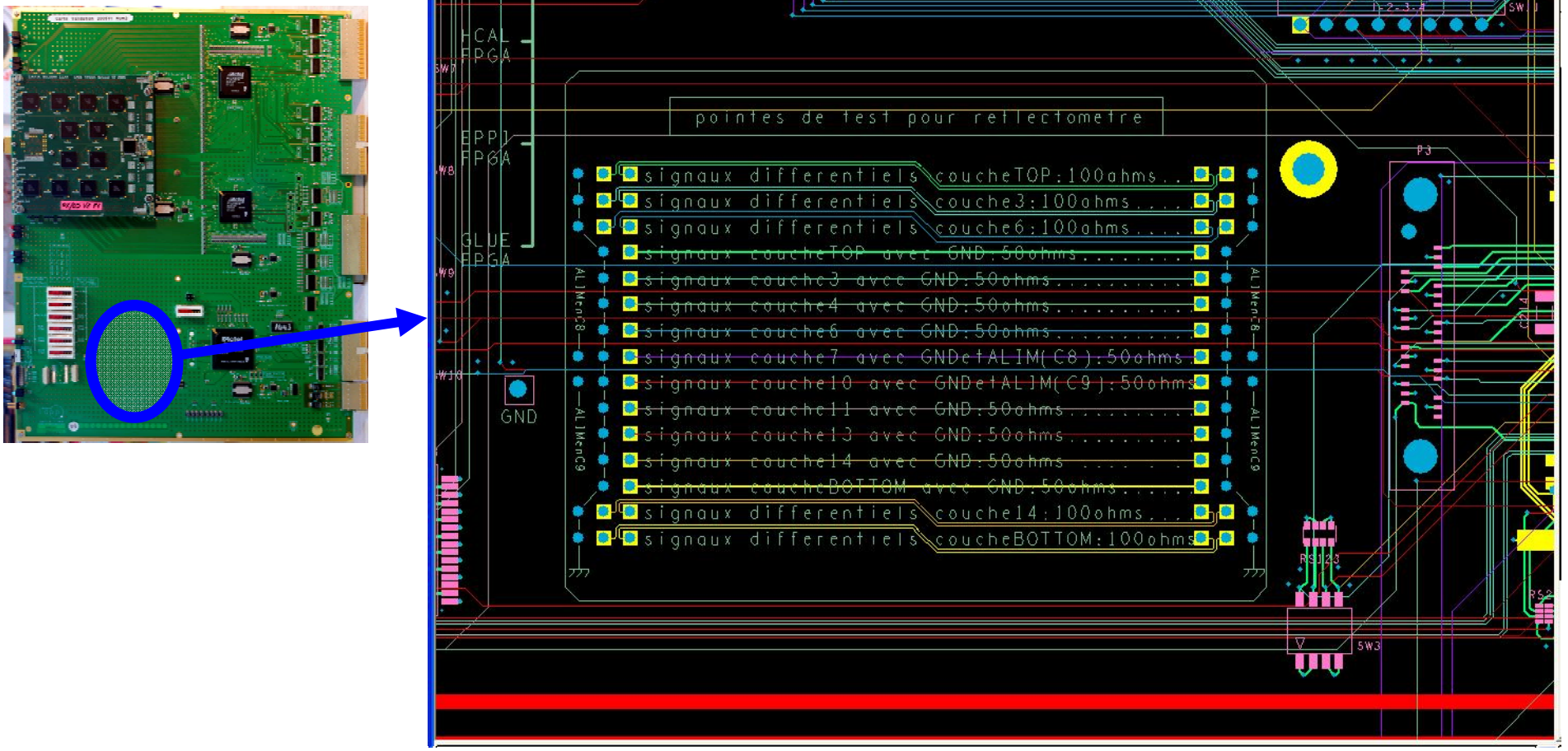
Impedance control: CEM rule



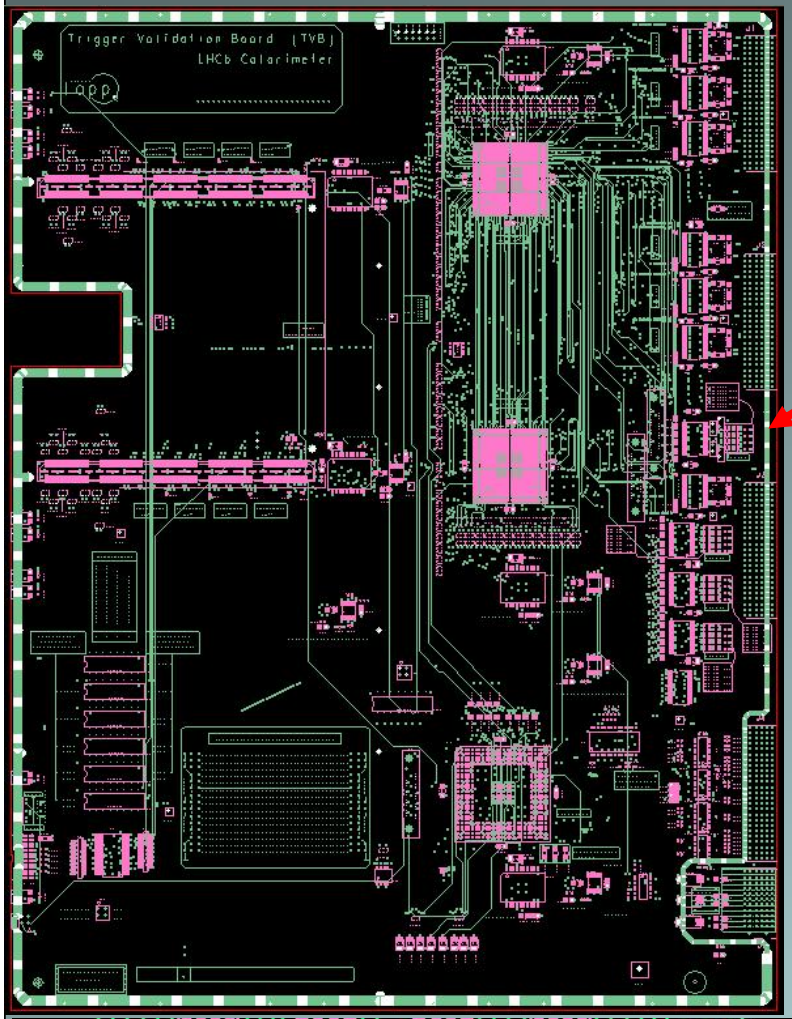
All wires are adapted

empilement carte validation	couche	epaisseur (mm)	**materiau** (dielectrique sans halogene)	signaux uni 50 ohms largeur Cu	signaux diff 100 ohms largeur Cu , isolement
	serigraphie				
	verni recto	0,02			
	1 (top)	0,035	feuille en cuivre 0,009 +recharge	250µ	150µ , 150µ
epaisseur totale: 2,411		0,156	prepreg hitachi:GEA-679FG en 2 x 1080		
sans verni: 2,371	2	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	3	0,0175	cuivre 0,0175 (couche externe du stratifié)	160µ	120µ , 180µ
		0,12	prepreg hitachi:GEA-679FG en 2 x 1080		
	4	0,0175	cuivre 0,0175 (couche externe du stratifié)	160µ	
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	5	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,11	prepreg hitachi:GEA-679FG en 1 x 2116		
	6	0,0175	cuivre 0,0175 (couche externe du stratifié)	120µ	
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	7	0,0175	cuivre 0,0175 (couche externe du stratifié)	120µ	
		0,11	prepreg hitachi:GEA-679FG en 1 x 2116		
	8	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	9	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,11	prepreg hitachi:GEA-679FG en 1 x 2116		
	10	0,0175	cuivre 0,0175 (couche externe du stratifié)	120µ	
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	11	0,0175	cuivre 0,0175 (couche externe du stratifié)	120µ	
		0,11	prepreg hitachi:GEA-679FG en 1 x 2116		
	12	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	13	0,0175	cuivre 0,0175 (couche externe du stratifié)	160µ	
		0,12	prepreg hitachi:GEA-679FG en 2 x 1080		
	14	0,0175	cuivre 0,0175 (couche externe du stratifié)	160µ	120µ , 180µ
		0,152	stratifié hitachi:MCL-E-679FG en 6 mils		
	15	0,0175	cuivre 0,0175 (couche externe du stratifié)	plan	plan
		0,156	prepreg hitachi:GEA-679FG en 2 x 1080		
	16 (bottom)	0,035	feuille en cuivre 0,009 +recharge	250µ	150µ , 150µ
Cyril Drancourt, 22 sept 2005	verni verso	0,02	puis serigraphie		

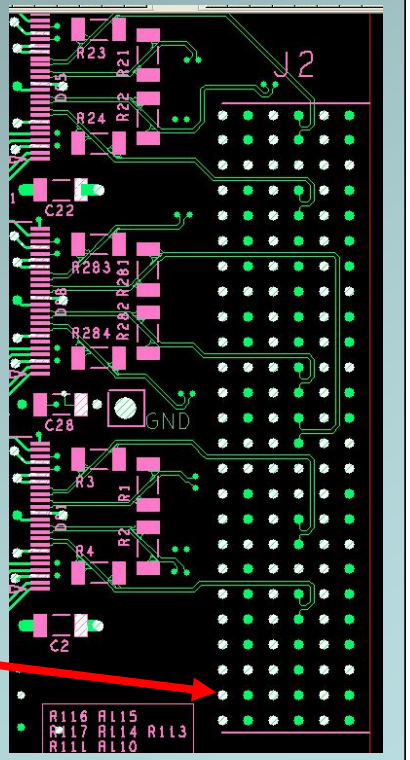
Impedance measure control



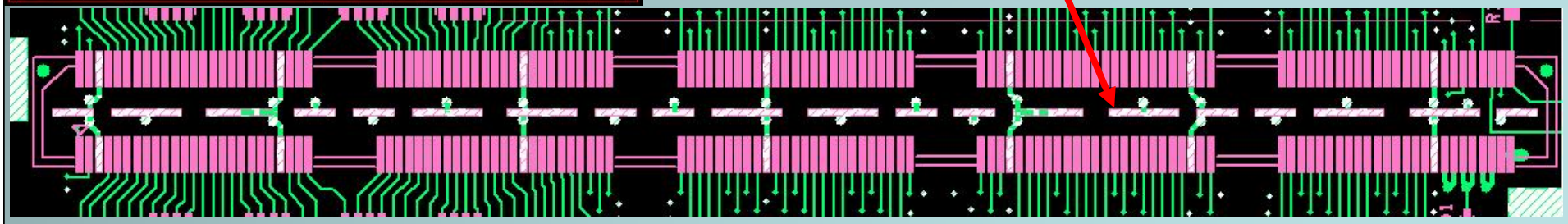
Others CEM rules….



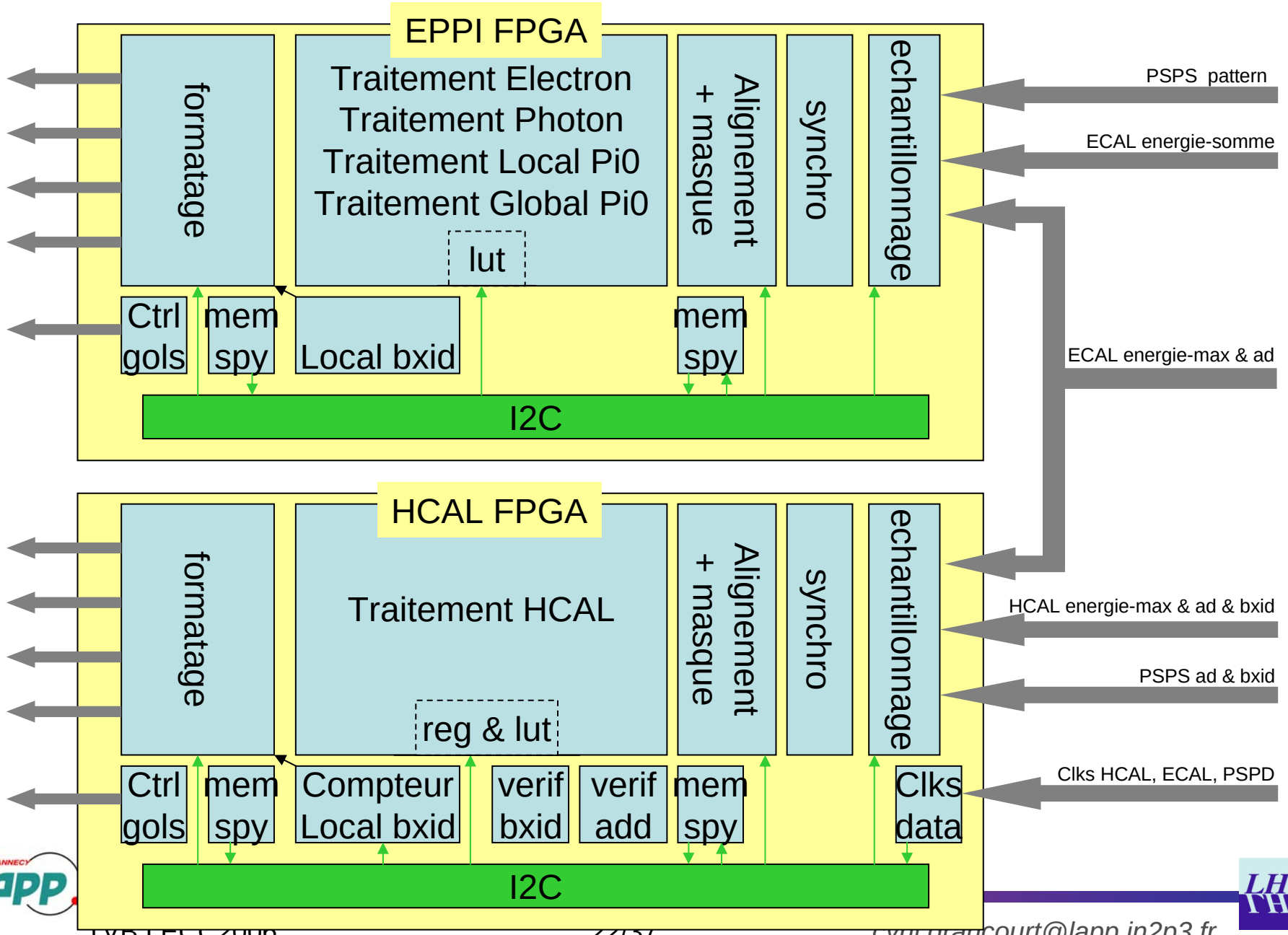
GND beld on each layers

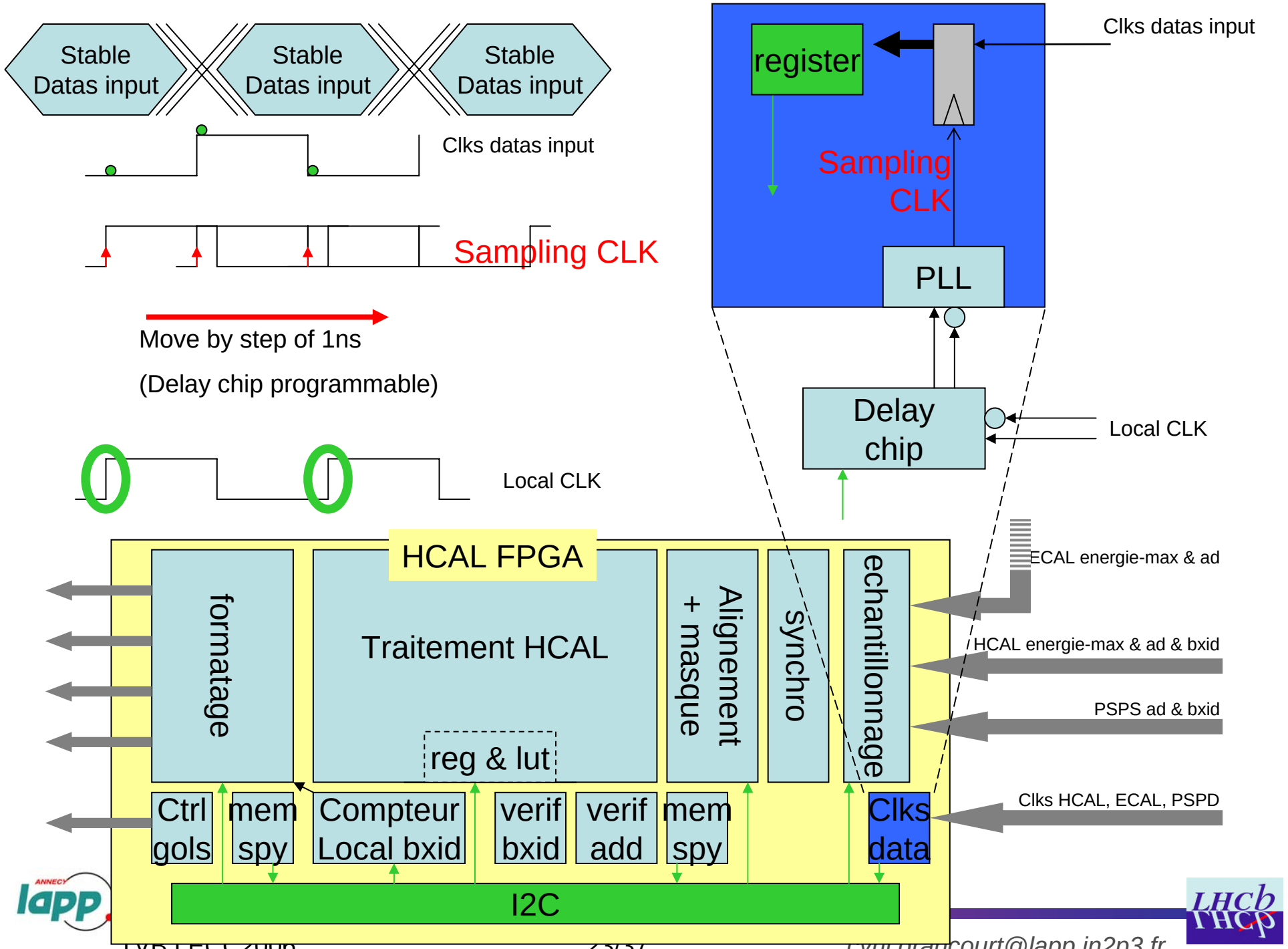


Connectors with many GND



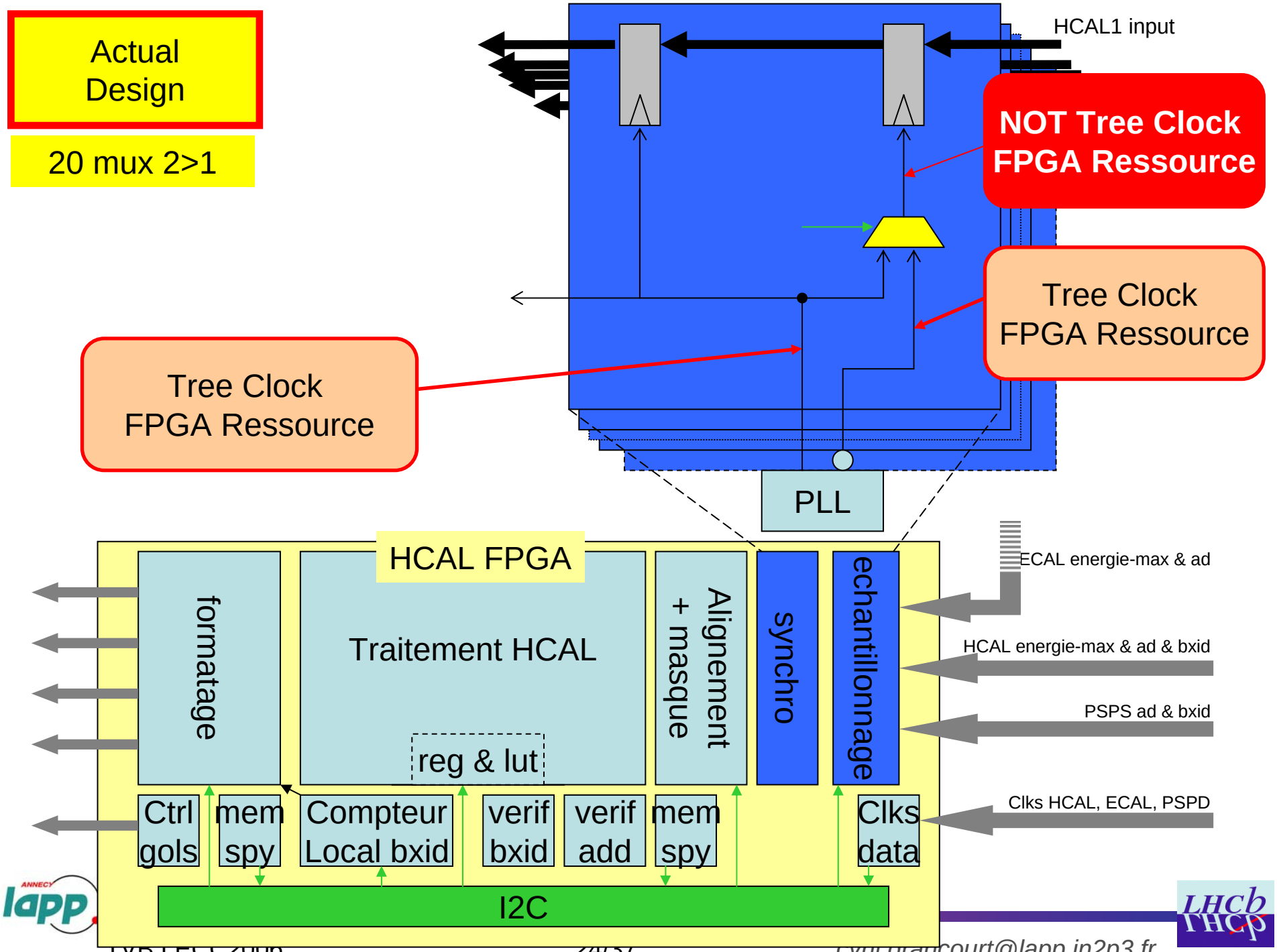
FPGAs Carte Validation (TVB) des calorimètres LHCb




Stable Datas input
Stable Datas input
Stable Datas input
Clks datas input
Sampling CLK
Move by step of 1ns
(Delay chip programmable)
Local CLK
register
Clks datas input
Sampling CLK
PLL
Delay chip
Local CLK
HCAL FPGA
formatage
Traitement HCAL
reg & lut
Alignement + masque
synchro
echantillonnage
ECAL energie-max & ad
HCAL energie-max & ad & bxid
PSPS ad & bxid
Clks HCAL, ECAL, PSPD
Ctrl gols
mem spy
Compteur Local bxid
verif bxid
verif add
mem spy
Clks data
I2C

Actual Design

20 mux 2>1

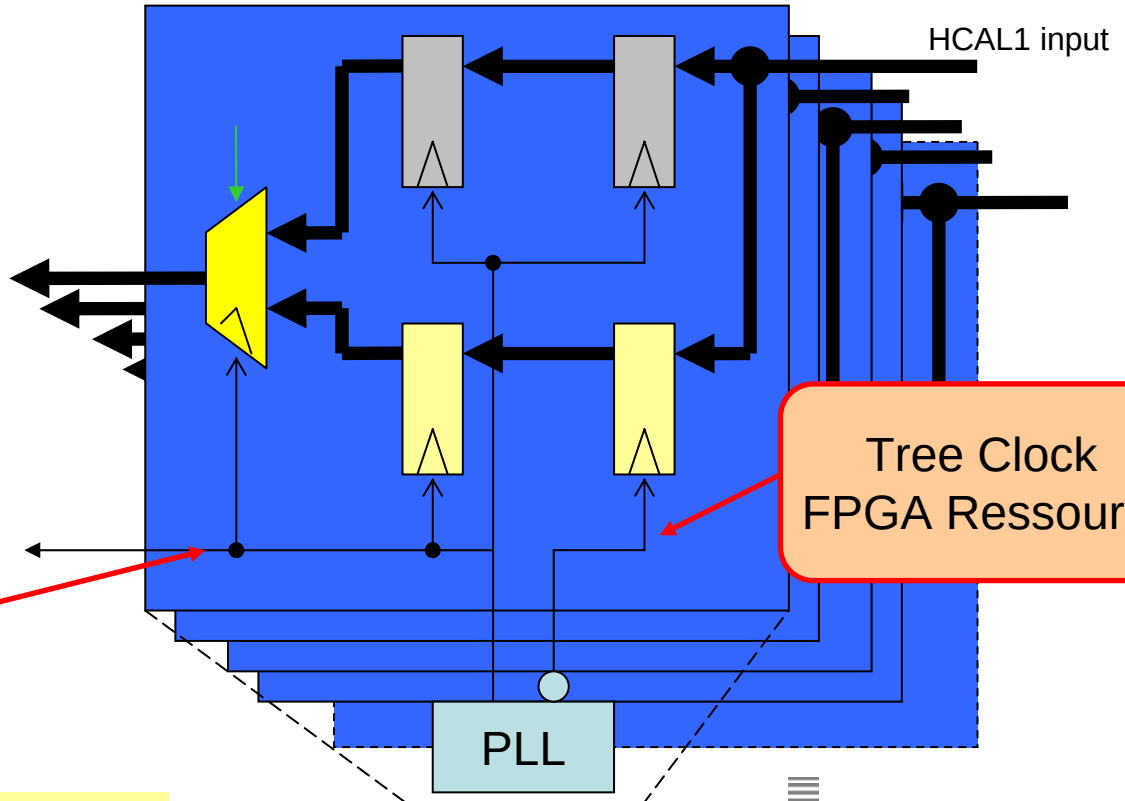


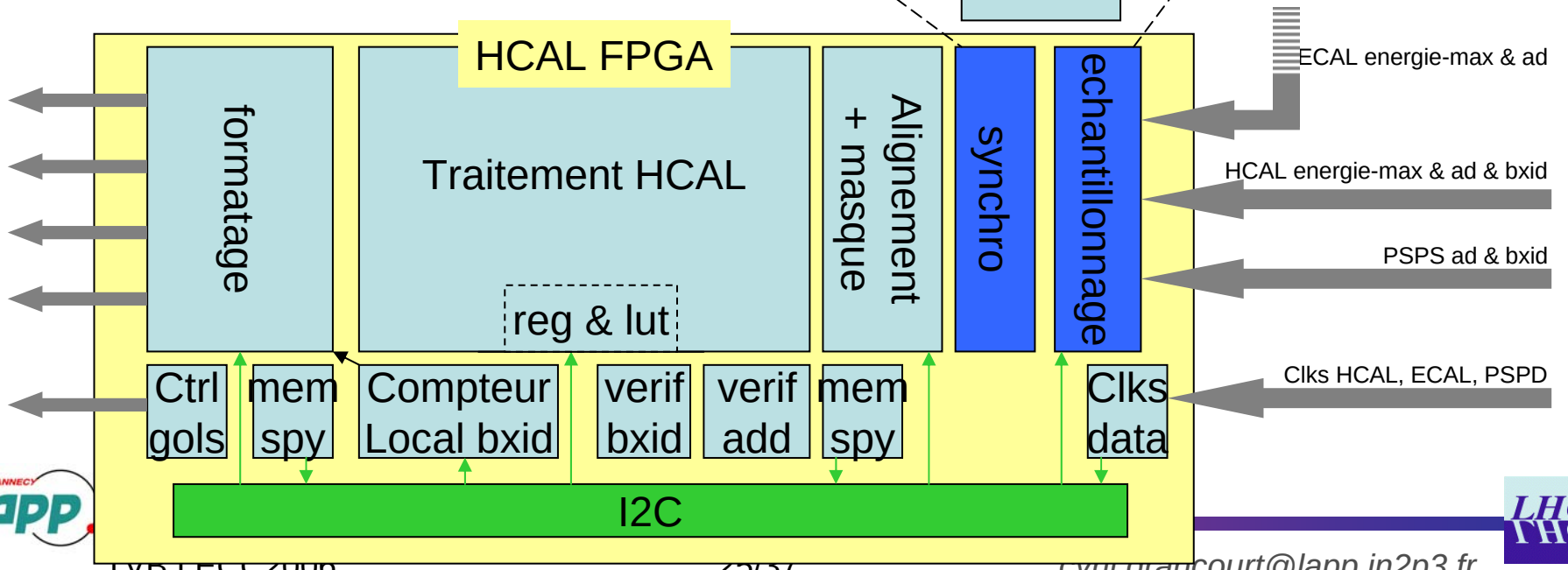
cyril.drancourt@lapp.in2p3.fr

Other
Solution:
Not tested
(Not implemented)

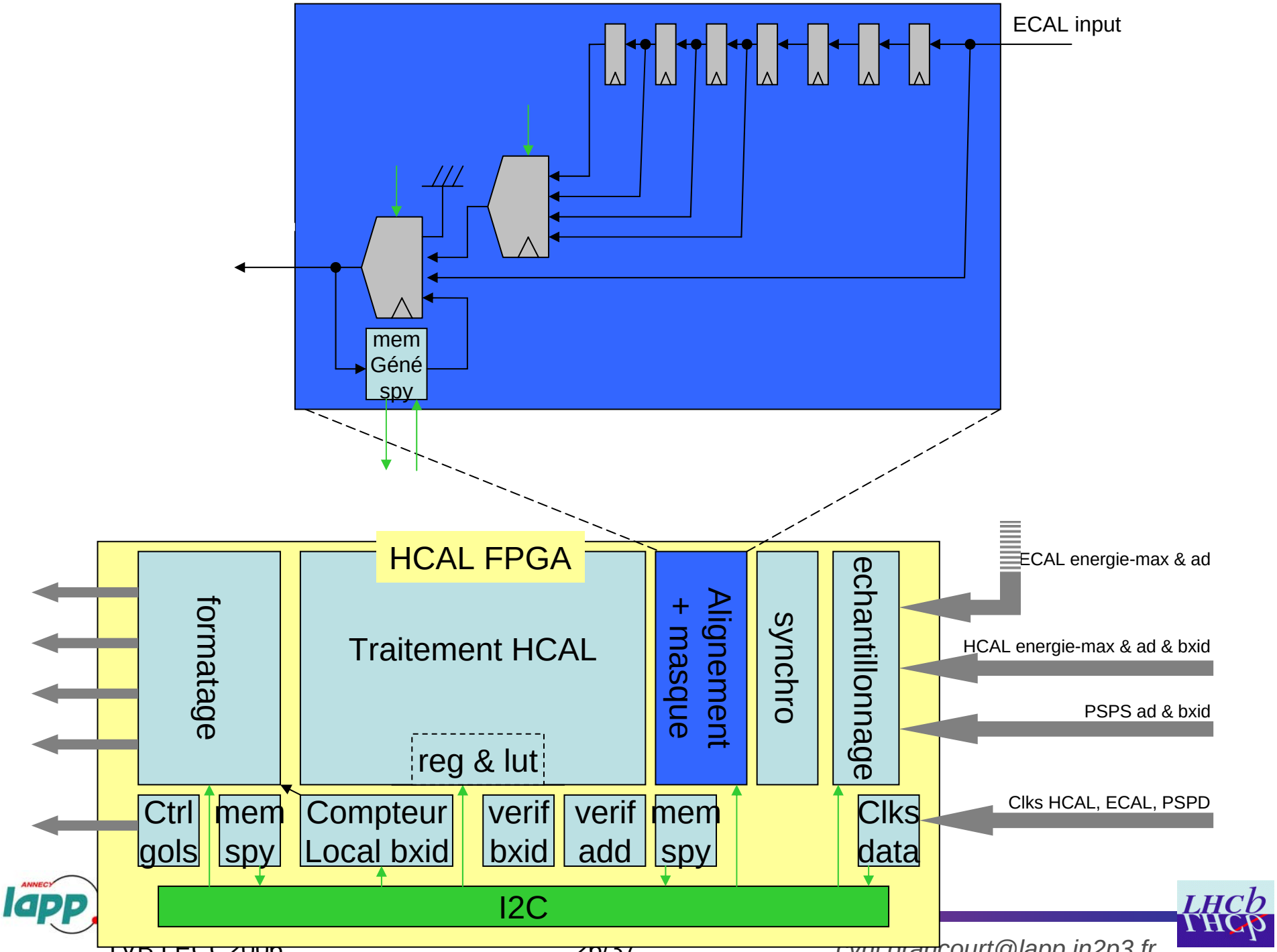
280 mux 2>1

+ 560 flipflop added

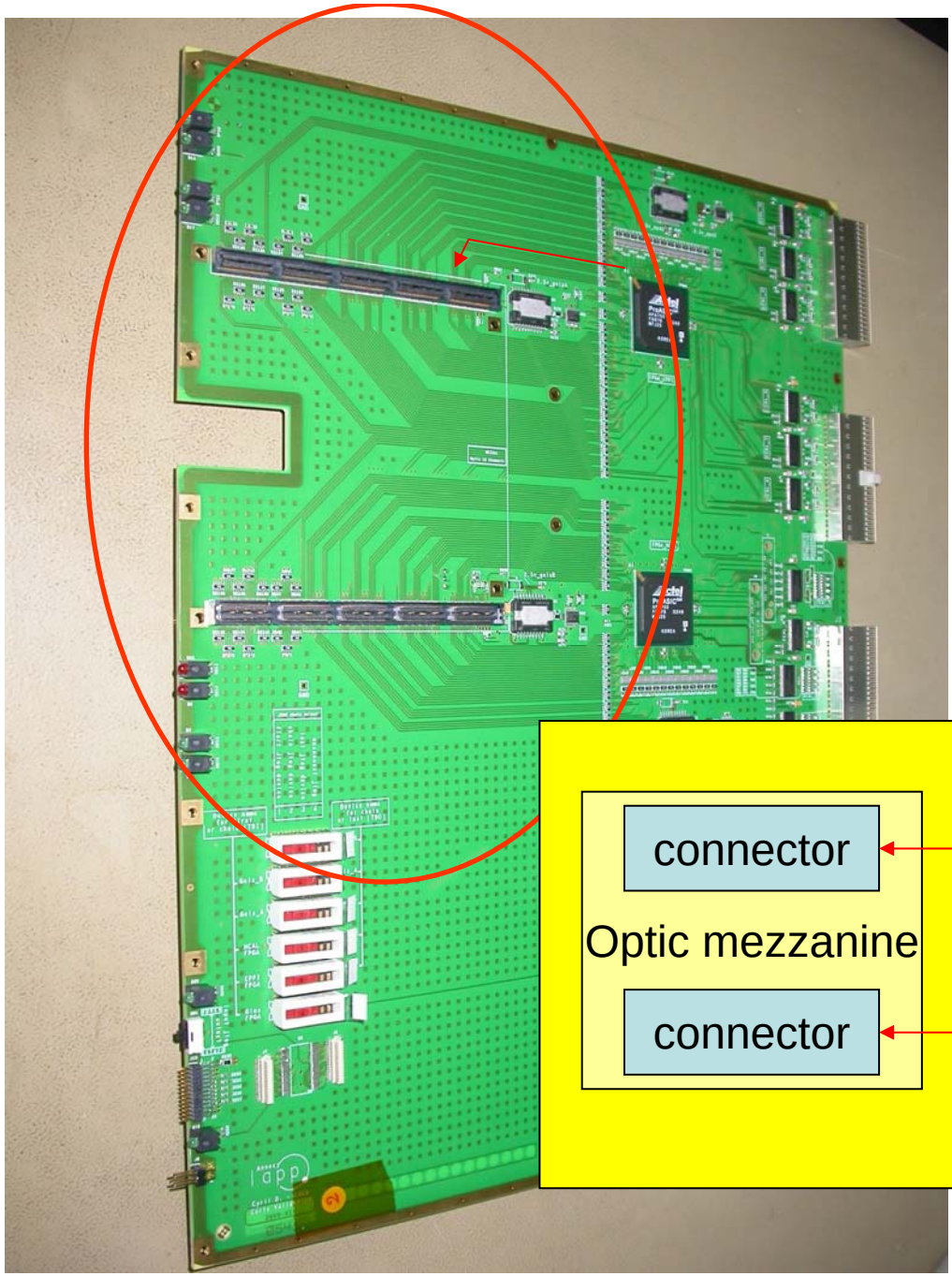




cyril.drancourt@lapp.in2p3.fr



cyril.drancourt@lapp.in2p3.fr



Outputs FPGAs:
40MHhz

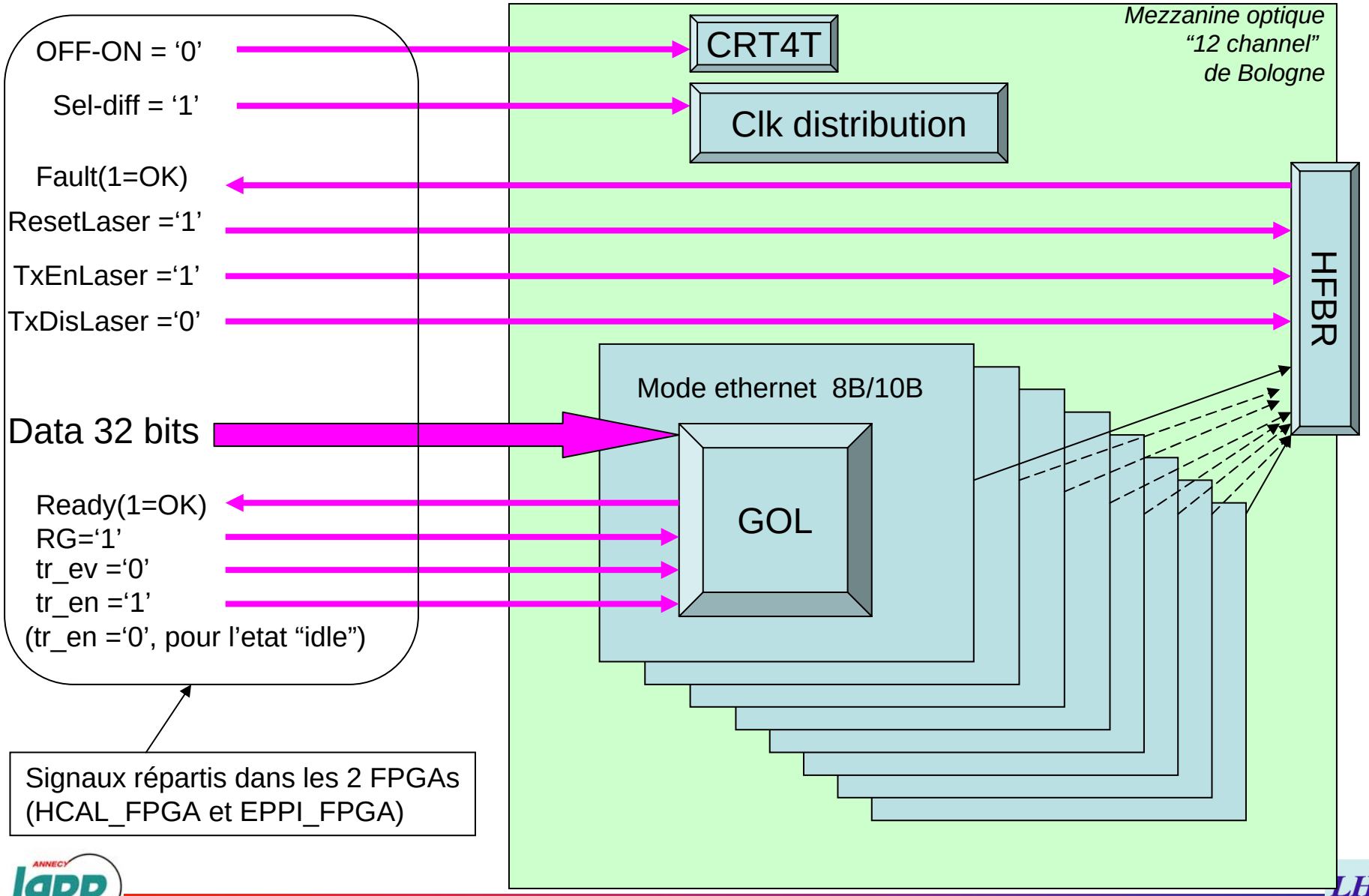
128 bits from EPPI
+ ctrl signals

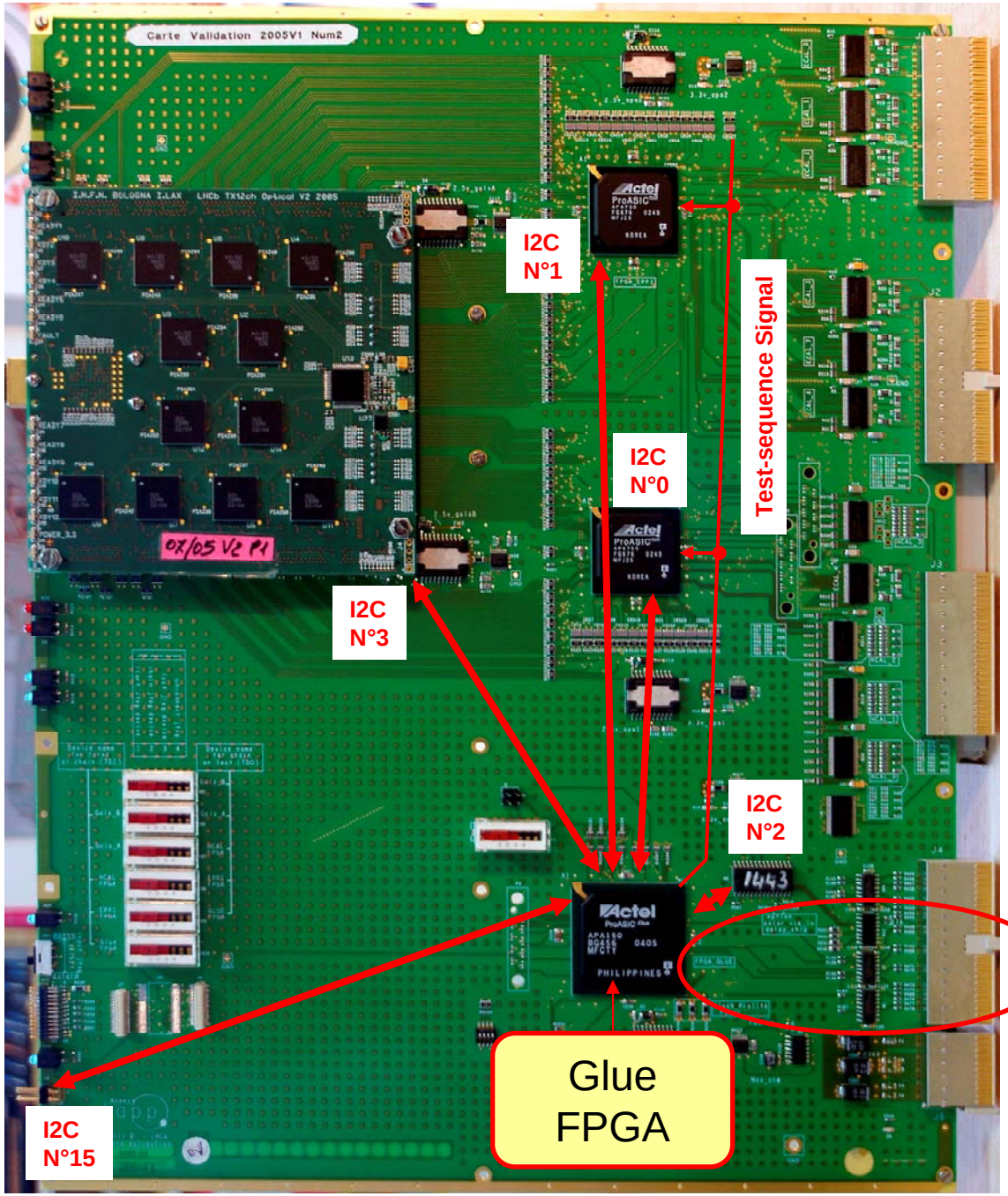
128 bits from HCAL

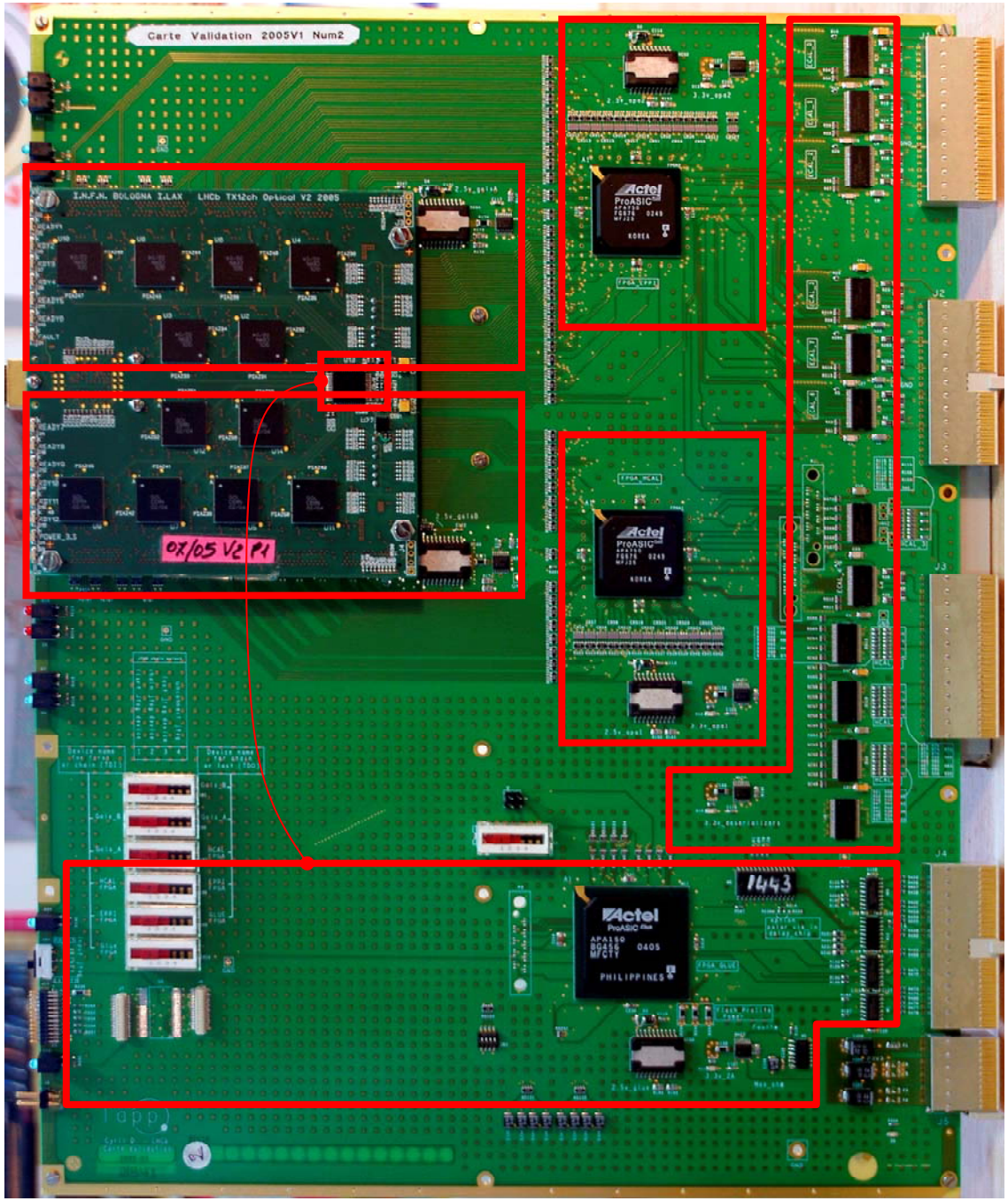
Output TVB

Transmission optique depuis la carte validation

Etat des signaux pour transmettre…..:



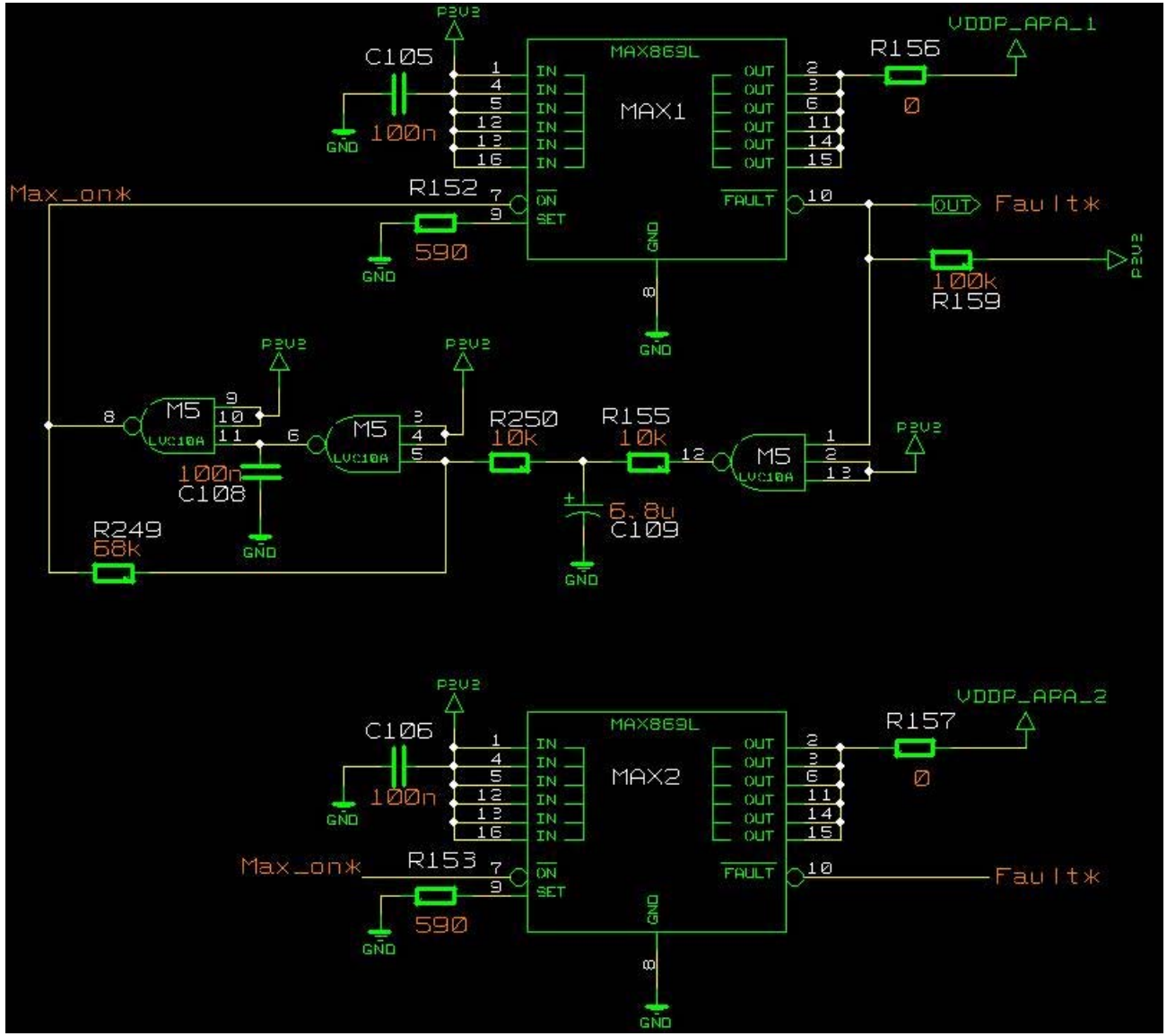

Carte Validation 2005V1 Num2
I2C N°1
I2C N°0
I2C N°3
I2C N°2
I2C N°15
Test-sequence Signal
Glue FPGA
Glue FPGAs
Specs interface
Specs Link With CROC



Power Area

With Delatcher

Radhard tolerant design (1)



- Power off all components on the board in case of latchup
- Auto power on after small delay

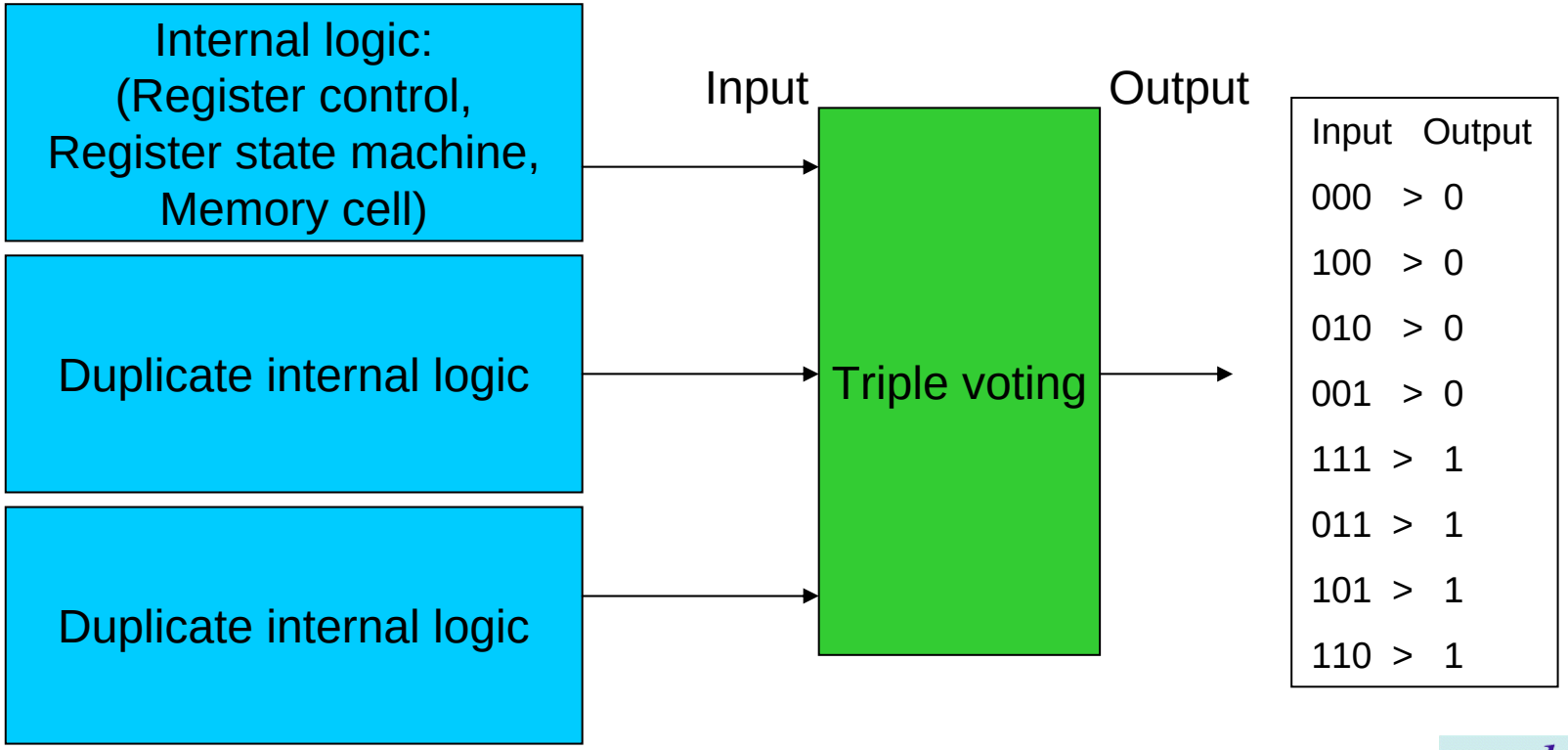
Radhard tolerant design (2)

•All components are tested on beam test.

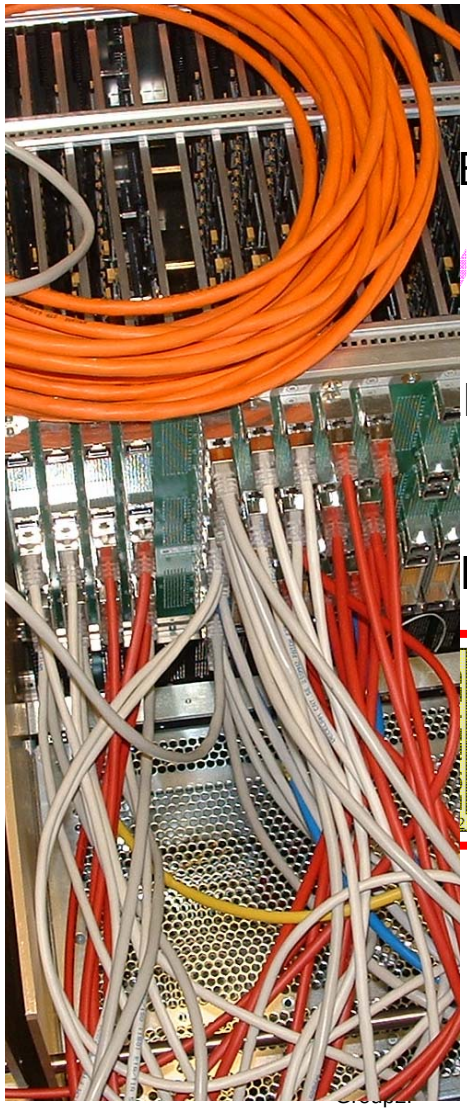
•About FPGAs, We use ACTEL, family “ProAsicPlus”.

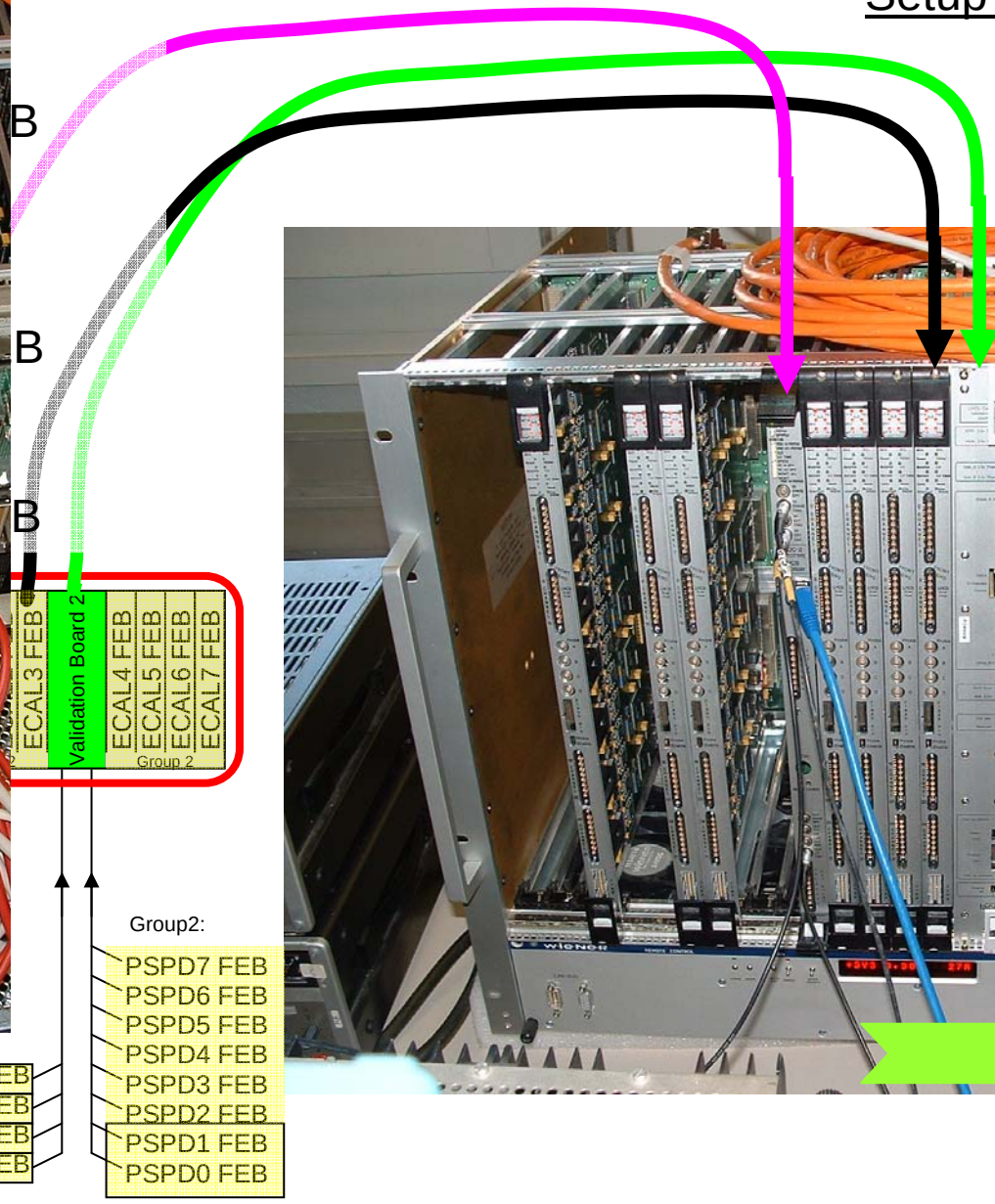
Some Nasa tests in 2004 show the SEU report.

To perform the design, we implement inside redundancy technique with triple voting.

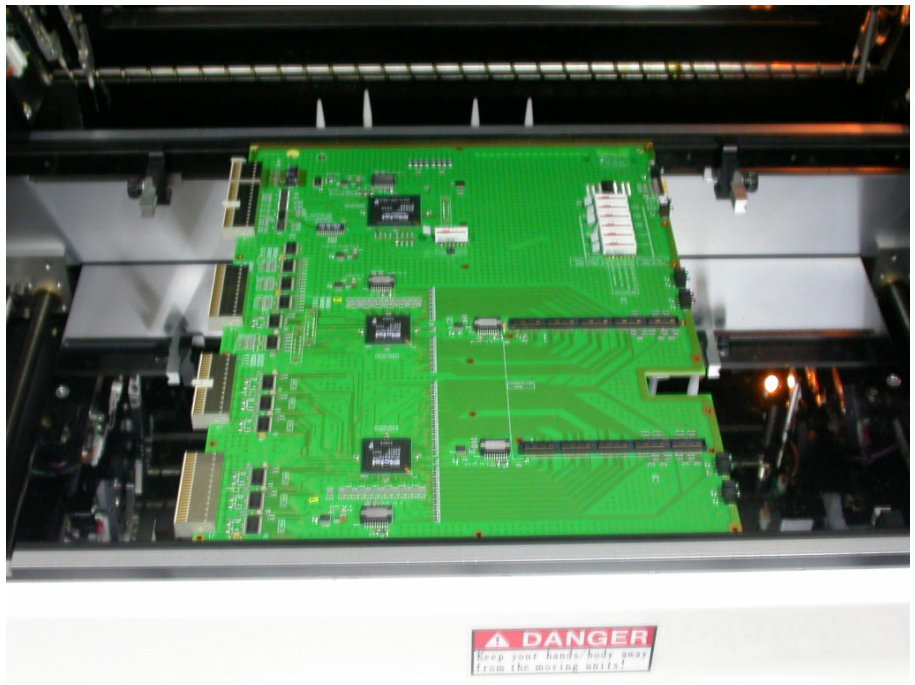


Setup test – CERN Today:





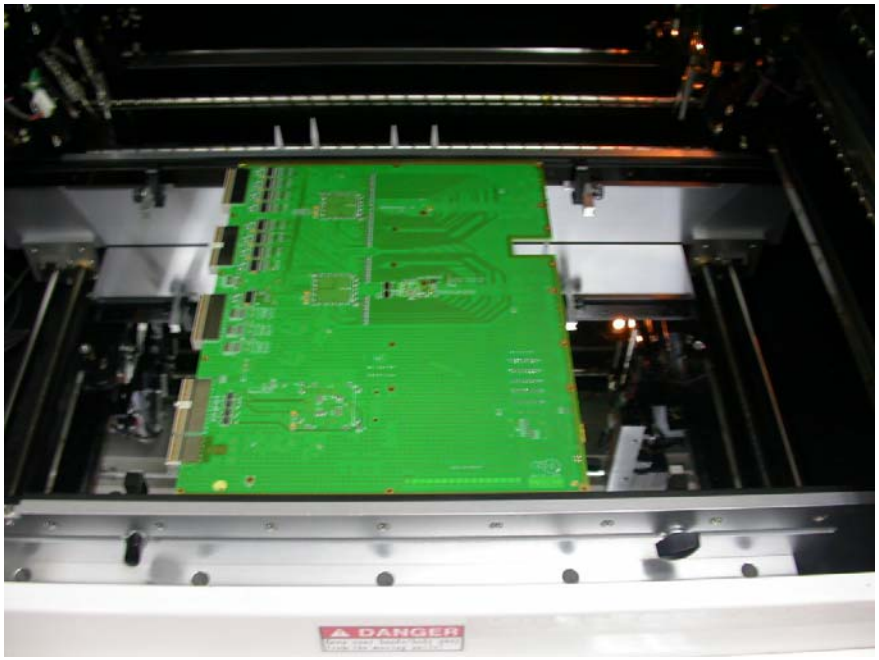
100% total inputs tested of TVB



Takaya
Test

by manufacturer

(Flying probe)

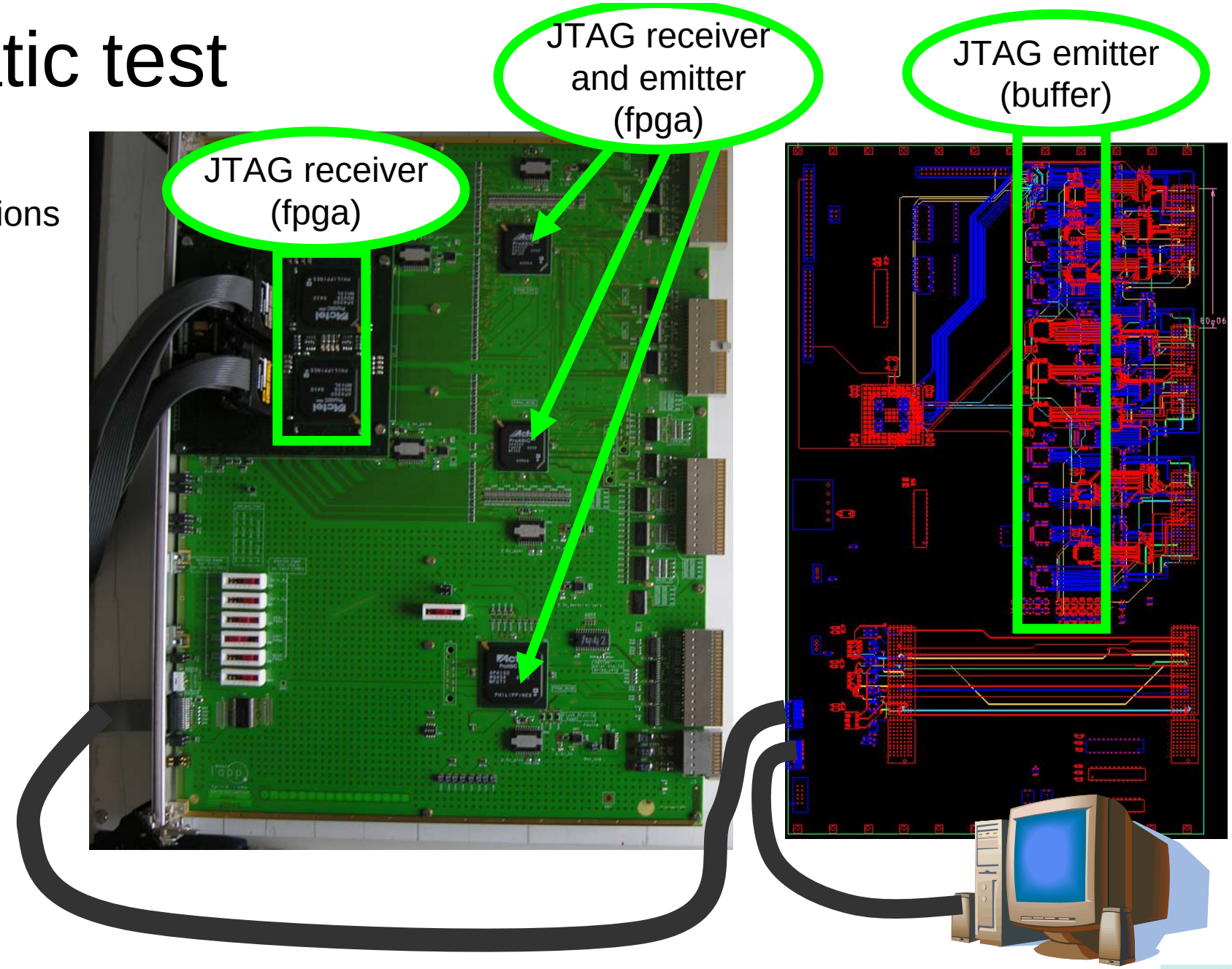


90 % of
discrete
componant
are tested

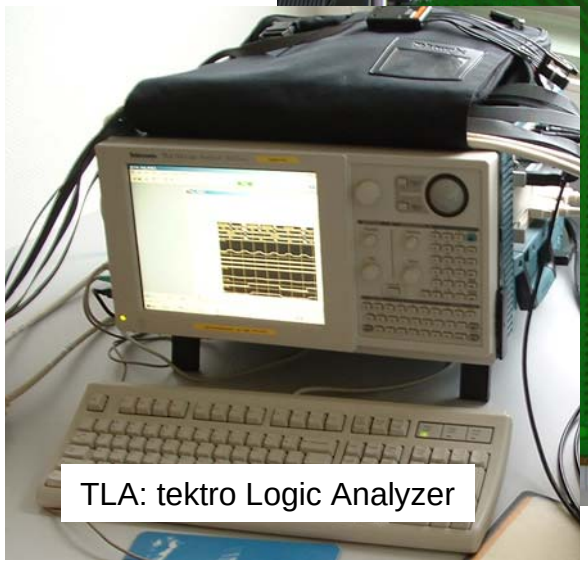
static test

95% connexions

cover

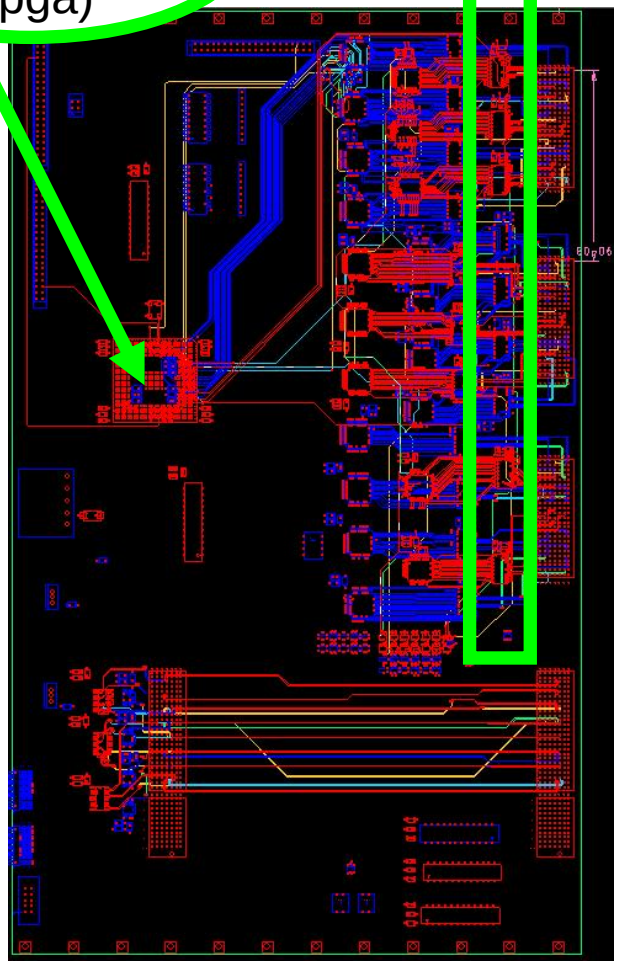


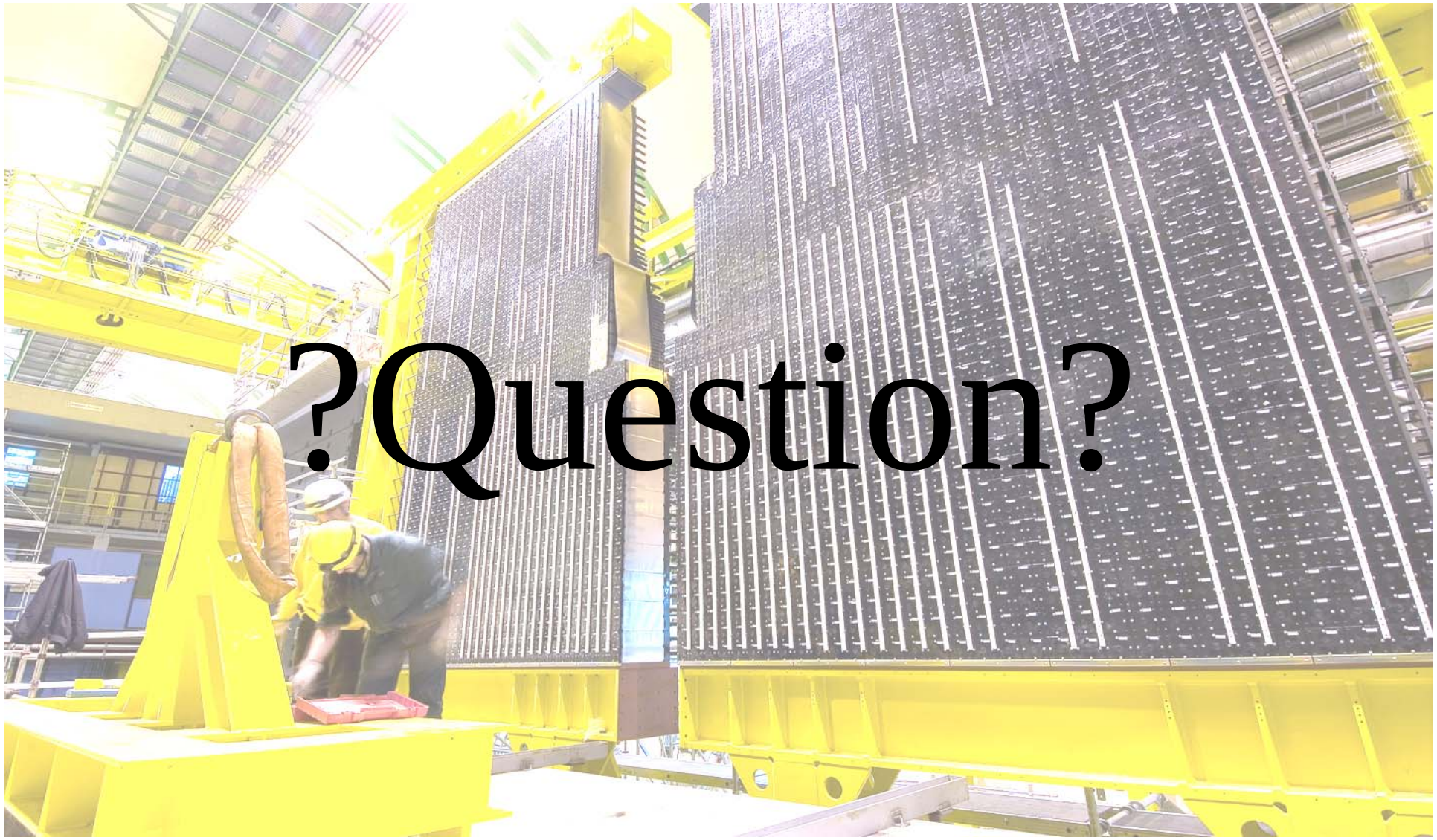
dynamic test



Data 40MHz generator (fpga)

20 Serializers




?Question?