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LHCb Calorimeter Trigger : Validation Board

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The Validation board participates in the electronic for triggering system of LHCb calorimeter detector.
The board, designed in Annecy-le-vieux Laboratory (LAPP-France), has logic radiation tolerant components: programmable logic, LVDS deserializer, 1.6Gbits optic transmitter.
The inputs come from Front-end board of 4 different detectors (Electromagnetic, Hadronic, PreShower, Scintillator-Pad) by backplane board or shielded twisted pair long cable.
All inputs transmit serial data in LVDS level at 280MHz. The treatment is implemented in 2 large Actel FPGAs cadenced at 40MHz.
The outputs go through an optic mezzanine driven a 12 Channels fibber ribbon.

Summary

The first prototype of the validation board was finished in October 2005. It works without fault. The methology of the design will be exposed: schematic, layout, EMC rule.
The board process 440 input bits and create 256 output bits at 40Mhz. Speed, environment,
material and component choice will be described.
This board will be in the Cavern of LHCb detector. The PCB is with free halogen dielectric, all components must be protected in case of latch-up and redundancy is implemented in Actel ProAsicPlus FPGA.
We choice 676 BGA Package, the PCB is high density with 16 layers, 250µm via and 2.4mm thickness. All CEM rules are used: Clock routing, adapted net, plane, Shielded belt around board, connector. Presentation will show one detail of each rule in the Layout of Trigger Validation Board.
To test all connectivity of the board, we are using several techniques: Flying Probe Test, Boundary Scan Test, dynamic test with bit pattern generator and logic analyzer, dynamic test with spy-memory inside FPGA. 100% of components and nets are tested. The contribution impact of these 4 processes will be shown.
Some inputs are driven by a long cable (15 meter) and signal inside have 280Mhz frequency. To perform this communication, Validation Board has pole zero compensation near the receiver. The motivation of this implantation and the related results will be discussed.
Inputs come from several other electronic rack and crate with several length of cable (2 meter to 15 meter). The mechanism used to synchronise the inputs inside FPGAs will be presented.
At the end, all dialog of this board in the experiment and the result of actual test setup are shown.
To conclude, this talk shows :
• how design a PCB with high speed and high density ;
• what are the important CEM rules ;
• what we must include at the beginning of a conception for the test board ;
• some radiation protection solution ;
• how synchronise many high speed inputs.

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