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Evaluation of Data Transmission at 80MHz and 160MHz Over Backplane, Copper and Optical Links

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The results of data transmission tests over custom backplane, copper and optical links at a multiples of the LHC bunch clock frequency are presented. We have evaluated a parallel data transmission at 80MHz and 160MHz using the GTLP and LVDS standards as well as serial copper and optical links operating at 3.2Gbps.

Summary

The bunch clock frequency of the LHC accelerator at CERN is specified at 40.07897 MHz. Most of the LHC experiments will utilize this frequency (or its multiples or derivatives) as the main frequency of data transmission for their Trigger and DAQ electronic systems. For example, the triggering system of the Cathode Strip Chamber (CSC) Endcap Muon sub-detector at the CMS experiment utilizes data transmission at a doubled LHC frequency for most of its data paths, including the LVDS links from an on-chamber electronics to peripheral crates; custom peripheral and Track Finder GTLP backplanes; optical links between the peripheral and Track Finder crates.

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A proposed  Super-LHC (SLHC) upgrade with increase of the operating frequency
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will be challenging for many synchronous data transmission systems. The goal of this work was to evaluate possible solutions for data transmission at 80MHz and 160MHz suitable for the SLHC era. We have used an existing hardware designed for the CSC electronic system for the evaluation of data transmission at 80MHz and 160MHz using the LVDS and GTLP logical standards. We have designed a new evaluation board to study the optical and copper links operating at 3.2Gbps. The results of measurements and possible solutions are presented.

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