Contribution ID: **120** Type: **Oral**

Technology Scaling and CMOS Analog Design

Thursday 28 September 2006 09:45 (45 minutes)

Modern and future ultra-deep-submicron technologies make challenging the analog design especially when power consumption must match digital counterparts. The decrease of the supply voltage reduces the voltage headroom in analog circuits, the gate leakage current increases, the voltage gain decreases in planar bulk transistors, 1/f noise deteriorate when using new high-k gate dielectrics. The transistor and passive components mismatches give rise to large inaccuracies. Only some of these problems can be solved at the technology level; others require new circuit topologies and design techniques. The increased digital processing capability not only pushes the analog-digital interface toward more and more digital, thus limiting the analog design to very first interfaces and data converters, but also enables to use digital methods for the correction and digital assisted analog design. Several of the solutions currently proposed for analog pre-processing and data converter design are discussed in this paper.

Author: MALOBERTI, Franco (University of Pavia)

Co-author: MALOBERTI, Franco (University of Pavia)

Presenter: MALOBERTI, Franco (University of Pavia)

Session Classification: Plenary Session P4-HEP electronic and ASIC trends