Level 0 trigger decision unit (L0DU) for the LHCb experiment

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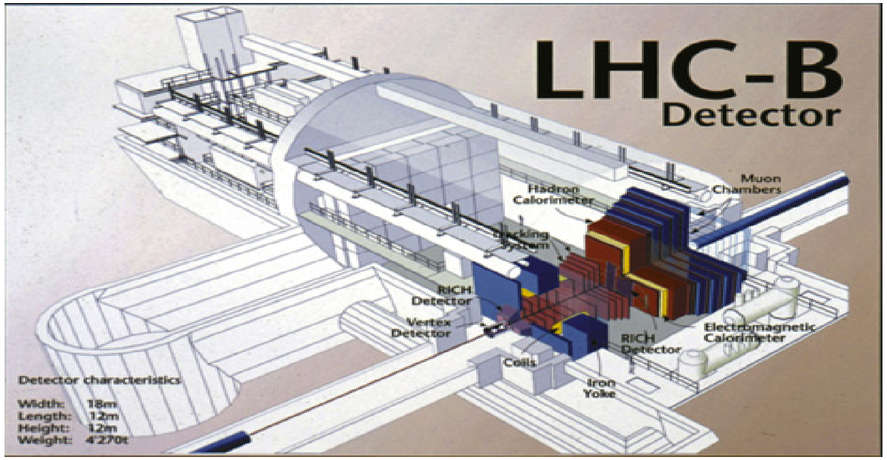
Outline



- ✓ **System overview:**
  - **- the LHCb experiment**
  - **- the Level 0 trigger**
  - **- input/output and timing**
  - **- L0DU set up**
- ✓ **The L0DU:**
  - **- L0DU board design**
  - **- board layout & simulation**
  - **- the test bench**
- ✓ **The L0DU processing:**
  - **- algorithm requirements**
  - **- global architecture**
  - **- conclusion**

PART I:
System overview

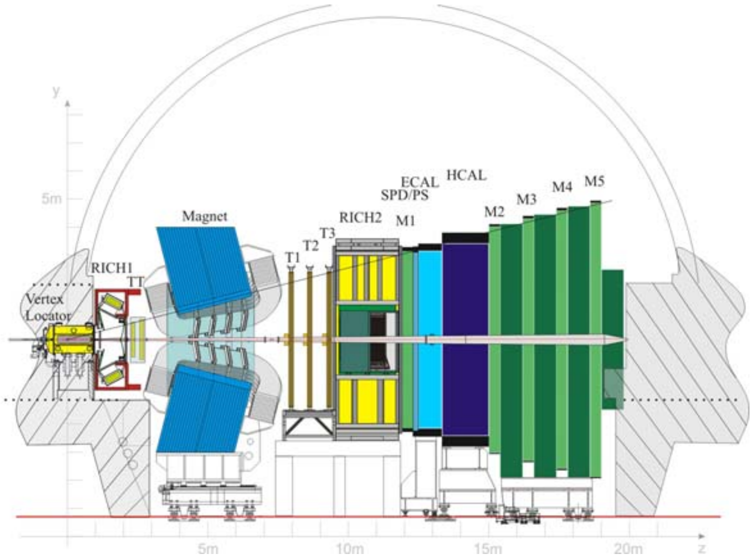
LHCb experiment

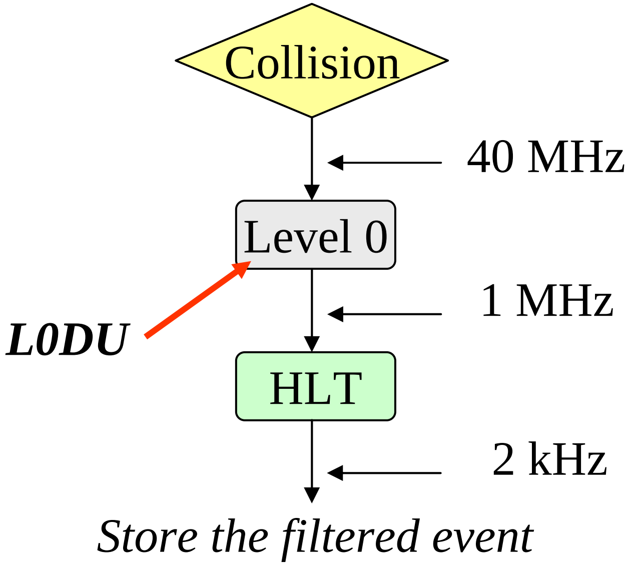
- **<u>Aim:</u>**
  Measure the CP violation in B decays

- Proton/proton **collisions occur** @ **40 MHz**

- Due to the high quantities of produced data, an **on-line selection system** of interested events is implemented:
  - a specific channel for the **D**ata **A**cquisition (DAQ)
  => *assembles data corresponding to a collision*
  - and a trigger channel

- Trigger channel composed of:
  - an hardware level, Level 0 trigger
  - a software level, High Level Trigger (HLT)





Collision

40 MHz

Level 0

1 MHz

L0DU

HLT

2 kHz

Store the filtered event

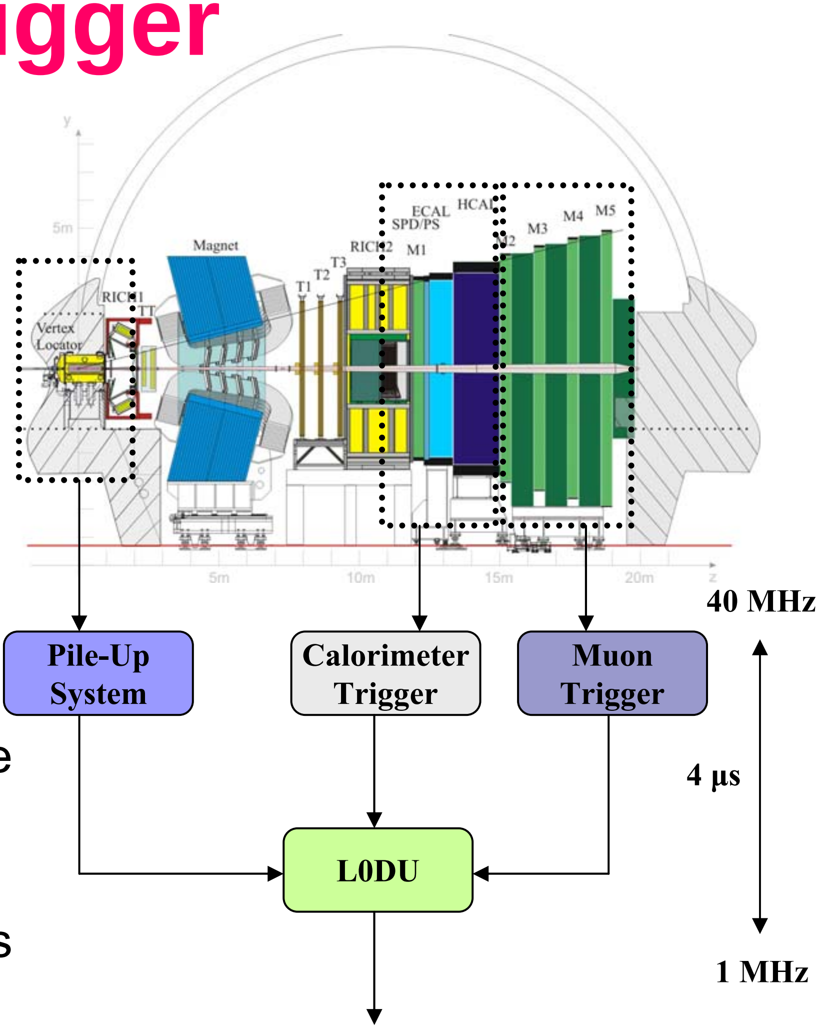
Overview of the L0 trigger

- **Composed of four custom processors:**
  - L0 Calorimeter trigger
  - L0 Muon trigger
  - L0 Pile-Up system
  And
  The Level 0 Decision Unit (L0DU)

- Reduce the data flow down to 1 MHz for the next trigger level

- System fully synchronous, pipeline architecture
  => each event is processed
  => a decision is produced every 25 ns and the system is able to generate consecutive triggers

- **A physics algorithm is applied to select events** and to deliver the L0DU decision



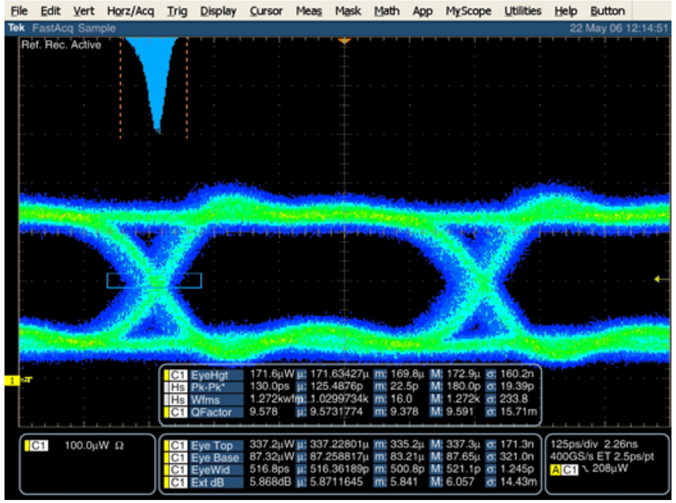
L0DU Input

- All the L0 trigger processors send their data via **optical links**
  => 24 optical inputs at 1.6 Gb/s

Twelve links ribbon with female M PO connectors

- Use of two fibber ribbons of 12 single fibers

- **Expected input data flow** : 864 bits@40MHz



```
Tek  FastAcq Sample                                                          22 May 06 12:14:51
Ref. Rec. Active

C1 EyeHgt   171.6µW  µ: 171.63427µ  m: 169.8µ  M: 172.9µ  σ: 160.2n
Hs Pk-Pk*   130.0ps  µ: 125.4876p   m: 22.5p   M: 180.0p  σ: 19.39p
Hs Wfms     1.272kwfmµ: 1.0299734k  m: 16.0    M: 1.272k  σ: 233.8
C1 QFactor  9.578    µ: 9.5731774   m: 9.378   M: 9.591   σ: 15.71m

C1  100.0µW  Ω
C1 Eye Top  337.2µW  µ: 337.22801µ  m: 335.2µ  M: 337.3µ  σ: 171.3n   125ps/div  2.26ns
C1 Eye Base 87.32µW  µ: 87.258817µ  m: 83.21µ  M: 87.65µ  σ: 321.0n   400GS/s ET 2.5ps/pt
C1 EyeWid   516.8ps  µ: 516.36189p  m: 500.8p  M: 521.1p  σ: 1.245p   A C1 ⌐ 208µW
C1 Ext dB   5.868dB  µ: 5.8711645   m: 5.841   M: 6.057   σ: 14.43m
```

Eye diagram for a 1.6 Gb/s optical link

L0DU Output

- **Decision word:**
  => 16bits@40MHZ

- **DAQ word:**
  => 1024 bits@1MHz for off-line monitoring purpose

L0DU timing

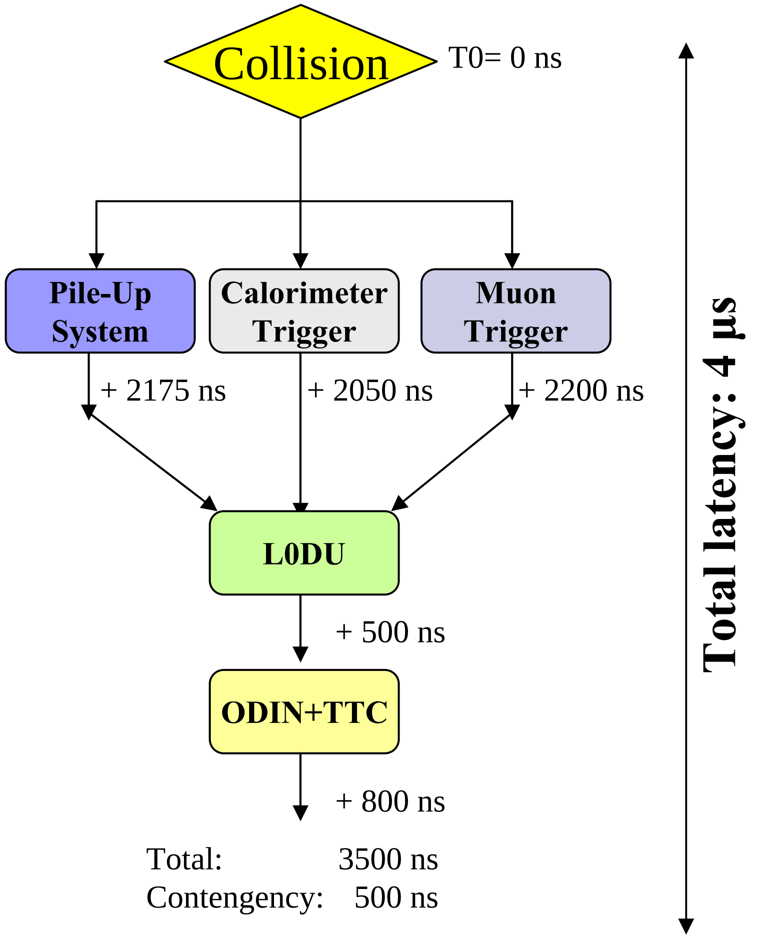
- L0DU is synchronized by the Timing and Trigger Control (TTC) which delivers:
  - the LHC clock
  - reset and trigger signals

- Events are processed in time order
  => Use of a pipeline architecture

- Input FIFO for time domain interfacing

- Each L0 sub-trigger has a fixed latency
  => Need to align in time the incoming data
  => Specific procedure to determine the latency
  => Monitoring of the time alignment

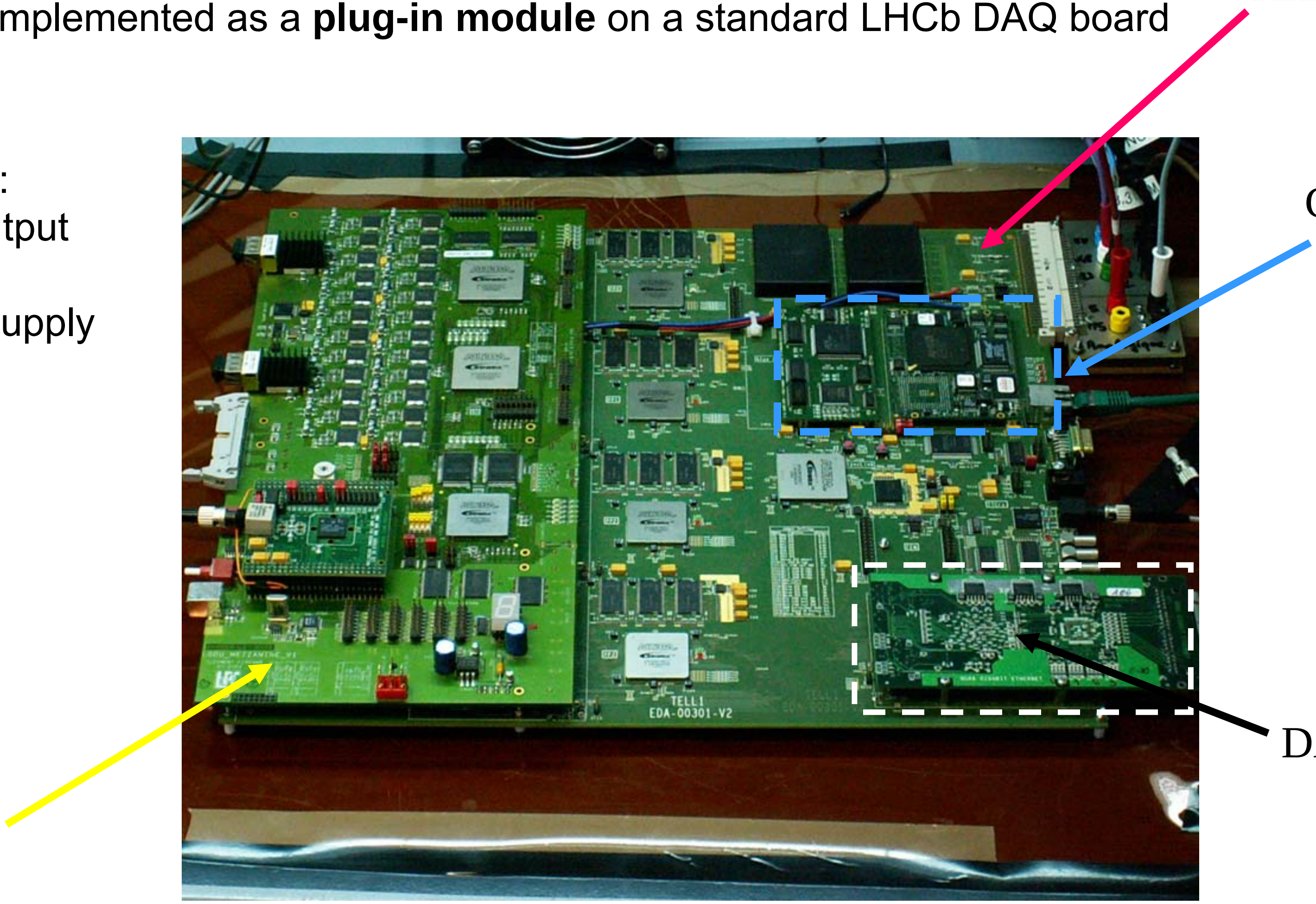
- Latency budget for the L0DU is 500 ns



Standard LHCb DAQ board (TELL1)

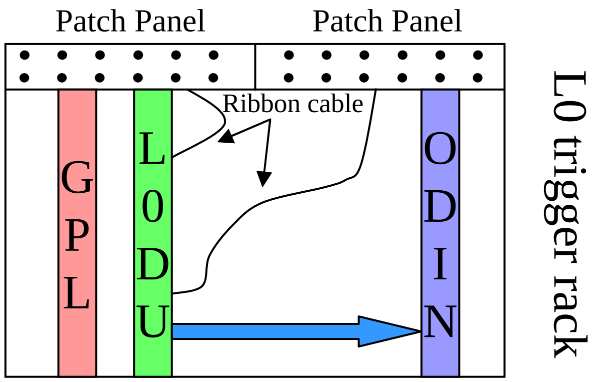
- L0DU is implemented as a **plug-in module** on a standard LHCb DAQ board (TELL1)

- Used for:
  - DAQ output
  - control
  - power supply
  - JTAG

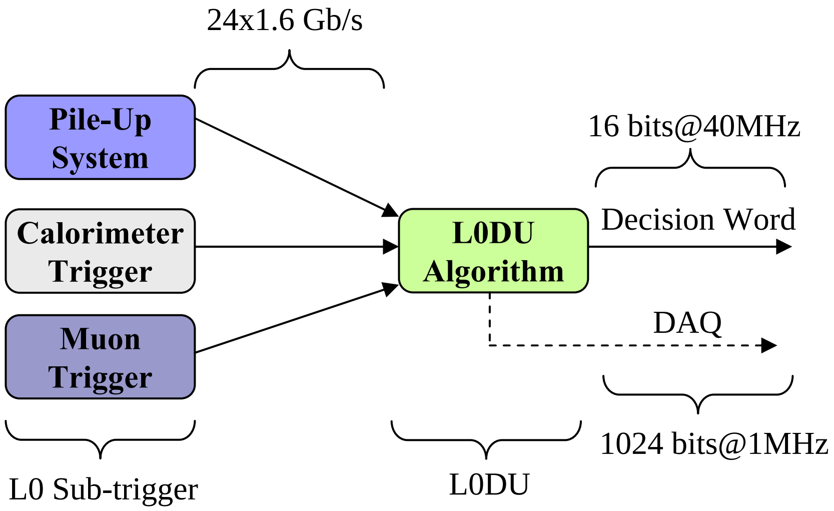


L0DU data flow

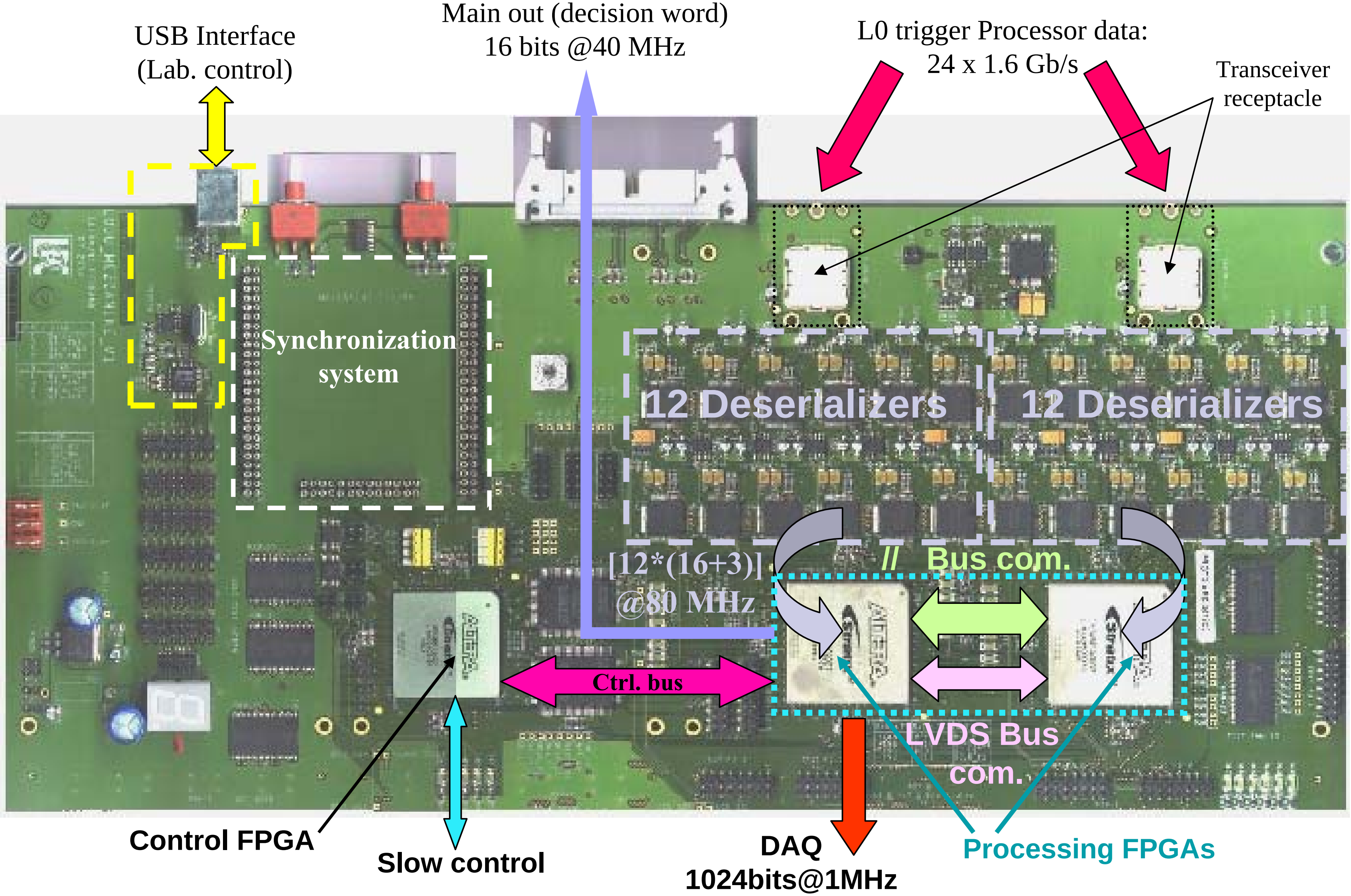
- The main data flow does not use the TELL1 board
- The main data flow is:
  - L0 sub-trigger data sent to L0DU
  - L0DU processing
  - Decision word sent to the TTC system driver (ODIN)
- Second data flow is sent to the DAQ under ODIN request



L0DU set up



PART II:
The L0DU board


USB Interface
(Lab. control)
Main out (decision word)
16 bits @40 MHz
L0 trigger Processor data:
24 x 1.6 Gb/s
Transceiver
receptacle
Synchronization
system
12 Deserializers
12 Deserializers
[12*(16+3)]
@80 MHz
// Bus com.
Ctrl. bus
LVDS Bus
com.
Control FPGA
Slow control
DAQ
1024bits@1MHz
Processing FPGAs

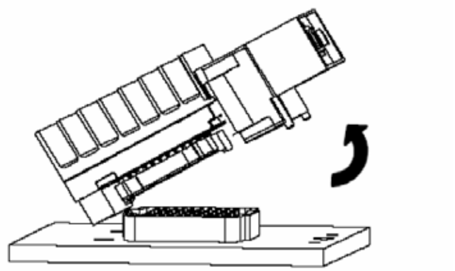
Optical design

- Composed by:
  - a reception module:
  => optical signal to copper differential signal
  - a clock distribution network low jitter

- The reception module is based on:
  - optical transceiver HFBR-782BE from Agilent
  => protected against EMI
  => use of a pluggable version with BGA support
  - deserializers TLK2501 from Texas Instrument:
  => 8-bit/10-bit encoding/decoding
  => jitter required for the clock reference, less than 40 ps

- The L0DU implements:
  - 2 optical transceivers
  - 24 TLK2501

Optical transceiver

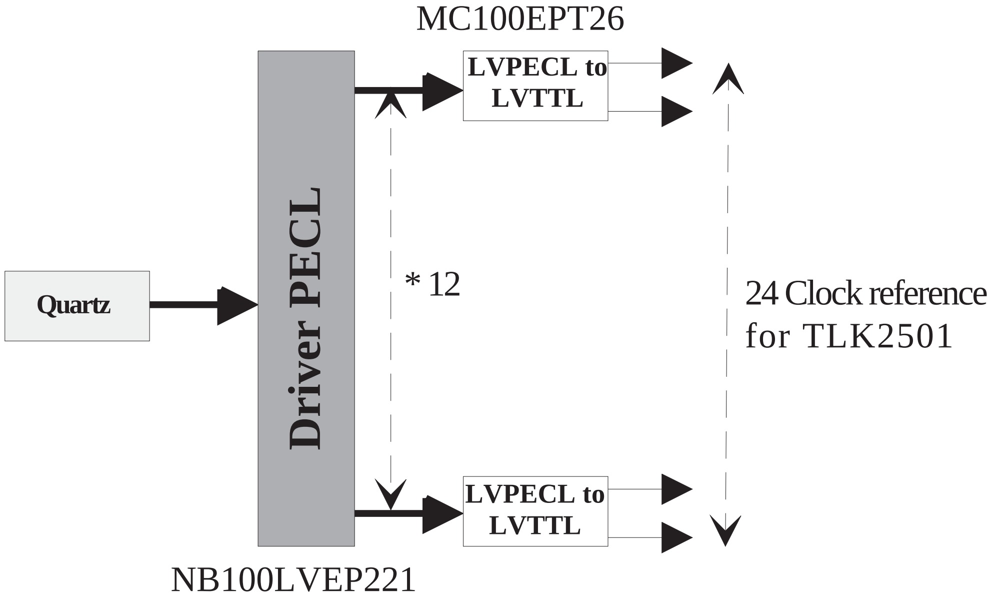


HFBR receptacle

Optical input power measurement

Optical design: clock network

- Each deserializer receives a clock reference issued from the clock distribution network composed by:
  - a local quartz at 80 MHz
  - a LVPECL fan-out
  - 12 LVPECL to LVTTL converters



MC100EPT26

Quartz

Driver PECL

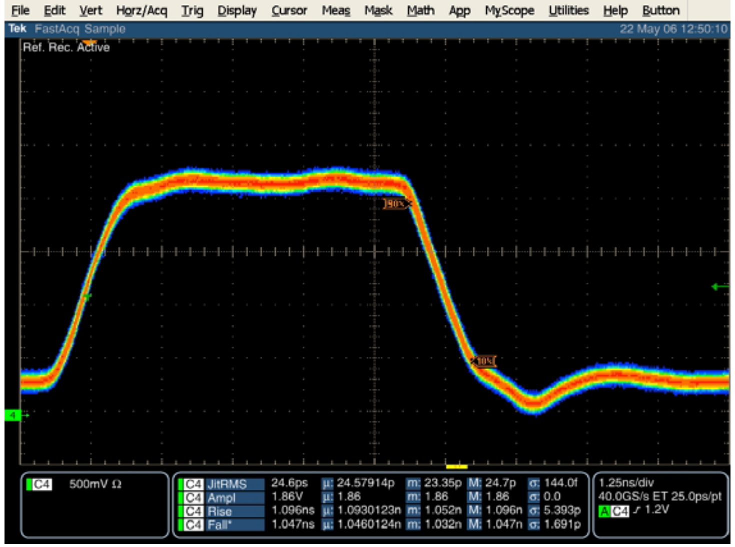
LVPECL to LVTTL

* 12

LVPECL to LVTTL

24 Clock reference for TLK2501

NB100LVEP221



File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek FastAcq Sample
Ref. Rec. Active
90%
10%
4

```
22 May 06 12:50:10
C4  500mV Ω
C4 JitRMS  24.6ps    µ: 24.57914p   m: 23.35p  M: 24.7p   σ: 144.0f
C4 Ampl    1.86V     µ: 1.86        m: 1.86    M: 1.86    σ: 0.0
C4 Rise    1.096ns   µ: 1.0930123n  m: 1.052n  M: 1.096n  σ: 5.393p
C4 Fall*   1.047ns   µ: 1.0460124n  m: 1.032n  M: 1.047n  σ: 1.691p
1.25ns/div
40.0GS/s ET 25.0ps/pt
A C4 ↗ 1.2V
```

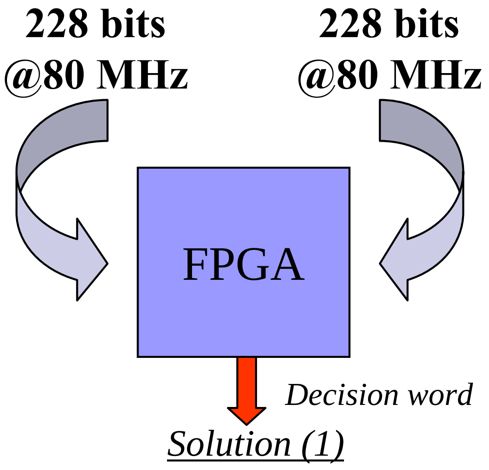
Clock jitter qualification

- Clock jitter measured at the input clock reference of each TLK2501

- Peak to Peak RMS value measured:
  18 ps < jitter < 30 ps

Design & Parallel communication bus

- <u>Two architectures have been studied:</u>
  (1) implementation of the processing in one FPGA
  (2) implementation of the processing in two FPGA



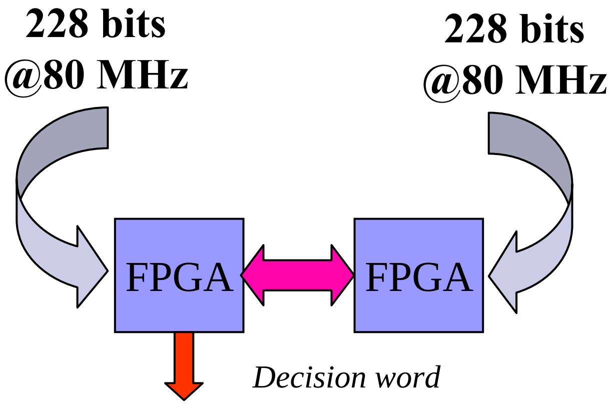
Solution (1)

Sol. n°	Advantages	Inconvenients
1	- Single FPGA with all L0 trigger data	- Board layout very complex - Wire lengths very different between the deserializers and the FPGA
2	- Board layout less complex - More easy to have equal length wire between deserializers and FPGA	- Need to centralize the L0 trigger data

- <u>Choice:</u> *Solution n°2*

- Need to add a **parallel communication bus** between the two processing FPGA **to centralize the L0 trigger data**

- <u>Characteristics:</u>
  - 160 wires
  - able to run @40 and 80 MHz



Solution (2)

Board Layout

- Layout complex due to:
  - high density of signals
  - frequency of the signals:

  1.6 GB/s *(tr,tf: 110 ps)*, 80 MHz *(tr,tf: 1 ns),*

- Must follow **specific design rules** for high speed signals, clock and power supply:
  - keep trace as short as possible
  - controlled impedance
  - keep the trace identical between the differential signals to prevent signal skew

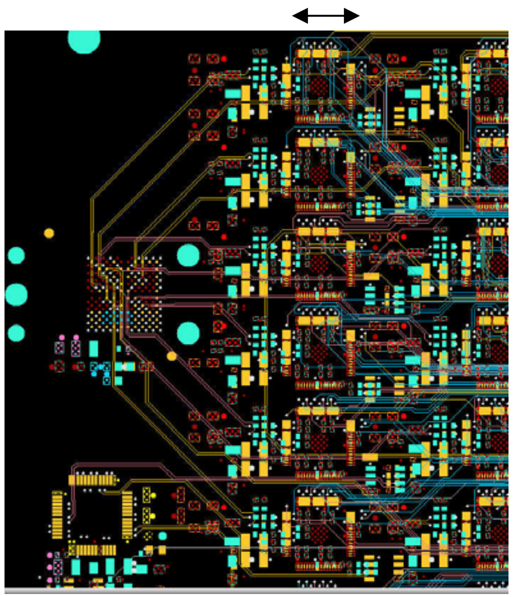
- All the critical parts of the PCB layout have been simulated:
  - interconnexion between transceivers and deserializers
  - interconnexion between deserializers and FPGA
  - interconnexion bus between the two processing FPGA

- PCB: 16 layers class 6

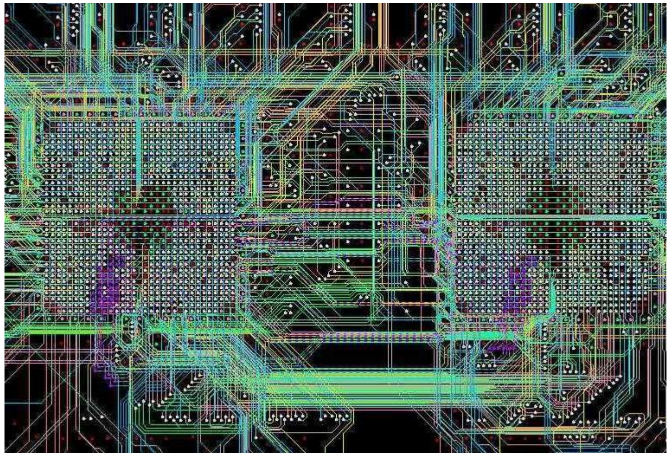
Length (mm)	Width (mm)	Depth (mm)
366.7	170	2

- Optical design area:

  => 100mm x 200mm (32% of total area)

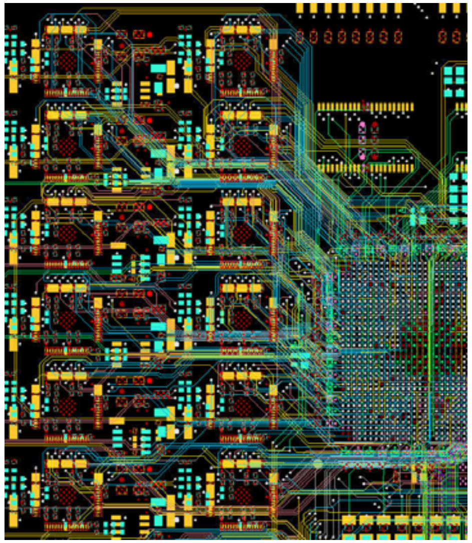


Transceivers => Deserializers

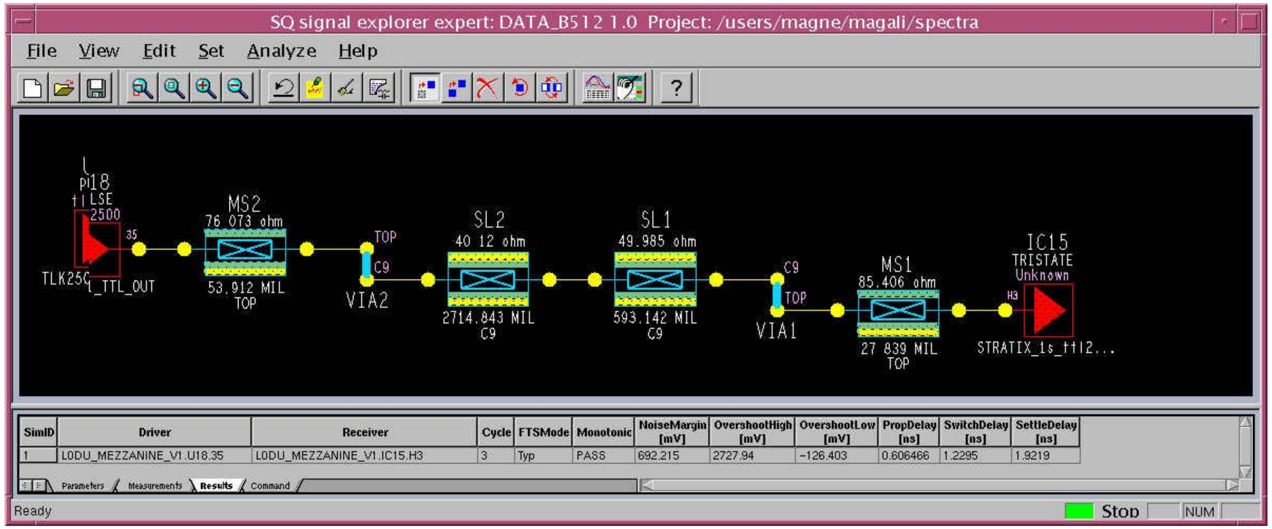


FPGA => FPGA

Board Layout simulation

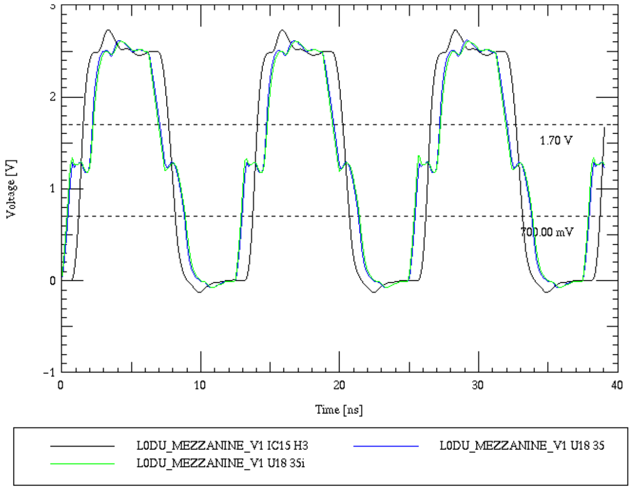


Deserializers => FPGA



SimID	Driver	Receiver	Cycle	FTSMode	Monotonic	NoiseMargin [mV]	OvershootHigh [mV]	OvershootLow [mV]	PropDelay [ns]	SwitchDelay [ns]	SettleDelay [ns]
1	L0DU_MEZZANINE_V1.U18.35	L0DU_MEZZANINE_V1.IC15.H3	3	Typ	PASS	692.215	2727.94	-126.403	0.606466	1.2295	1.9219

- <u>Example of simulation done with Specctra Quest:</u>
  - Output buffer TLK => Input FPGA buffer
  - verification of the signal integrity

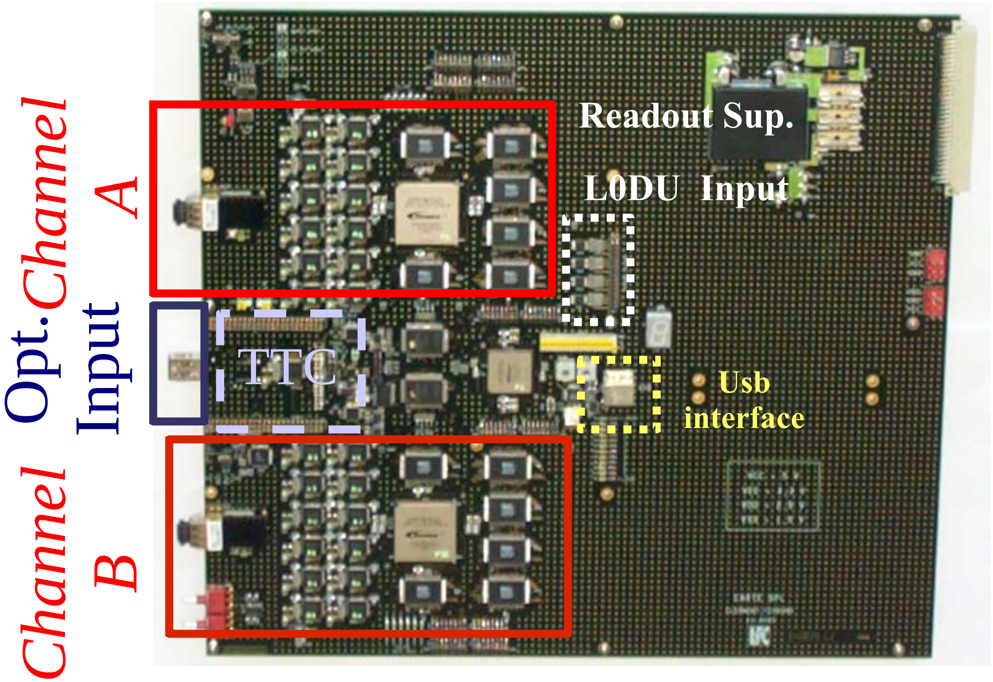


- <u>Other simulations have been made:</u>
  - crosstalk
  - reflexion
  - qualification of line impedance

L0DU Test bench

See GPL poster

- The test of the L0DU and the test bench are more complex than the unit itself
- A Specific pattern injection **(GPL)** has been developed to be able to emulate the L0 sub-triggers and to characterize the links used.



- PCB: 16 layers
- VME 9U
- Dual characteristics as L0DU
- Software interface

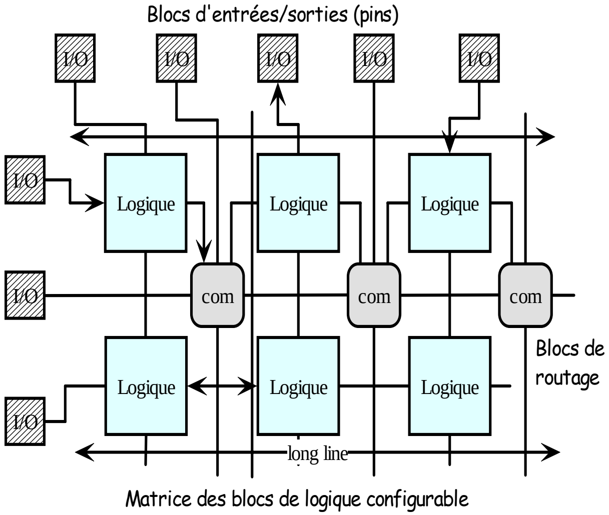
- Allows to:
  - Characterize the links and the optical design
  - Emulate the L0 sub-triggers outputs

PART III:
L0DU Processing

L0DU algorithm requirements

- **L0DU architecture must be flexible** in order to set up the decision algorithm **without FPGA reprogramming**

- Two notions:
  - Configurable:
  => the architecture must allow to select the input of the decision algorithm and the logical operators
  - Parameterizable:
  => the architecture must allow to parameterize the thresholds



- The **principle** is based on **pre-synthesized logic cells** that are selected by switching matrix

- Limitation due to the amount of pre-synthesized logic cells and the size of the FPGA (Stratix EP1S25-F1020)

- Use of a **dedicated software** which represents the L0DU algorithm
  => Configuration and parameterization via the **control interface**

L0DU algorithm structure

- Algorithm are based on multiple conditional choices based on physics criteria
- Each condition is composed by arithmetic and logical operators like adder, comparator and logical AND
- The global decision is obtained by making the logical OR between all the conditional structures
- Arithmetic operators and other useful logic blocks are seen as configurable pre-synthesized cells

Legend

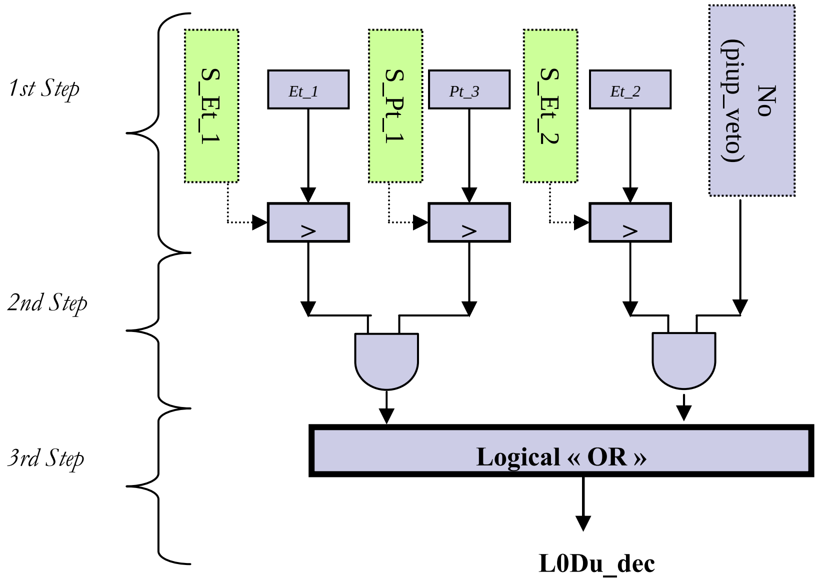
🟪 → Configuration

🟩 → Parameterization

✓ **Algorithm example** :

decision := No
If { Et_1 > S_Et_1 & Pt_3 > S_Pt_3)
then decision : = Yes
If { Et_2 > S_Et_2 & No(Pileup_veto) }
then decision : = Yes

✓ **Electronic interpretation** :



L0DU global architecture

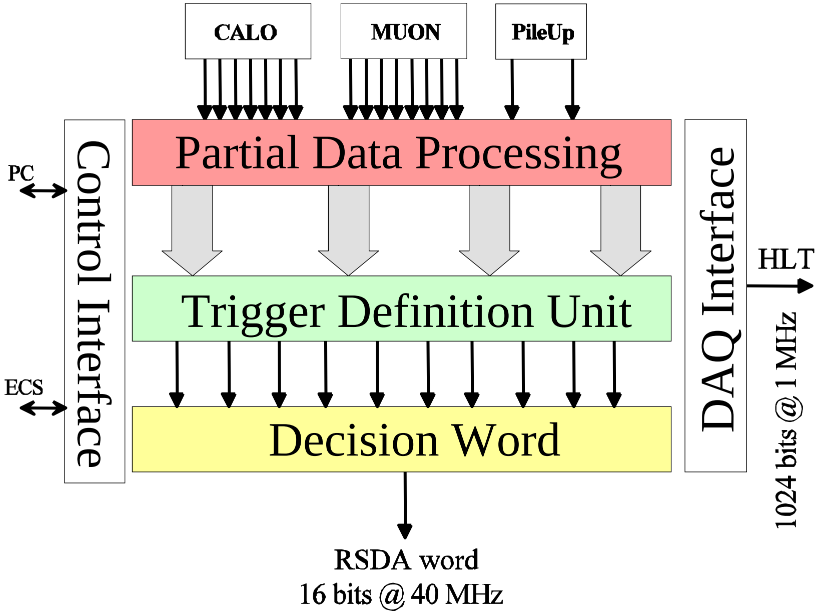
- **<u>Partial Data Processing (PDP):</u>**
  - re-phases the data with the local system clock

  - does the time alignment (latency compensation)

  - **specific pre-processing** for each L0 sub-trigger data

  - prepares the algorithm data

  - produce new data, ex: sum of two inputs



- **<u>Trigger Definition Unit:</u>**
  - processes the information to form a set of trigger conditions which are combined to compute the L0DU decision

Flexible architecture

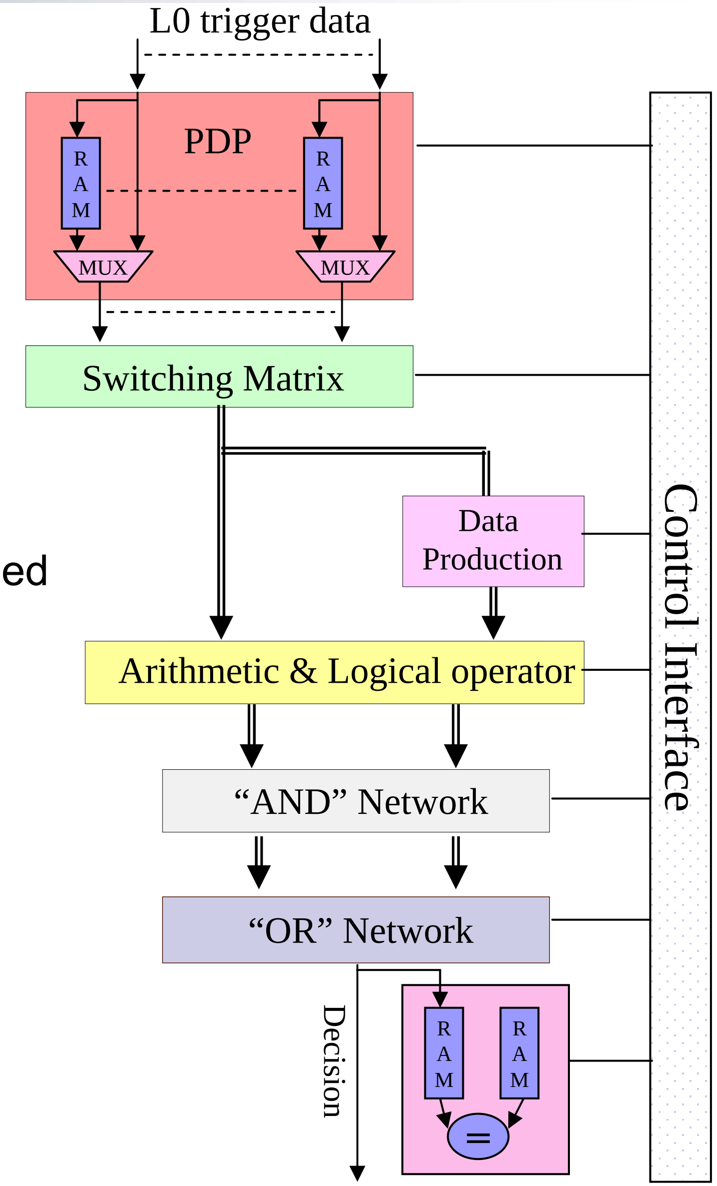
- **Flexible architecture due to:**
  - input selection via a switching matrix

  - configurable thresholds stored on internal registers

  - selectable arithmetic operators (>, <, ≤, ≥, ≠) via registers

  - use of a **P**rogrammable **L**ogic **D**evice (PLD) structure based on "AND" and "OR" network to set up the trigger channels => "easy" to add new trigger channels

- **In addition** to the PDP and TDU:
  - **monitoring functions for on-line monitoring:**
  => counters associated to sub-trigger channel
  => counters associated to L0DU decision
  => error counters
  - an **internal test bench** is implemented to check the behaviour of the L0DU in the pit
  - the memories of the internal test bench can be used to **store the L0 trigger data** (spy mode)



Flexible architecture

Conclusion

- The PCB, the L0DU interfaces and the functionalities have been tested and validated
- Processing of the FPGA have been tested with the GPL board (see GPL poster)
- Board layout complex due to the high frequency and the high density of signals
- Many Specctra Quest simulations must have been done before manufacturing and allow to make a such design without hardware failure
- Status: this prototype will be used during the LHCb detector commissioning phase