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The Level-0 Decision Unit of LHCb experiment

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The Level-0 Decision Unit (L0DU) is the central part of the first trigger level of the LHCb detector. The L0DU receives information from the Calorimeter, Muon and Pile-Up sub-triggers at 40 MHz via 24 high speed optical fiber links running at 1.6 Gb/s. The L0DU performs simple physical algorithm to compute the decision in order to reduce the data flow down to 1 MHz for the next trigger level. The processing is implemented in FPGAs using a 40 MHz synchronous pipelined architecture. The algorithm can be easily configured with the Experiment Control System (ECS) without FPGA reprogramming. The L0DU is a 16 layer custom board.

Summary

The Level-0 Decision Unit (L0DU) is the central part of the first trigger level of the LHCb detector. It is a full custom 16 layers board using FPGAs in BGA package. The L0DU receives information from the Calorimeter, Muon and Pile-Up sub-triggers at 40 MHz which arrive at different fixed times. The Level-0 sub-triggers transmit the data via high speed optical links running at 1,6 Gb/s. A total of 24*16 bits @ 80 MHz is expected as input of the L0DU while up to now 17*16 bits @ 80 MHz are used.
The processing is implemented in FPGAs using a 40 MHz synchronous pipelined architecture. The L0DU latency budget is 500 ns, counted from the last arrival of the sub-triggers data. It performs simple physical algorithm to compute the decision in order to reduce the data flow down to 1 MHz for the next trigger level.
The L0DU decision is sent at 40 MHz in LVDS level to the Readout Supervisor which takes the ultimate decision to accept or not the event. The unit sends a summary block to L1 and HLT trigger for further analysis purpose. The L0DU is plugged on a TELL1 board which is the standard Data Acquisition interface module used by the sub-triggers in LHCb. The L0DU is synchronised by the Timing and Trigger Control (TTC) and is connected to the Experiment Control System (ECS) via a CC-PC. An additional USB interface is implemented for the control of the board without the ECS standard.
The internal design of the processing FPGA is composed by a Partial Data Processing (PDP) and a Trigger Definition Unit (TDU). The aim of the PDP is mainly to adjust the clock phase, perform the time alignment and prepare the data for the TDU. Moreover, the PDP implements specific functions to monitor the links and check the data time alignment.
The TDU is flexible and allows to configure through the ECS different decision algorithm with the same programmed architecture in order to answer to the need of algorithm evolution during the functioning of the detector and to adapt the algorithm parameters to the luminosity of the detector. The flexibility is introduced by the use of an internal switching matrix, AND network and OR network that are configurable via the ECS. The TDU architecture is similar to a PLD device and allows to define various trigger channels that are ORed to obtain the final L0DU decision. All the trigger channels are downscaled in order to tune permanently the 1 MHz at this trigger level despite of the luminosity decrease of the detector during run. All threshold and downscaling factors are parameterized through the ECS without reprogramming the board. The TDU also implements monitoring function in order to check the efficiency of the trigger channel and the global efficiency of the decision algorithm. The L0DU software gives the rate of trigger channel and global decision, and alarms the user if the output trigger rate is different of 1 MHz. An internal test bench is implemented on the L0DU to check the behaviour of the L0DU.

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