

The ALICE silicon pixel detector read-out electronics

Wednesday, 27 September 2006 12:00 (20 minutes)

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system. The SPD contains 10 million pixels organized in 120 detector modules (half staves) connected to the off-detector electronics via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the routers. This paper describes the detector readout, control and off-detector electronics.

Summary

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system which contains 10 million pixels organized in 120 detector modules called half-staves. Each half-stave contains one multi chip readout module and two detector ladders with each 5 pixel chips bump-bonded to one sensor. The ALICE SPD off-detector electronics controls, configures and reads out the detector via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the routers.

Each of the two link-receiver channels has three optical fibre links; two links for the clock and the serial trigger, control and configuration data and one 800 Mbit/s G-link compatible link to receive data from the detector.

The Routers receive the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip and forward the trigger commands to the pixel detector. Upon reception of the L1 trigger signal the pixel data are copied into multi-event buffers on the pixel chips. After reception of a positive L2 decision data are sent from the detector to the link receivers. On the link receiver the pixel data stream is de-serialized and stored in a buffer-FIFO before data are zero suppressed, encoded, re-formatted and written to a dual port memory. Once the link receiver has processed the data the router processor is informed to read the data from the link receiver dual port memory.

Each Router sequentially reads one event from each of the link receiver channels in order to merge data from the 6 channels and label them with trigger and status information to build one router sub event. The sub events of each of the routers are sent to the ALICE-DAQ system through the ALICE detector link (DDL). The read out data stream can also be copied to a dual port memory, where it is accessible for data monitoring and analysis via the VME-interface.

The data access for the SPD control and configuration is performed via the router VME-interface. The router converts the data to JTAG compatible commands which are sent to the detector on the optical links with a maximum data rate of 5 Mbit/s.

The full SPD read out chain was successfully operated with two half staves during a beam test in November 2004 where detector modules of all ITS systems (silicon pixel (SPD), silicon drift (SDD) and silicon strip detectors (SSD)) were installed. The functionality and the interface of the off-detector electronics to the ALICE TTC, the DAQ, a simplified version of the DCS system and the on-detector electronics were verified in a combined run with SSD and SDD during 11 hours where some 5 000

000 events were recorded without errors.

The SPD detector system including the off-detector electronics is currently pre-installed in the CERN DSF where the full detector system is integrated and commissioned before being moved to the underground area.

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Session Classification: Parallel Session B4-Trigger & DAQ session 1