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”CMAD”, a Full Custom ASIC, for the Upgrade of COMPASS RICH-1

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In this paper we present an 8 channel full-custom ASIC prototype, named “CMAD”, designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN.

The task of the chip is amplifying the signals coming from fast multi-anode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

CMAD was developed using a 350nm commercial CMOS technology.

Summary

COMPASS is an experiment at the CERN SPS designed to study the structure and Spectroscopy of hadrons with diverse types of high intensity beams.

One of the key components of the experimental apparatus is a Ring Imaging Cherenkov (RICH) detector, used to perform particle identification.

In order to improve the reconstruction efficiency of the RICH, an upgrade is under development. The experience gained with the first physics runs has, in fact, shown that a trigger rate of 100 kHz and a single channel rate of 5 MHz should be sustained in order to reach optimal performance.

These tight requirements can be achieved by detecting the photons produced in the sensitive volume by photomultiplier tubes equipped with fast read-out electronics. The granularity of the system demands the use of compact multi-anode photomultipliers (MPT).

In this paper we present an 8 channel full-custom ASIC prototype, named “CMAD”, which has been developed for the read-out of the MPTs in COMPASS. Produced in AMS 0.35 um CMOS technology, the chip performs binary read-out of the MPT signals. Each processing channel features in fact a low-noise transimpedance amplifier followed by a fast shaper with baseline restorer and a comparator.

The gain of the preamplifier can be adjusted from 0.6 mV/fC to 1.5 mV/fC in eight steps. This allows to compensate at least partially for the channel-to-channel gain variation of the MPTs. Additionally, the threshold of each comparator can be adjusted on a channel by channel basis via a local 8-bit D/A. The gain of the front-end and the D/A values are programmed using a digital control unit and the IC2 standard.

The peaking time at the output of the shaper is 10ns. The system has been designed to cope with a rate in excess of 5MHz/Channel.

The output pulses are stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels.

The chips have been extensively simulated and prototypes were fabricated. The chips are currently being tested and results of the measurements will be reported in the final paper.

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