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ATLAS Pixel Detector Timing Optimisation with the Back of Crate Card of the Optical Pixel Read out System

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The ATLAS detector is one of the LHC experiments going to start data taking in 2007. The innermost subdetector of ATLAS will be a pixel detector. It consists of 1744 pixel modules which are controlled and read out via optical signals. The off detector end of the optical link is the Back of Crate card which is performing the optical-electrical conversion and adopting the timing for the detector and the readout hardware.
Studies to test the timing capabilities have been done during a combined test beam which will be presented. Additionally information about the production of this card and the optical link are given.

Summary

The Back of Crate card will be used in two subdetectors of ATLAS, namely SCT and the Pixel detector.
It is a 9U VME card paired to one Read out Driver each. In the pixel detector 132 Back of Crate cards will be used. The card is the electrical-optical interface between the Read out Drivers and the detector modules on one hand and between the Read out Drivers and the Read out Buffers on the other hand.
It has to control data transmitting, laser control, data receiving and recovery, and the timing of the on and off detector electronics.
The electrical-optical conversion itself is performed on plugin boards, the TX-plugins and RX-plugins, housing laser arrays or pin arrays.
The timing capabilities of the Back of Crate card are important to drive the pixel detector efficiently. The Back of Crate card is responsible for the timing of the on detector and off detector electronics. It receives the 40MHz system clock from a Timing-Trigger-Control Interface Module and copies it to the Read out Driver and to the modules.
The clock for the detector modules is encoded on the Back of Crate card with the control data for a module into one bi-phase mark signal. This signal is decoded at the on detector system and passed to the module. It enables the system to use only one optical
fibre per module to transmit the control signals and the clock. The data transmission from the modules to the Back of Crate card is done over one or two fibres per module depending on the transmission bandwidth.

The timing of the individual modules is quite important. If a read out trigger (LV1) is sent to the module, all hits registered in the clock cycle matching the trigger timestamp are read out. The hits being registered in the front end electronics have a timewalk depending on the deposited charge in the sensor. Therefore hits coming from a small charge deposition are registered significantly later than hits with higher charge depositions. If the timing is not optimised, hits will be associated to a wrong bunch crossing.
Because of cable length differences and different locations of the modules in the detector the clock timing and trigger arrival has to be adopted for each module individually, by modulewise delaying the encoded clock and data signal being transmitted to the module.

During the ATLAS combined testbeam a study of this timing functionality has been performed. It shows that it is possible to optimise the timing for the modules and therefore increase the read out efficiency.
The read out window width of 25ns is confirmed and all hits being registered in the

correct 25ns wide clock cycle window are read out. Additionally an estimation about the smallest amount of charge, which is necessary to associate the hit to the correct bunch crossing, can be determined.

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