A Test Stand System for High-Energy Physics Applications

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Abstract

The Front-End R&D group at Fermilab has been developing pixel hybridized modules and silicon strip detectors for the past decade for high-energy physics experiments. To accomplish this goal, one of the activities the group has been working on includes the development of a flexible high-speed and high-bandwidth data acquisition and test system to characterize front-end electronics. In this paper, we present a general purpose PCI-based test stand system developed to meet the stringent requirements of testing silicon strip and pixel detectors. The test stand is based on a platform that is flexible enough to be adapted to different types of front-end electronics. This system has been used to test the performance of the electronics for different experiments such as BTeV, CDF, CMS, and Phenix. The paper presents the capabilities of the system and how it can be adapted to meet the testing requirements of different applications.

I. PCI Test Adapter

A peripheral component interconnects (PCI) based test stand was developed to meet the high-speed readout requirements of the electrical characterization of the silicon strip and pixel modules used in HEP experiments. This test stand is developed around a PCI test adapter (PTA). The PTA has a Xilinx Virtex4 field programmable gate array (FPGA) that gives it the flexibility necessary to meet, for example, the changing demands of the pixel module characterization (e.g., as new ICs are designed) and different applications. Figure 1 shows a functional block diagram of the PTA.

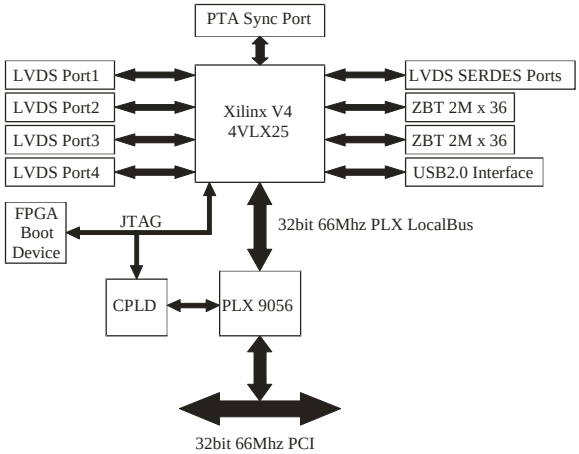

Figure 1: Functional diagram of the PTA

The data bus from the pixel modules is connected to low-voltage differential signaling (LVDS) ports, and the data is packed by the FPGA and stored in the local ZBT memory banks until further readout by the PCI bus. A 66MHz PCI-mastering device (PLX Technology PCI9056) maps the local ZBT memory banks to the computer's memory using direct memory access (DMA). The PTA has other features such as a USB2.0 interface (useful for applications using a laptop computer) and a pair of high-speed serializers - deserializers (SERDES) used to expand the data traffic capabilities of the board. Figure 2 shows a picture of the PTA board.

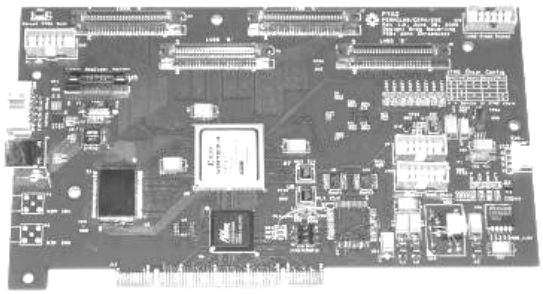

Figure 2: Photograph of the PTA

The PTA is distributed with drivers and middleware that works in both Windows and Linux environments. Data acquisition and data analysis software have been developed for both operational systems as well. A screenshot of the data analysis software is shown in Figure 3.

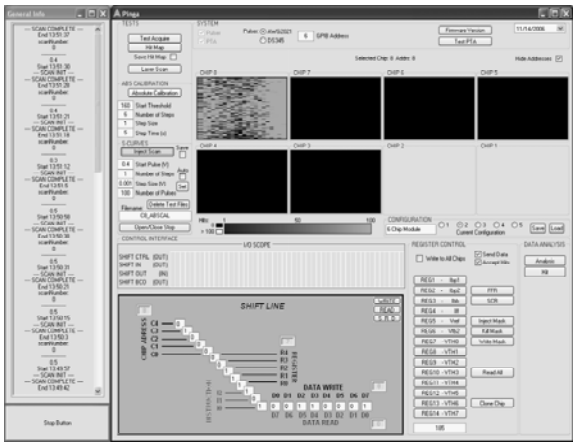

Figure 3: Screenshot of the DAQ software

Over 200 PTAs have been produced, distributed, and used in test stands around the world. One of these applications is testing pixel modules using the third version of the Fermilab pixel chip (FPIX2). Figure 4 shows a photograph of this test stand at Fermilab.

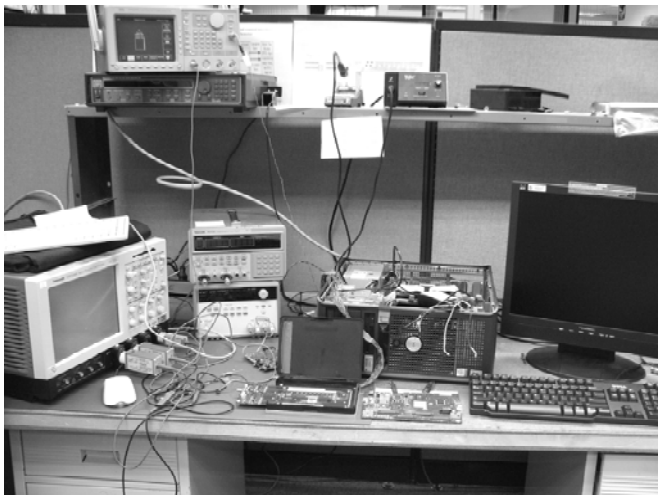

Figure 4: Photograph of the test stand with a PTA and pixel module

A. PTA Specifications

PCI: The PTA uses the PCI9056 Bus Mastering PCI interface from PLX. The PLX9056 is a 32bit/66Mhz PCI Master that has a 32bit/66Mhz local bus.

FPGA: The PTA uses the Xilinx 4VLX25 Vertex4 FPGA. The Vertex4 series FPGA's have built in LVDS termination resistors that save PCB space and make it much easier to change designs.

LVDS Ports: The PTA has 4 I/O connectors. In the default PTA configuration the 4 ports will be configured for LVDS. The LVDS termination resistors can be turn on and off inside of the Xilinx FPGA. No resistors will have to be placed and/or removed when the PTA is used for different test stands. Each connector has 18 pairs of signals, and 6 pairs of grounds. The signal pairs can be used as 18 differential pairs or 36 singled ended signals.

Memory: The PTA has two banks of 8M ZBT memory that runs up to 266MHz. The Xilinx FPGA has 1.3Mbits of memory.

USB: The PTA uses the Cypress FX2 USB2.0 interface chips. The PTA has a connector for an external power supply so it can be powered out of a PC. The PC is then able to use the PTA through the USB port. The Cypress FX2 chips have transfer rates above 20MB/s.

Miscellaneous: The PLX9056 is able to boot the Xilinx FPGA via the JTAG port. The Virtex4 FPGA has LVDS SERDES ports. Each port has TX data and clock pairs and RX data and clock pairs. Depending on the speed grade of the FPGA, the SERDES can run up to 1Gbit/Sec.

II. Front-End Module Interface Card

The Front-End Module Interface Card (FEM) is a test module designed to support test stands instrumented with the PTA [1]. The FEM is used in tandem with the PTA to supply digital and analog signals to the devices under test. In summary, the FEM has the potential to replace four of equipments commonly used to test front-end electronics in HEP: pulser, low voltage supply, high voltage supply, and temperature sensor signal conditioner. Figure 5 shows the functional diagram of the FEM.

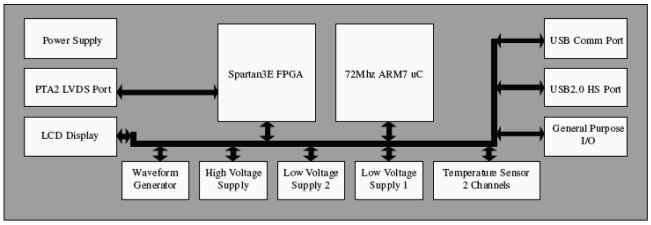

Figure 5: Functional diagram of the FEM

A. FEM Specifications

Microcontroller: The FEM uses an ARM7 LPC2348 microcontroller from NXP Semiconductor. The LPC2348 is the heart of the FEM as it controls all of the various test module functions and communicates with a PC via a USB2.0 high speed interface.

FPGA: The Spartan3E FPGA is used for various FEM glue logic, thus allowing a flexible interface between the FEM and the various front-end devices under test.

USB2.0: The USB2.0 High Speed Port is used by the FEM to communicate with a PC running the test stand software. The port is a high speed port that can do USB bulk transfers at 480Mbps.

USB COMM: The USB COMM port is used by the microprocessor for debugging purposes. It can be used to connect the FEM to a terminal for debuggin messages or it can be used to update the LPC2348's boot loader firmware. This port will not be used in normal operation.

RTD Temperature Sensor Interface: The FEM can monitor two different RTD temperature sensors. The sensors are placed near or on front-end electronics under test.

Low Voltage Supplies: The low voltage supplies are used to power the devices under test. Normally one channel of the supply is used for the analog part and the other for the digital part of the device under test. The output voltage is programmable via the USB port and can be adjusted from 1.2V to 4.0V. Each supply can source 1A of load current. Both the voltage and current are monitored by the microprocessor and passed on to the test PC via the USB port.

High Voltage Supply: The FEM's voltage is used to bias the sensor on the front-end module. The output voltage has a range of 0VDC to -500VDC and can supply 2mA of current. The voltage and the current of this power supply can be monitored via the USB port.

Waveform Generator: The waveform generator is used to generate a pulse that is used to inject charge in the preamplifier of the front-end chips. The waveform generator uses a DAC connected to the FPGA to generate the pulse. All of the pulse attributes can be programmed via the USB interface.

LVDS Port: The LVDS port is a standard connector to interface to the PTA.

General I/O Port: The I/O port is used for general purpose signals that can be configured as inputs or outputs as needed. The outputs can source/sink 24mA @ 3.3V/5V and the inputs can handle 5V signals.

LCD Display: The LCD display is used to show current FEM operating conditions. It can be programmed to show the monitored voltages and currents, RTD temperatures, and various other things.

Mechanical Specifications: The FEM is housed in a 6.3"H X 6.3"L X 2.1"H extruded aluminum enclosure.

Input Power Supply: The FEM uses an external desktop switching power supply as its main supply. The supply is rated at +12V, 7A.

III. Case Studies

A. Test of Pixel Multichip Modules

One of the recent applications of the PTA is the test and characterization of the pixel multichip modules for the Phenix LDRD project at Brookhaven National Laboratory [2]. The pixel sensor is bump-bonded to the Fermilab Pixel chip version 2.1 (FPIX2.1). The readout chip is wire bonded to a high-density interconnect (HDI). Figure 6 shows a picture of the pixel sensor bump-bonded to 8 FPIX2.1 chips. The pixel module is assembled onto a thin-film HDI. The HDI is then wire bonded to a test card, and the test card has matching connectors to the PTA.

Figure 6: Pixel multichip module

The 8-chip pixel module has a total of 22528 pixels that read out data at a maximum rate of 700 Mbps. The serial lines out of the FPIX2.1 chips can be configured so that data is read out in 1, 2, 4, or 6 parallel lines per chip. The PTA supports all these different readout modes. The readout chip doesn't require any trigger; hence there is a continuous flow of data through the serial lines. When the chip has no data to transmit, the synchronization word is sent out to the PTA continuously. This provides steady power consumption with no current bursts and no need for DC balancing the transmission lines. Figure 7 shows the data structure out of the FPIX2.1 chip into the PTA when 1 serial line is used.

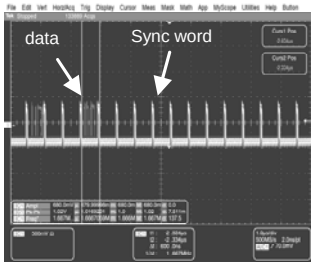

Figure 7: Data output from FPIX2.1 into PTA

The test stand software also does the full characterization of the pixel modules. Figures 8 show the results of calibrating the digital registers of the FPIX2.1 chip and the pixel sensor using X-ray sources with different energies.

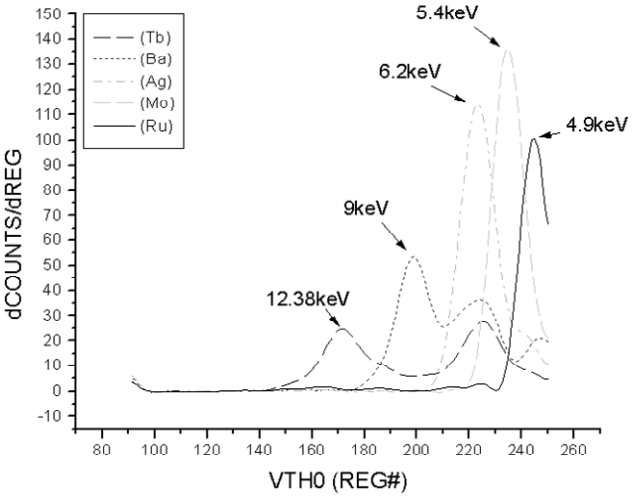

Figure 8: Test results of a pixel sensor using radioactive sources

The test stand also allows the visualition of the hit map using a beta gun (Sr^{90}). The hit map is very useful for the determination of the quality of the bump-bonds. Figure 9 shows the hit map of the pixel sensor when the radiactive source is shined at the edge of the module. The gap between the chips is shown.

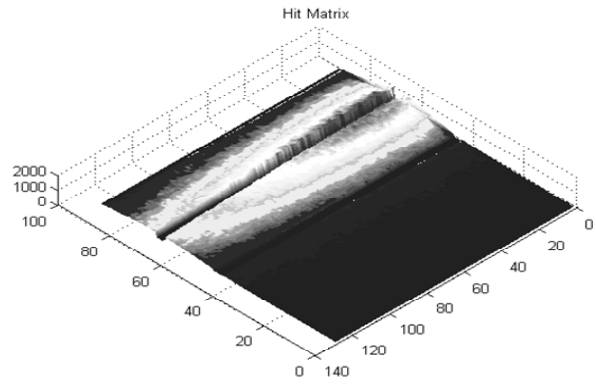

Figure 9: Hit map detail between two FPIX2.1 chips

Figure 10 shows the hit map of the region where the high voltage bias was connected to the sensor using silver epoxy. In this figure it is possible to observe the footprint left by the high voltage connection. When an aluminum wire bond is used no foot print can be seen on the hit map

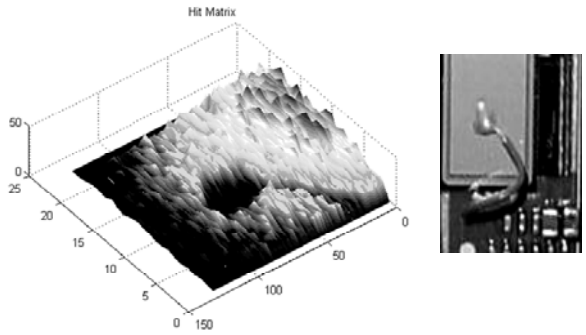

Figure 10: Hit map footprint of bias connection

B. *Test Beam DAQ*

The scalability capabilities of PTA allowed us to use the test stand described in the previous section as the building block to develop a complete DAQ for the test beam of pixel modules. The functional diagram of this DAQ is shown in Figure 11.

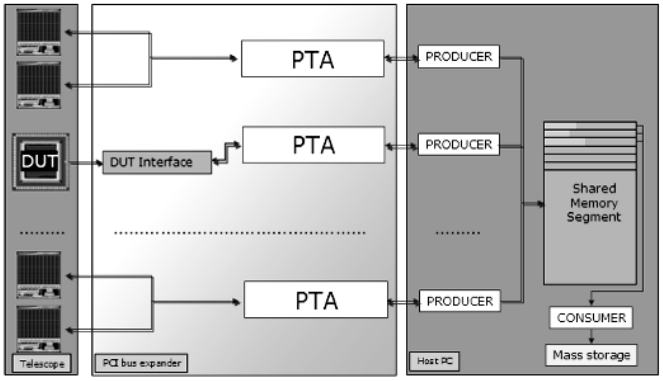

Figure 11: Functional diagram of the test beam DAQ

Each set of two pixel boards located at the telescope is connected to a single PTA sitting on the PCI bus of the DAQ computer. This application is employing a 13-slot PCI bus extender that allows the connection of 13 PTA cards. The arrangement of the test beam pixel telescope and the device under test is shown in Figure 12.

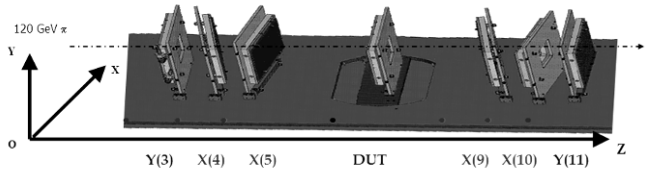

Figure 12: Telescope of 6 pixel detectors and device under test (DUT)

The telescope has a total of 6 pixel planes, 2 Y-measurement planes and 4 X-measurement planes. The pixel cells are 50 μm × 400 μm, and each chip has 2,880 cells. The device under test (DUT) is placed in the center of the telescope. The track projection error achieved by this telescope is ~3 μm on X-direction and ~8 μm on Y-direction.

1) *DAQ Architecture*

The FPIX2.1 chips does not require a trigger to send data out, hence the PTA-based DAQ must be fully data driven DAQ. Hits from the detectors are sent to readout as soon as they are above threshold (the process is driven by a clock synchronized with the accelerator clock). Each hit is tagged by PTA cards with a hardware generated time-stamp. An event, defined as "*a collection of equal time-stamp hits from multiple detectors*", is built by the consumer process using an efficient sorting algorithm.

Data is produced by the FPIX2.1 at a variable rate while the host computer receives them at its own rate (depending upon CPU clock and processor current activity). The PTA has been programmed to get data from the FPIX2.1 chips and to act as an intermediate rate-balancing buffer. This is accomplished by a periodic switching of the data flow between two RAM banks.

The architecture has been designed to allow for a continuous, lossless sustained data-rate. In a test-beam setup several detectors are read-out simultaneously and data made available to the even-builder. The DAQ framework (C++) allows adding and replacing different event-building algorithms by defining an abstract interface to the appropriate implementation. This allows for different detectors, with different event-building strategies, to be read-out by the same DAQ system.

IV. Conclusions

A multi-purpose DAQ system has been developed to test and characterize front-end electronics for HEP applications. The system is flexible enough to accommodate different types of detectors as well as different event-building strategies. The system has been used extensively in test beams as well as in various laboratories to characterize detector performances.

The PTA and the FEM have proven to be a useful, low cost and efficient approach to readout detectors in demanding environments like bench test and beam test. The design and implementation of a low/mid-size DAQ system in C++ has been successfully achieved, and the code is available to future collaborators upon request.

V. References

[1] Rivera, R., et al., "FEM Specifications," CD/ESE Internal Document, October 2006.

[2] Turqueti, M., et al., "Pixel Multichip Module Development at Fermilab for the PHENIX Experiement," IEEE Nuclear Science Symposium, San Diego, November 2006.