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A Test Stand System for High-Energy Physics Applications

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The Front-End R&D group at Fermilab has been developing pixel hybridized modules and silicon strip detectors for the past decade for high-energy physics experiments. To accomplish this goal, one of the activities the group has been working on includes the development of a high-speed and high-bandwidth data acquisition and test system to characterize front-end electronics. In this paper, we present a general purpose PCI-based test stand system developed by the Front-End group at Fermilab to meet the stringent requirements of testing silicon strip and pixel detectors. The test stand is based on a platform that is flexible enough to be adapted to different types of front-end electronics. This system has been used to test the electrical performance of the electronics for different experiments such as BTeV, CDF, CMS, and Phenix. The paper presents the capabilities of the system and how it can be adapted to meet the testing requirements of different applications.

Summary

The Front-End R&D group at Fermilab has been developing front-end electronics to meet the stringent requirements of high-energy physics (HEP) experiments. A peripheral component interconnect (PCI) based test stand was developed at Fermilab to meet the high-speed readout requirements of the electrical characterization of the silicon strip and pixel modules used in HEP experiments. This test stand is developed around a PCI test adapter (PTA). The PTA has a Xilinx Virtex4 field programmable gate array (FPGA) that gives it the flexibility necessary to meet, for example, the changing demands of the pixel module characterization (e.g., as new ICs are designed) and different applications. The data bus from the pixel modules is connected to the low-voltage differential signaling (LVDS) ports, and the data is packed by the FPGA and stored in the local ZBT memory banks until further readout by the PCI bus. A 66MHz PCI-mastering device (PLX Technology PCI9056) maps the local ZBT memory banks to the computer's memory using direct memory access (DMA). The PTA has other features such as a USB2.0 interface (useful for applications using a laptop computer) and a pair of high-speed serializers - deserializers (SERDES) used to expand the data traffic capabilities of the board. The PTA is distributed with drivers and middleware that works in both Windows and Linux environments. Data acquisition and data analysis software have been developed for both operational systems as well. Over 100 PTAs have been produced, distributed, and being used in test stands around the world. One of these applications is testing pixel modules using the third version of the Fermilab pixel chip (FPIX2).

PTA Specifications

PCI: The PTA uses the PCI9056 Bus Mastering PCI interface from PLX. The PLX9056 is a 32bit/66Mhz PCI Master that has a 32bit/66Mhz local bus.

FPGA: The PTA uses the Xilinx 4VLX25 Vertex4 FPGA. The Vertex4 series FPGA's have built in LVDS termination resistors that save PCB space and make it much easier to change designs.

LVDS Ports: The PTA has 4 I/O connectors. In the default PTA configuration the 4 ports will be configured for differential LVDS. The LVDS termination resistors can be turn on and off inside of the Xilinx FPGA: No resistors will have to be placed/removed when the PTA is used for a different test stand.

Each connector has 18 pairs of signals, and grounds. The signal pairs can be used as 18 differential pairs or 36 singled ended signals.

Memory: The PTA has two banks of 8M ZBT memory that runs up to 266MHz. The Xilinx

FPGA has 1.3Mbits of memory.
USB: The PTA uses the Cypress FX2 USB2.0 interface chips. The PTA has a connector for an external power supply so it can be power out of a PC. The PC will then be able to use the PTA through the USB port. The Cypress FX2 chips have transfer rates above 20MB/s.
Miscellaneous: The PLX9056 is be able to boot the Xilinx FPGA via the JTAG port. The Virtex4 FPGA has LVDS SERDES ports. Each port has TX data and clock pairs and RX data and clock pairs. Depending on the speed grade of the FPGA, the SERDES can run up to 1Gbit/Sec.

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