# Proposal for a First Level Trigger using pixel detector for CMS at Super-LHC

F. Palla[a]

[a] INFN Sezione di Pisa, Pisa, Italy
Fabrizio.Palla@cern.ch

*Abstract*

A proposal for a pixel based Level-1 trigger for the Super-LHC is presented. The trigger is based on fast track reconstruction using the full pixel granularity exploiting a readout which connects different layers in specific trigger towers. The trigger will implement the current CMS High Level Trigger functionality in a novel concept of intelligent detector. A possible layout is discussed and implications on data links are evaluated. Finally the performances are shown.

## I. Introduction

The CMS collaboration [1] at the LHC is currently in the final stages of construction and commissioning of the CMS detector and an intensive effort is being devoted to finalize the online and offline software required for data taking and analysis. LHC will start its operations in Summer 2007 and will increase its luminosity to the design limit of $10^{34}$ cm$^{-2}$ sec$^{-1}$. However, to further continue the investigation of exotic rare phenomena and to assess the properties of new particles possibly found at LHC, upgrades are being foreseen that would increase the luminosity up to a maximum of $10^{35}$ cm$^{-2}$ sec$^{-1}$[2], with a collision frequency of 80 MHz, and have the same centre of mass energy. This second phase of LHC operations is called Super-LHC (SLHC). The increased luminosity will require a general redesign of the existing experiments in order to cope with the increased number of particle fluxes into the detector elements.

## II. Trigger at SLHC with the Tracker Detector

In the CMS design, the First Level Trigger (FLT) will filter the 40 MHz input rate of proton-proton crossings down to a maximum of 100 kHz of accepted events. The trigger is based on a set of specialized processors working on small subsets of the calorimeter and muon chamber information. The next selection step, the High Level Trigger (HLT), will receive, on average, one event every 10$\mu$s. In this time the rate must be reduced to 100 Hz, which is the estimated bandwidth that can be put on tape.

At SLHC luminosity there will be about 100 proton-proton collisions occurring every 12.5 ns, in contrast to only 22 collisions for normal LHC operations. This would correspond to about 10 billions of collision events per second, to be compared to the rare physics phenomena which will occur at about few Hertz or lower. Each proton bunch crossing will generate much more than the present 1MB of data, and the expected data transfer to disk will not exceed the rate of about 100 Hz. Hence, the increased luminosity will also require a drastic revision of the existing trigger strategies.
As an example, Fig. 1 shows the rate of the single muon trigger as a function of the muon $p_T$ threshold [3]. The performance at FLT suffers from poor transverse momentum resolution at high $p_T$. The use of the Tracker information at HLT (labelled as Level 3 in Fig. 1) allows a drastic change in the slope of the rate.

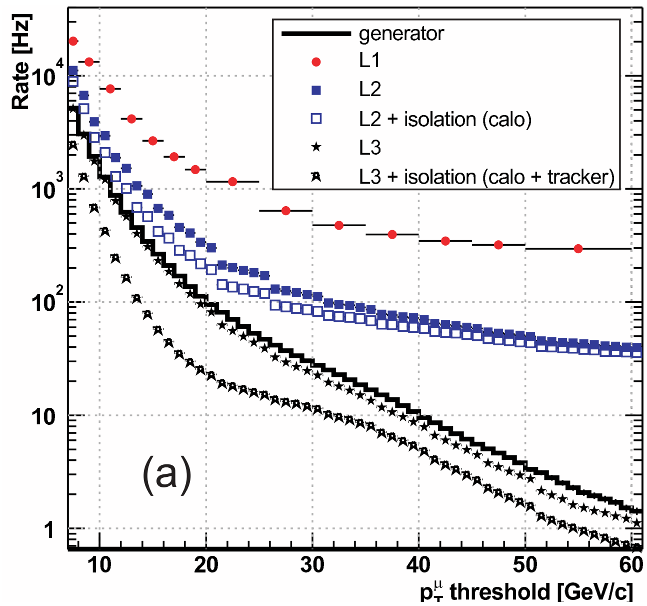


Figure 1: The FLT and HLT single-muon trigger rates as a function of the $p_T$ threshold. The rates are shown separately for Level-1 and HLT (Level-2, and Level-3), with and without isolation applied at Levels 2 and 3. The rate generated in the simulation is also shown.

Due to the shape of the underlying background distributions, the required FLT rate reduction for SLHC cannot be achieved by increasing the redesigned FLT thresholds, even if one is willing to pay the price of cutting useful physics. Gain in background reduction can only come from improving the FLT algorithms for selection of physics signals. Furthermore at the SLHC the FLT efficiency and purity to select Higgs and other exotic signals will degrade due to the increase of the minimum bias events by at least a factor of 5. Given that the current FLT design already uses information from all detectors but the silicon tracker, any improvements in background reduction efficiency and purity can only come by including tracking information at the FLT. Hence, the need for a First Level Tracking Trigger.
Using tracking information at the FLT algorithms will more than compensate for the factor of 5 increase of the backgrounds. The largest benefit is obtained by using the tracks/hits and vertices found by the vertex detector, which in turn creates severe challenges for any tracking trigger due to the stringent constraints in terms of power, radiation hardness and data volume and speed.

## III. TRACKER TRIGGER STRATEGY

The basic idea which drives the FLT based on Tracking is to port as much as possible what HLT Tracking has shown feasible now [3], and design new algorithms reflecting tracking trigger capabilities.

The proposed trigger strategy will influence the layout of the tracker detector and *viceversa*. The requirements on the hardware are, however, minimal. The proposed strategy makes use of binary readout of the front end electronics, followed by transfer of the full granularity data using fast and radiation hard fibers to the barracks where dedicated processors will reconstruct tracks.

The tracking trigger aims to provide tracks above a given momentum threshold that could be matched with FLT muons or electrons in the Global Trigger.The most important feature of the trigger, relies upon the usage of established detector and electronics technologies to get a robust project stretched beyond the current limits thanks to the miniaturization of the electronics. That implies using the current hybrid pixel technologies [4] for the sensors, expand existing Tracking Triggers (SVT) [5] based on the use of Associative Memories chips[6] and finally making use of more radiation hard optical fibers technologies.

In particular, as far as the logic running the tracking algorithms in the barracks is concerned, the proposed system is an evolution of the Silicon Vertex Tracker (SVT) built for the CDF experiment, at the Tevatron Collider, where real time tracks are reconstructed. The implementation that is envisaged here, is mainly used for best momentum reconstruction.

### A. Design considerations

The main usage of a Tracking Trigger is for reconstruction of particles exceeding a given transverse momentum ($p_T$) threshold. What is therefore needed are detectors with low occupancy (based on pixelized detectors) providing sufficiently distant measurements, rather than brilliant space-point resolutions. Equipping large areas with small pitch detectors is cost demanding, hence a compromise between the two requirements should be found. The charged track multiplicity at SLHC is foreseen to be about 600 tracks per rapidity bin, hence a good pattern recognition is required. If the Tracker material budget will not decrease by a sizeable amount, then multiple scattering will drive the momentum resolution below about 10 GeV/c hence a point resolution of no better than a few tens of microns is needed in the $r - \phi$ coordinate to determine the momentum with about 10% precision for order of half a meter lever arm.
To limit the amount of data to be transferred to the Trigger logic, a binary readout for each channel is proposed. To profit of the best pattern recognition we assume that full granularity pixel data is available for processing. This assumption is the real challenge of the proposed trigger strategy and dictates the more serious requirements on the hardware as well as on fast links to transport the data to the FPGAs in the barrack. In addition, the same data links as of the data readouts could be used for trigger signals, avoiding duplication of fibers. In order to cope with the large data volume to be processed, the proposed approach makes use of the information coming from the radial region from 25 to 50 cm, that shows radiation levels where current hybrid pixel technologies and optical fibers could work without challenging technological efforts. The large radius would in addition provide the large lever arm required for momentum measurement, with the addition of the precise beam spot information in the r-$\phi$ plane.

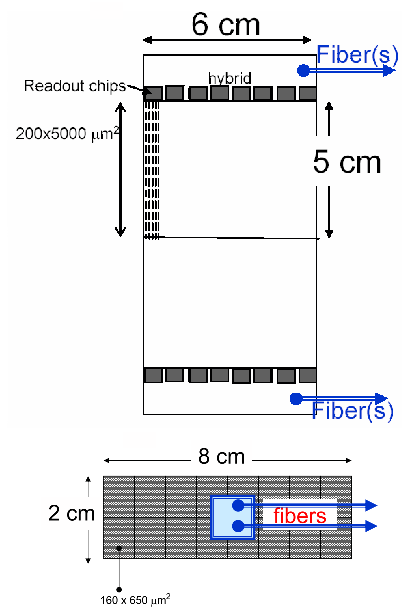

Figure 2: Module for the outer (up) and inner (low) radius layers.

### B. Tracker Layout

In the current proposal, for sake of simplicity, only a barrel region is considered, covering the pseudorapidity region of $|\eta| < 1.5$. The considered Tracker Trigger region is composed by four layers at radii of 26, 34, 42, 50 cm from the beam line, at exactely the same locations as the present CMS Silicon Strip Inner Barrel (TIB)[8]. All problems linked to the mechanics, cooling or silicon sensor technologies, go beyond the scope of this contribution. It is sufficient to state that in this region, both the radiation hardness as well as services will not be as dramatic as in the layers below 15 cm radius, and is widespread belief that would not be insormountable technological problems.

Following a proposal from R. Horisberger[4] the innermost layer of the four, is equipped with hybrid pixel modules of dimensions of about 2 (r-$\phi$) $\times$ 8 (z) cm$^2$ and composed of 16 readout chips (2 in r-$\phi$ and 8 in z),as they are in the current CMS design. The cell dimensions, however, will be 200 (r-$\phi$) $\times$650 (z) $\mu$m, in order to allow for reduced costs in the bump-bonding. At a radius of 25 cm there will be about 14 modules in each ladder in z and 80 modules in azimuth. The other three layers will be equipped with large elongated pixels of 200 (r-$\phi$) $\mu$m $\times$ 5 (z) mm and a sensor area of 6 (r-$\phi$) $\times$ 12 (z) cm$^2$. A possible layout of the modules is sketched in Fig. 2. Each module is equipped with radiation hard fibers and laser drivers having the largest speed as possible. For fiber lengths of about 100 meters (the distance from the modules to the barracks) the VCSEL technology is already able to provide radiation hard fibers with about 2 Gbps[9], with a power consumption of about 1W. It is not impossible that R&D will deliver a speed of 4 to 5 Mbps radiation hard fiber technology in a few years time, in time for

SLHC.[7] As previously stated, the real problem in the proposal is to make such a large amount of data available to single tracking processors in time. The input bandwidth sets and upper limit either on the event rate or on the size of the detector connected to it. We envisage to send data to the trigger exploiting a parallel readout of the detector layers on four buses. Nevertheless, in order to sustain very high event rates, it is necessary to organize the tracking processor as a set of independent engines, each working on a different sector of the silicon tracker. The detector will be divided into azimuthal sectors. Each sensor of every layer in the sector will send the information to the specific engine working on it, located in the barrack, which will combine the information from at least 3 layers out of 4 to determine the track momentum with a resolution better of about few ($<$10)% at 10 GeV/c.

The sector granularity has been chosen taking into account the minimum measurable $p_T$ for triggering purposes, without efficiency loss. The innermost layer is divided into about 80 azimuthal sectors, matching the width of a module. This width well covers the bending of a track of 5 GeV/c $p_T$ and above.

Table 1: Layout of the pixel layers, giving the radius from the beam line, the number of modules is z and r-$\phi$.

| Radius (cm) | No. Modules in z | No. Modules (sectors) in r-$\phi$ |
|---|---|---|
| 26 | 14 | 81 |
| 34 | 9 | 36 |
| 42 | 9 | 44 |
| 50 | 9 | 52 |

The number of sectors in the three outermost layers will also follow the sensors widths. Table 1 shows the number of modules per sector in each layer. 20 bits will be sufficient to locate any hit in each layer of the sector. In the barrack, the hit information from suitable overlap regions of neighboring sectors could be sent to more than one engine to decrease efficiency losses in the boundaries between sectors.

### C. *Simulation results*

The results are based on about 3000 minimum bias (MB) events and 250 top events generated with Pythia 6.227 with default settings. Chunks of 100 MB events have been passed through a complete GEANT4 simulation of the Tracker detector and digitized and the resulting occupancies are studied. Table 2 shows the expected mean and rms number of hits per sensor per bunch crossing (12.5 ns) in the different layers. It is important to notice that the largest contribution to the occupancy comes from the primary tracks. In case of $t-\bar{t}$ events at SLHC, the largest increase in the occupancy is smaller than the rsm of the hit rate coming from MB events. The largest hit rate per module occurs at the second layer with an average of 8.5 hits/sensor. The large fluctuations occurring in the module occupancy could be accomodated by using pipelines in the readout electronics.

Table 3 shows instead the data rate traffic on the fibers (using 20 bits/hit encoding) together with the estimated number of fibers per layer, with the assumption of a fiber link speed of 5 Gbps. It is noticeable that the required amount of fibers is comparable (and even smaller) of the current CMS Inner Tracking Barrel (2000 in the innermost layer and 2600 in the second layer), giving confidence that such a system will not become more complex even in the case of lower speed links. The power density contribution from the laser drivers is estimated to be of the order of 60 mW/cm$^2$ in the innermost layer, that has the largest density, to be compared with about 200 mW/cm$^2$ for the current CMS pixel electronics.

Table 2: Mean and rms number of hits in each module and layer per bunch crossing (12.5 ns) in Minimum Bias events.

| Radius (cm) | No. hits/module/bx (RMS) | No. hits/sector/bx |
|---|---|---|
| 26 | 3.1 (1.4) | 43 |
| 34 | 8.5 (4.5) | 78 |
| 42 | 5.3 (3.5) | 49 |
| 50 | 3.7 (2.0) | 34 |

Table 3: Mean data rate per each sector every bunch crossing (12.5 ns) in Minimum Bias events, together with the number of fi bers needed to bring the signal out (5 Gbps speed).

| Radius (cm) | Data rate per sector/bx (Gbps) | No. data links/layer |
|---|---|---|
| 26 | 69 | 1100 |
| 34 | 125 | 900 |
| 42 | 78 | 700 |
| 50 | 55 | 600 |

## IV. Dimensioning the Tracker Trigger Hardware

Each engine working on a particular $\phi$ sector, located in the barracks, will receive the hits from each layer and will produce track candidates. We propose to implement the engine with an associative memory chip (AM chip) where a set of all possible tracks exceeding a given $p_T$ cut and originating from a certain luminiosity region compatible with the beam spot, has been previously loaded. Tracks are pre-calculated taking into account multiple scattering. These are referred as banks of patterns. Each stored hit pattern is provided with the necessary logic to compare itself with the event. The AM pattern bank is limited by the size of the hardware, mainly consisting of low-density content-addressable custom memories. The size of the bank pattern depends on the number of detectors in each Trigger sector and on their granularity. The estimated number of patterns to be stored for the current proposal is about 25,000 for a lower momentum cut of 5 GeV/c. This is compatible with the capacity of a next generation single chip.

The AM chip used in SVT has about 5000 patterns for 6 tracking planes in UMC 0.18 $\mu$m CMOS 1P6M logic by IMEC [6]. Once developed in 90 nm technology, each AM chip could accommodate about four more patterns. The same memory can be reorganized to fit 30,000 patterns for 4 triggering planes.

The current AM chip runs at 50 MHz with 6 parallel buses of 18 bits encoding each. The future evolutions of the AM chip will run at 100 and 200 MHz, so each one is expected to support a rate of 3.6 Gbps while the largest flux from the second layer is about 40 times larger. In order to be able to run in such conditions, we envisage that the flux coming from the detector is sent to a switch that distributes the hits coming from the detector into different sets of storage units depending on the event number, enough to store up to 40 events at the same time. In this way 40 AM chips will work in parallel on different events, being able all together to sustain the input rate, 40 times larger the input bandwidth of a single chip. Figure 3 shows a conceptual design of the Trigger Logic.

About 80 boards with 40 AM chips each will be required, for a total of about 3200 chips. The current cost of a batch of 3000 AM chips in 0.18 $\mu$m technology (which has a yield of about 75%) is 30K$.

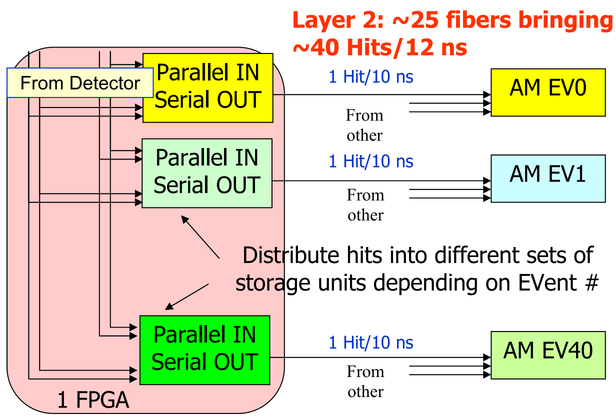


Figure 3: Conceptual design of a possible Tracker Trigger logic using a switch that distributes hits coming from the four pixel layers in a Trigger sector to 40 Associative Memories, one per each event.

The latency budget for a FLT at SLHC is 256 bunch crossings. In the current layout a fair fraction of the latency unavoidably comes from the fiber length of about 100 meters, which corresponds to about 25 bunch crossings. The biggest component comes from the swicth and the AM which are estimated to take about 80 bunch crossings. In order to cope with the allocated budget the detector readout electronics should be executed in less than about 80 bunch crossing, allowing for number of hit fluctuations in the detectors and a margin for the Global Trigger to be executed. This limit does not seem impossible to achieve with existing technologies.

## V. RESULTS AND CONCLUSIONS

A fast estimate of the Tracking Trigger capability has been developed taking into account its possible use together with a single muon FLT. The effect is shown in Fig. 4, where a sizeable reduction is visible at $p_T$ larger than 10 GeV/c, and even lower. The results are preliminary, but as can be seen, the immediate benefit of the usage of a First Level Tracking Trigger combined with muons will bring the single muon rate to a level of about 10 KHz at 10 GeV/c muon $p_T$.

Further studies are required to evaluate possible other applications as well as complete implications both in electronics and in power density.

This work has shown that a first level trigger based on full granularity information of four barrel layers is feasible. The trigger is capable to reduce the FLT rate to manageable levels to be further scrutinized by HLT algorithms running in the filter farms.

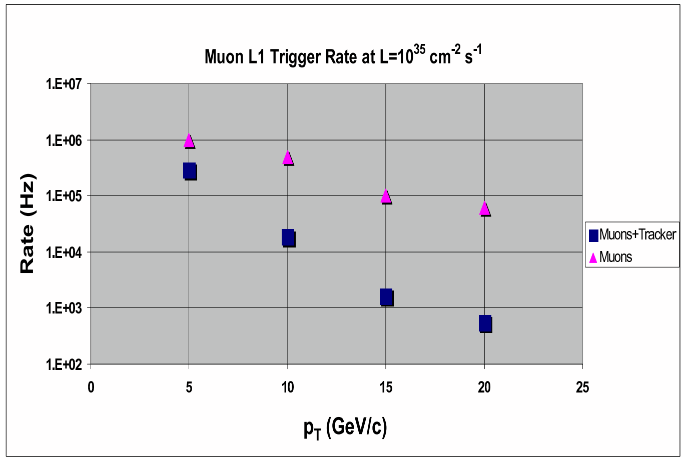


Figure 4: First Level Trigger Rate for single muons at SLHC as a function of the measured Muon $p_T$. Triangles show the estimated rate from the Muon system alone, while squares show the combined Muon plus Tracker First Level Trigger.

## VI. ACKNOWLEDGMENTS

I wish to thank the Conference organizers for having accepted the contribution and the fantastic venue. This talk could not have been possible without useful interactions with Paola Giannetti, Marcel Vos, Mauro Dell'Orso, Roland Horisberger and Francois Vasey.

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