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Proposal for a First Level Trigger using pixel detector for CMS at Super-LHC

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A proposal for a pixel based Level-1 trigger for the Super-LHC is presented. The trigger is based on fast track reconstruction using the full pixel granularity exploiting a readout which connects different layers in specific trigger towers. The trigger will implement the current CMS High Level Trigger functionality using dedicated ASIC and FPGA, in a novel concept of intelligent detector. A possible layout is discussed and implications on data links are evaluated. Finally the performances are shown.

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